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doi:10.15199/48.2024.05.37

Enhanced Half Bridge Series Resonant Inverter for Induction Cap Sealing with Controlled load adaptation

Abstract. *An enhanced half-bridge resonant inverter for induction cap sealing is presented in this research. The proposed method is a combination of a matching transformer, a resonant capacitor, and the series resistance and inductance elements of an induction cap-sealing load. The asymmetrical duty cycle approach is employed to regulate the output power. During the induction cap sealing process, the operating frequency is adjusted automatically through the application of a phase-locked loop control mechanism in order to maintain a steady lagging phase angle between variations in load parameters. The validity of the proposed technique is evaluated using computer simulation, followed by a hardware experiment completed within an operating frequency range of 52.05–53.8 kHz.*

Streszczenie. *W pracy przedstawiono ulepszony półmostkowy falownik rezonansowy do indukcyjnego zgrzewania pokrywy. Proponowana metoda polega na połączeniu transformatora dopasowującego, kondensatora rezonansowego oraz szeregowych elementów rezystancji i indukcyjności obciążenia indukcyjnego zgrzewającego kołpak. Do regulowania mocy wyjściowej stosuje się podejście asymetrycznego cyklu pracy. Podczas procesu zgrzewania indukcyjnego nasadki częstotliwość robocza jest dostosowywana automatycznie poprzez zastosowanie mechanizmu sterującego z pętlą synchronizacji fazowej w celu utrzymania stałego opóźnionego kąta fazowego pomiędzy zmianami parametrów obciążenia. Ważność proponowanej techniki ocenia się za pomocą symulacji komputerowej, a następnie eksperymentu sprzętowego przeprowadzonego w zakresie częstotliwości roboczej 52,05–53,8 kHz.* (***Ulepszony falownik rezonansowy z półmostkiem do indukcyjnego uszczelniania nasadek z kontrolowaną adaptacją obciążenia***)

Keywords: half-bridge resonant inverter**,** induction cap-sealing application**,** asymmetrical duty cycle**,** phase-locked loop control**.**
Słowa kluczowe: półmostkowy falownik rezonansowy, zastosowanie z uszczelnieniem indukcyjnym, asymetryczny cykl pracy.

Introduction

Induction heating has developed growing popularity as a widely employed technique for generating high temperatures, which finding application in various fields including steel melting, brazing, surface hardening, cooking, and cap sealing [1-5]. Optimal frequency selection for the particular application is based on the specific properties of the skin-depth parameters and the geometry of the workpiece [6]. The induction heating bottle sealing machine has application in the sealing of many types of bottles, such as those containing dietary supplements and pharmaceuticals, among other applications. In this area of research, several different power electronic topologies have been developed. Both current-fed [7, 8] and voltage-fed resonant inverters [9-12] are relatively typical and can be successfully used in a variety of applications.

Several articles [11-13] have proposed the use of the voltage source resonant inverter for controlling the series resonant tank. The selection is motivated by the advantages it offers, such as sampling control and minimum power losses during the turn-on transition. Therefore, the use of zero voltage switching (ZVS) is necessary for the voltage source resonant inverter. Moreover, the matching transformer has been used to reduce the high current occurring on the inverter side, while also serving as an isolated circuit that separates the power circuit from the load circuit [12].

In the induction heat application, a voltage source half-bridge resonant (HBR) inverter has been proposed in [13-16]. Various control techniques, including switching frequency variation [13], duty cycle control [15], and pulse density modulation [17]. The method of varying the switching frequency (VFM) is discussed in reference [13], which addresses a problem of increasing inverter losses in the case of adjusted output power under light loads. In addition, research [18] comprises adjusting induction cooking load inverter output power. However, this technique does not monitor load frequency changes. In order to maintain the lagged phase shift, resonant tracking with phase lock loop (PLL) is one of the several power control techniques for resonant inverters that have been presented [19, 20]. The implementation of the phase-locked loop (PLL) approach using digital signal processing (DSP) has been employed in modern inverter technologies because of a requirement for efficient evaluation of real-time controllers [21].

The article discusses the regulatory requirements of the output power of a half-bridge resonant inverter used in an induction cap sealing application, specifically focusing on the implementation of the adjusted duty cycle (ADC) strategy.

The goal of this investigation is to enhance the efficiency of inverters under light load conditions. The proposed approach is distinguishing by its simplicity of implementation and ability to maintain the zero-voltage switching (ZVS) state consistently, even when subjected to load variations. The proposed approach will be critically examined in order to confirm its viability for practical use. The proposed system, modes of operation, circuit analysis, implementation, simulation results, experimental results, and conclusions comprise the structure of this research.

Proposed system

The proposed system for the induction cap sealing application is shown in Fig. 1 and comprises of a full-bridge rectifier, the half-bridge resonant (HBR) inverter, matching transformer (T_{r1}), and the series resonant tank consisting of induction cap sealing load with the resonant capacitor (C_r). A full-bridge rectifier's primary function is to convert alternating current (AC) into direct current (DC). The HBR inverter is comprised of a pair of power MOSFETs, denoted as S_1 and S_2, together with two capacitors, denoted as C_1 and C_2. Fig. 2 shows the induction cap sealing load. Fig. 2(a) shows the top of the induction cap sealing. Fig. (b) shows the components of the induction cap sealing load, which includes a coil and a plastic bottle. The induction cap sealing coil is constructed with a design including 50 strands of copper wire, specifically sized at SWG #31. The location of the aluminum foil inside the plastic bottle closure is shown in Fig. 2(c). Induction cap sealing load can

represented using an equivalent circuit with resistance (R_{eq}) and inductance (L_{eq}), depicted in Fig. 2(d). The plastic bottles (1), (2), and (3) have capacities of 20 ml, 30 ml, and 50 ml, respectively. The measurements of each plastic bottle in which the LCR meter (HIOKI 3532-50) measures R_{eq} and L_{eq} in three different container types are shown in Table 1.

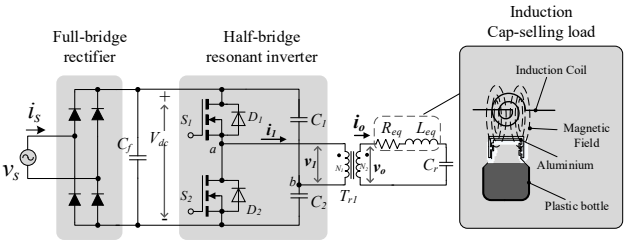

Fig.1. HBR inverter for induction cap sealing application

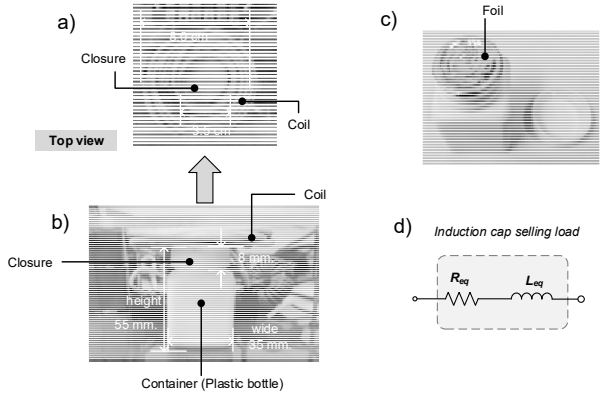

Fig. 2. The induction cap sealing load

Table 1. Different induction cap sealing parameter load sizes

Loads	Size (mm.) [width×length×height]	Parameters	
		R_{eq} (Ω)	L_{eq} (μH)
(1)	27×27×52	0.085	6.12
(2)	35×35×55	0.125	6.58
(3)	42×42×70	0.206	6.95

Operation mode

The HBR inverter configuration seen in Fig. 1 has been substituted with the simplified equivalent circuit represented in Fig. 3 in order to simplify the analysis. Fig. 4 presents the steady-state waveforms of the HBR inverter within the span of one cycle. These waveforms are comprised of gate-signals for switches S_1 and S_2, the voltage across switch S_1 (v_{DS_S1}), the current through switch S_1 (i_{S1}), the voltage across switch S_2 (v_{DS_S2}), the current through switch S_2 (i_{S2}), the output voltage (v_o), the output current (i_o), and output power (p_o). To achieve zero voltage switching (ZVS) operation, the inverter's switching frequency (f_s) is maintained above the frequency f_r at which the inverter's period time (T_s) is equal to $1/f_s$. The duty cycle (D) is the ability of adjusting the average power (P_o).

Fig.5 shows the four different modes of operation that can be successfully achieved by the HBR inverter during one cycle of operating in steady-state. Each mode is depicted in as follows:

Mode 1 for $t_0 - t_1$, when time equals time zero, the switch S_1 is set to in the off state. The negative current i_o passes via the series resonant tank, while the negative current i_1 flows through the anti-parallel diode D_1, the capacitor C_1, and the primary side of the transformer T_{r1}, respectively.

Mode 2 for $t_1 - t_2$, when the anti-parallel diode D_1 is turned off, the switch S_1 conducts. The HBR inverter achieves ZVS functioning in this mode. Positive current i_1 passes via the switch S_1, on the primary side of the transformer T_{r1}, and the capacitor C_2, while positive current i_o passes through the series resonant tank.

Mode 3 for $t_2 - t_3$, when D_2 is active at t=t_2, S_1 is switched off. The anti-parallel diode D_2, transformer T_{r1}'s primary side at a dot, and capacitor C_1 conduct the positive current i_1. Positive current i_o flows through the series resonant tank.

Mode 4 for $t_3 - t_4$, switch S_2 conducts at t=t_3 while anti-parallel diode D_2 is off. This mode allows HBR inverter ZVS operation. In this mode, the switch S_2, transformer T_{r1}, and capacitor C_1 receive the negative current i_1. A negative current flows through the series resonant tank.

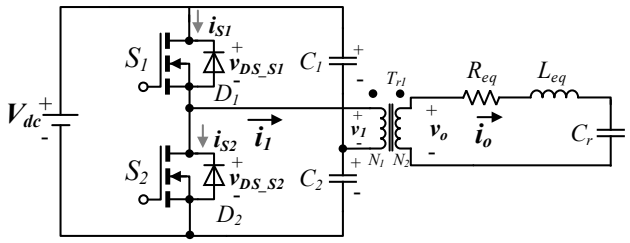

Fig. 3. Simplify circuit of HBR inverter

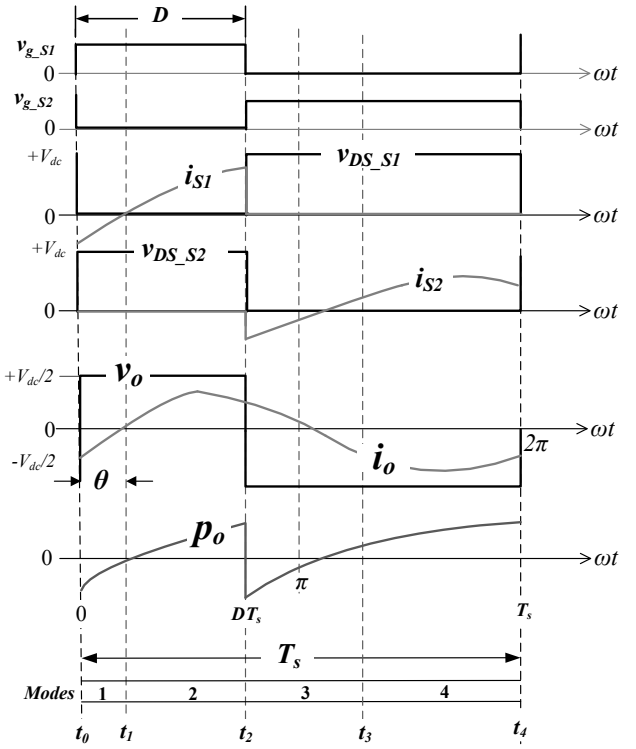

Fig. 4. Typical waveforms of HBR inverter

Circuit analysis

The equivalent circuit of the HBR inverter is shown in Fig. 6 and consists of a series resonant tank and an ADC voltage source. The average power of the HBR inverter is regulated by adjusting the duty cycle D of the output voltage. The regulation of the average power of the HBR inverter is achieved by the adjustment of the duty cycle D of

the output voltage. In Fig. 6, the series resonant tank circuit impedance is expressed by

(1) $$Z_t = R_{eq} + j\left(L_{eq}\cdot\omega_s - \frac{1}{C_r\cdot\omega_s}\right) = R_{eq}\left(1 + jQ\left(\omega_0 - \frac{1}{\omega_n}\right)\right)$$

where the amplitude impedance and phase of Z_t are

(2) $$|Z_t| = R_{eq}\sqrt{1+Q^2\left(\omega_0 - \frac{1}{\omega_n}\right)^2}$$

(3) $$\theta = \tan^{-1}\left(Q^2\left(\omega_n - \frac{1}{\omega_n}\right)\right).$$

The resonant frequency is given by

(4) $$f_r = \frac{1}{2\pi\sqrt{L_{eq}\cdot C_r}}.$$

a)

b)

c)

d)

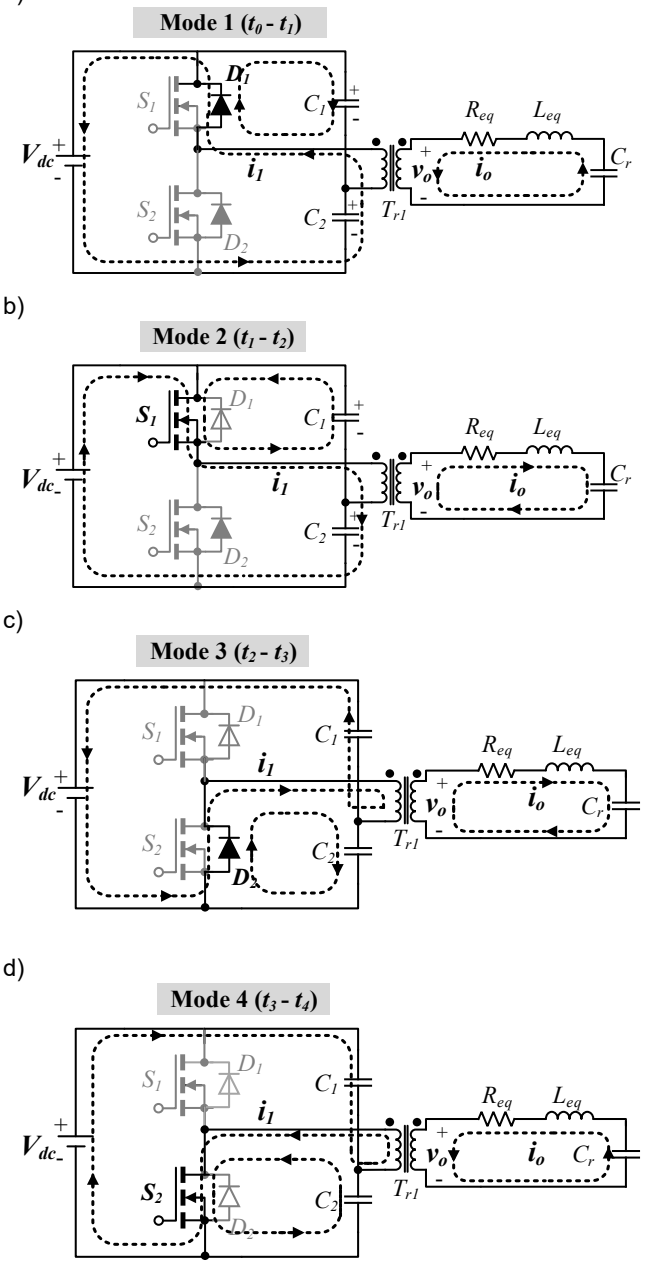

Fig. 5. Operation modes of the HBR inverter

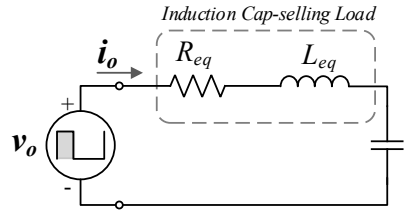

Fig. 6. The equivalent circuit of HBR inverter

The resonant angular frequency is given as

(5) $$\omega_r = \frac{1}{\sqrt{L_{eq}\cdot C_r}}.$$

The definition of the normalized switching angular frequency is

(6) $$\omega_n = \frac{\omega_s}{\omega_r}$$

where $\omega_s = 2\pi f_s$.

The induction cap sealing coil's loaded quality factor is expressed as

(7) $$Q = \frac{\omega_r\cdot L_{eq}}{R_{eq}} = \frac{1}{\omega_r\cdot R_{eq}\cdot C_r}.$$

The voltage across the series resonant circuit (see Fig. 4) is

(8) $$v_o = \begin{cases} +V_2 & for\ \ 0 < \omega_s t \le DT_s \\ -V_2 & for\ \ DT_s < \omega_s t \le T_s \end{cases}$$

where $V_2 = aV_1 = a\left(V_{dc}/2\right)$ and the turn ration of transformer T_{r1} as $a = N_2/N_1$. The instantaneous output voltage using the Fourier series is expressed as

(9) $$v_o = \sum_{n=1}^{\infty} V_{om(n)}\sin\left(n\omega_s t + \phi_n\right).$$

The amplitude of the voltage v_o is

(10) $$V_{om(n)} = \sqrt{\left(a_n\right)^2 + \left(b_n\right)^2}$$

where the coefficients are denoted by

(11) $$a_n = \frac{1}{T_s}\int_0^{T_s} v_o\cos n\omega_s t dt = \frac{V_{dc}}{n\omega_s T_s}\left(2\sin n\omega_s DT_s - \sin n\omega_s T_s\right)$$

(12) $$b_n = \frac{1}{T_s}\int_0^{T_s} v_o\sin n\omega_s t dt = \frac{V_{dc}}{n\omega_s T_s}\left(1 - 2\cos n\omega_s DT_s + \cos n\omega_s T_s\right)$$

The phase shift of the voltage v_o is

(13) $$\phi_n = \tan^{-1}\left(\frac{a_n}{b_n}\right)$$

The instantaneous output current is

(14) $$i_o = \sum_{n=0}^{\infty} I_{om(n)}\sin\left(n\omega_s t - \theta\right)$$

where the amplitude of the current i_o is

(15) $$I_{om(n)} = \frac{V_{om(n)}}{|Z_t|} = \frac{V_{om(n)}}{\pi R_{eq}\sqrt{1+Q^2\left(\omega_n - \frac{1}{\omega_n}\right)^2}}$$

Therefore, the average power of the HBR inverter is

$$P_o = \sum_{n=1}^{\infty} R_{eq}\left(I_{om(n)}\right)^2 = \sum_{n=1}^{\infty} \frac{\left(V_{om(n)}\right)^2}{2R_{eq}\left(1+Q^2\left(n\omega_n - \frac{1}{n\omega_n}\right)^2\right)}$$

$$P_o = \sum_{n=1}^{\infty}\left(\frac{V_{dc}}{n\omega_s T_s}\right)\frac{\sqrt{\left[\beta_1-\beta_2\right]^2+\left[1-\beta_3+\beta_4\right]^2}}{2R_{eq}\left(1+Q^2\left(n\omega_n - \frac{1}{n\omega_n}\right)^2\right)} \quad (16)$$

where $\beta_1 = 2\sin n\omega_s DT, \beta_2 = \sin n\omega_s T_s, \beta_3 = 2\cos n\omega_s DT_s$, and $\beta_4 = \cos n\omega_s T_s$.

Implementation

The HBR inverter circuit is shown in Fig. 7 (a) which includes two power MOSFETs of S_1 and S_2 and two capacitor C_1 and C_2. Fig. 7 (b) shows the induction cap sealing load as the series resonant tank. The conditioning circuit that has been used to detect the signals of voltage v_o and current i_o is shown schematically in Fig. 7 (c). The schematic of the controlled HBR inverter circuit (Fig. 7 (d)) uses Texas Instruments' TMS320F28335 (DSP#1) on a 32-bit fixed-point 150 MHz with a 10 kHz sample rate. The PI-controller provides the phase controller inside the Phase-Locked Loop (PLL) algorithm, with its main purpose being the correction of the error signal that arises from the difference between the phase command (φ_{com}) and the measured lagging phase. A variable resistor, denoted as R_1, is employed for the purpose of adjusting the power command (P_{o_ref}) of the resonant inverter. The proportional-integral (PI) controller is utilized by the power controller. This controller s necessary in order to correct for the error signal that is produced by the actual power P_o and the referance power P_{o_ref}. The signal produced by PI is limited by the power limitation (P_{o_limit}). After that, it will be supplied for the purpose of conducting a comparative analysis. The output signal produced by the voltage-controlled oscillator (VCO) is used to calculate a date time (td) of 1.8 μsec for the gate signal of the resonant inverter. The gate signals for MOSFETs S_1 and S_2 are produced by the optically isolated gate drivers U_3 and U_4, as illustrated in Fig. 7 (e). Fig. 8 illustrates the experimental arrangement for the proposed strategy. A specific plastic cap with a disk made of aluminum foil is used. After the bottle cap is screwed on firmly it is placed under an induction sealing coil immediately. The electromagnetic field produced by the coil induces thermal energy in the aluminum disk, resulting in its temperature increase. The disk is coated and subsequently laminated, resulting in its melting and merging with the bottle's mouth.

Simulation results

The results of the simulations of the HBR inverter's output power variations under varying duty cycles (D) of 0.2, 0.3, and 0.5 are presented as in Fig. 9, 10, and 11, respectively. These results serve to verify the proposed system. In Fig. 9, the simulation results show a duty D of 0.2 for adjusting the power of a load (1), a power P_o of 120 W, a frequency f_s of 53.5 kHz, and a delayed phase shift of 34°. The simulation results for the voltage v_{DS_S1} and current i_{S1} during the ZVS operation are shown in Fig. 9(a). The simulation results for a peak voltage value v_o of 15.5 V and a peak current value i_o of 12.8 A are displayed in Fig. 9(b). The simulation result for a power peak p_o of 185 W is shown in Fig. 9(c).

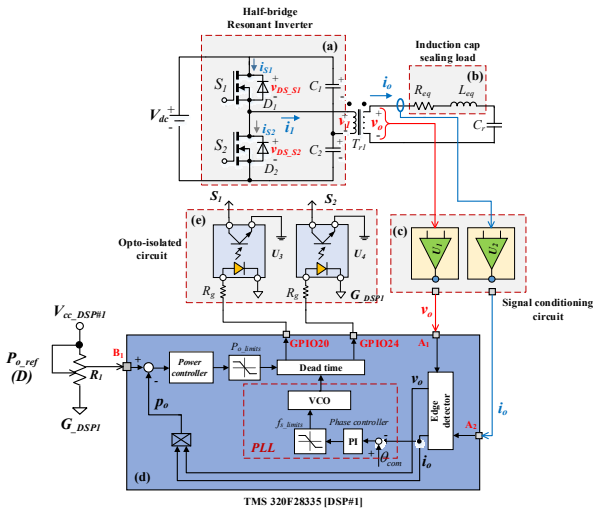

Fig.7. A schematic diagram of the proposed method's implementation: a) HBR inverter circuit; b) induction cap sealing load with a capacitor C_r; c) the conditioning circuit; d) the digital signal processing; e) The optically isolated gate drivers

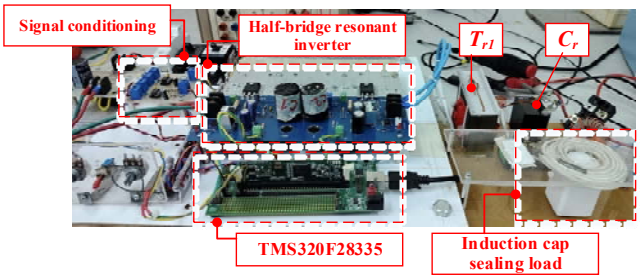

Fig.8. The experimental setup

Table 1. Setup parameters for experimentation and measurements

Experimental parameters		Values	Unit
V_{dc}		310	V
C_f (Electrolytic capacitor)		2200	μF
$C_1 = C_2$ (Electrolytic capacitors)		150	μF
C_r (Metallized Polypropylene Capacitor)		2	μF
R_1		100	kΩ
MOSFETs S_1 and S_2 [IRFP 460]	V_{DSS}	500	V
	I_D	20	A
	$R_{DS(ON)}$	0.27	Ω
Matching transformer [T_{r1}]	Ferrite core size E70 is 70.5 mm long, 32 mm wide, and 33.2 mm deep.		
	N_1	40	turns
	N_2	4	turns
	a	0.1	-
Zero crossing detectors U_1 and U_2		TLV7011 of Texas Instrument	
Opto-isolators U_3, U_4, and U_5		TLP250 of Toshiba	

Fig. 10 shows the results of a medium power HBR inverter simulation that adjusts the power of a load (2) with duty D = 0.3, f_s = 52.5 kHz, and 35° lagging phase shift. Fig. 10 (a) shows ZVS operation's simulated voltage v_{DS_S1} and current i_{S1}. The results of simulations for the peak voltage v_o of 15.5 V and current i_o of 20.0 A are represented in Figure 10(b). As showed in Fig. 10 (c), the simulation result of thepeak value of the power p_o is 440 W. The simulation results for an HBR inverter that regulates the power of a load (3) with a duty D of 0.5, f_s of 52.0 kHz, and a lagging phase shift of 36° are depicted in Fig. 11. Fig. 11 (a) shows

the voltage v_{DS_S1} and current i_{S1} under ZVS operation. The simulation results for the peak voltage v_o of 15.5 V and current i_o of 29.95 A are presented in Figure 11 (b). The peak value of power p_o, 440 W, is presented in Fig. 11 (c).

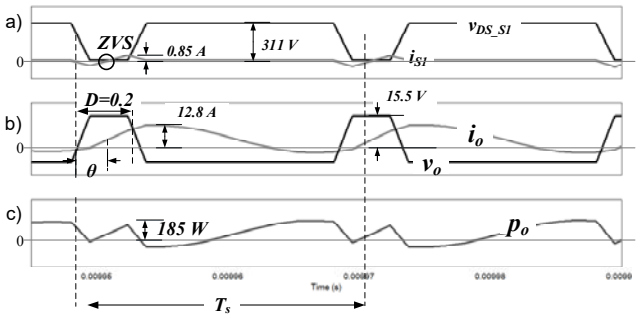

Fig.9. Simulated results of the HBR inverter with D =0.2; (a) v_{DS_S1} and i_{S1} waveforms, (b) v_o and i_o waveforms, and (c) p_o waveform

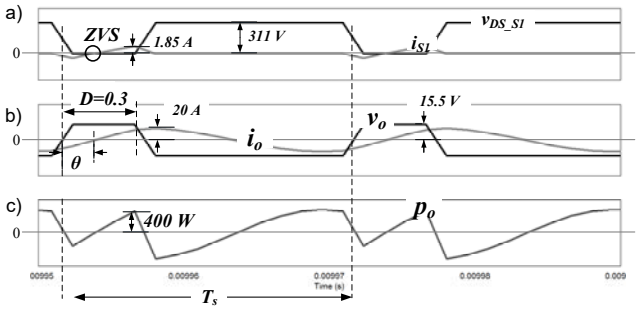

Fig.10. Simulated results of the HBR inverter with D =0.3; (a) v_{DS_S1} and i_{S1} waveforms, (b) v_o and i_o waveforms, and (c) p_o waveform

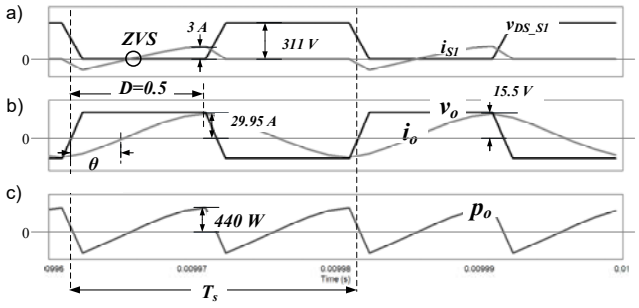

Fig.11. Simulated results of the HBR inverter with D =0.5; (a) v_{DS_S1} and i_{S1} waveforms, (b) v_o and i_o waveforms, and (c) p_o waveform

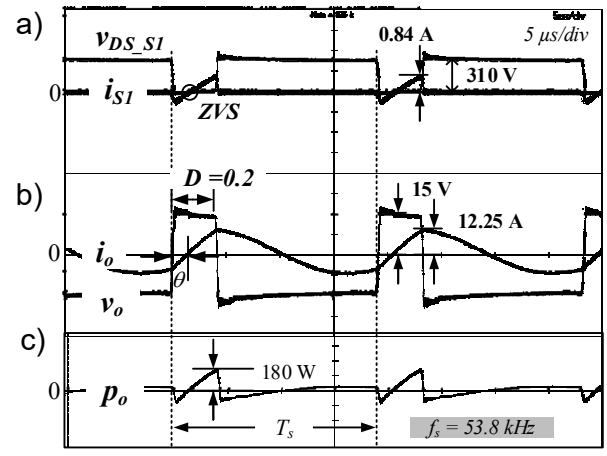

Fig.12. Experimental results of HBR inverter for D = 0.2: (a) v_{DS_S1} and i_{S1} waveforms (v_{DS_S1}: 200V/div, i_{S1}: 1.0 A/div time: 5 µs/div); (b) v_o and i_o waveforms (v_o: 10 V/div, i_o: 10.0 A/div, time: 5 µs/div) (c) p_o waveform (p_o:100 W/div, time: 5 µs/div)

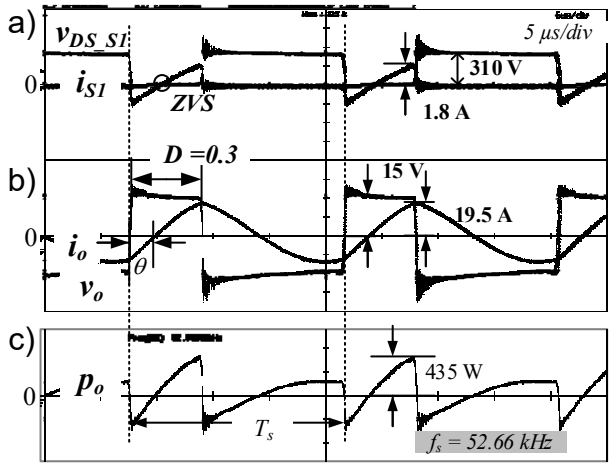

Fig.13. Experimental results of HBR inverter for D = 0.3: (a) v_{DS_S1} and i_{S1} waveforms (v_{DS_S1}: 200V/div, i_{S1}: 2.0 A/div time: 5 µs/div); (b) v_o and i_o waveforms (v_o: 10 V/div, i_o: 10.0 A/div, time: 5 µs/div) (c) p_o waveform (p_o:150 W/div, time: 5 µs/div)

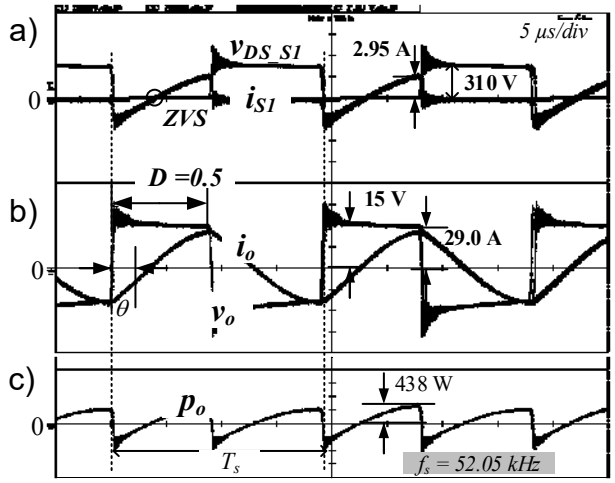

Fig.14. Experimental results of HBR inverter for D = 0.5: (a) v_{DS_S1} and i_{S1} waveforms (v_{DS_S1}: 200V/div, i_{S1}: 2.0 A/div time: 5 µs/div); (b) v_o and i_o waveforms (v_o: 10 V/div, i_o: 15.0 A/div, time: 5 µs/div) (c) p_o waveform (p_o:400 W/div, time: 5 µs/div)

Experimental results

Consequently, those problems will be resolved using the proposed strategy. The prototype for the induction cap sealing application (see Fig. 8), has been created in order to validate the experimental results. In order to confirm the theoretical research, the digital oscilloscope (YOKOGAWA DLM2024) was employed to measure the experimental results of voltage v_o, current i_o, and power p_o. These results are shown in Fig. 12 - 14. As a result, the proposed approach will be employed to solve the mentioned previously problems. The experimental waveforms of load (1) with an adjusted duty cycle D of 0.2 at a frequency f_s of 53.8 kHz are shown in Fig. 12.

The process of completely sealing the bottle required a total duration of 45 seconds. As shown in Fig. 12 (a), the peak values of the experimental voltage v_{DS_S1} and current i_{S1} waveforms are 310 V and 0.84 A, respectively. The experimental waveforms of the current i_o and voltage v_o vo are shown in Fig. (b). At the peak of the waveforms, the current i_o measures 12.25 A, while the voltage vo measures at 15 V. When the lag phase shift θ is 35.45°., the PLL control tracks the resonance frequency during load alteration. Fig. 12 (c) shows the instantaneous power p_o

with a peak p_o of 180 W. The experimental waveforms for a medium load of load (2) are illustrated in Fig. 13. The frequency f_s is 52.66 kHz, and the duty cycle D has been adjusted to 0.3. This process of completely sealing the bottle required 40 seconds in total. The experimental waveforms in Fig. 13 (a) show peak values of 310 V for the voltage $v_{DS_S1}$and 1.8 A for the current i_{S1}. Fig. 13 (b) shows the experimental waveforms of the voltage v_o and current i_o. The peak voltage v_o and current io are measured to equal 15 V and 19.5 A, respectively. The PLL control tracks resonance frequency at 35.8° lag phase shift during load change. Fig. 13 (c) shows the instatneus power p_o with a peak po of 435 W. Fig. 14 shows the experimental waveforms according to the maximum load of load (3). The duty cycle D is set to 0.5, and the frequency f_s is 52.05 kHz. The duration of the operation of completely sealing the container is 35 seconds. The experimental waveforms in Fig. 14 (a) show peak values of 310 V for the voltage v_{DS_S1} and 2.95 A for the current i_{S1}. Fig. 14 (b) shows the experimental waveforms of the voltage, v_o, and current, i_o. The peak voltage, v_o, is measured at 15 V, while the peak current, i_o, is measured at 29 A. At a load variation of phase shift θ of 36◦, the PLL control maintains resonance frequency tracking. Fig. 14 (c) shows the instantaneous power p_o with a peak po of 438 W.

The comparisons of the calculated and experimental efficiencies of the HBR inverter using the duty cycle method with the conventional method are shown in Fig. 15. The parameters provided in Tables 1 and 2 have been used for this analysis. The conventional control configuration [13] is similarly shown with the same parameter settings. The proposed method is capable of maintaining ZVS operating throughout the heating process, from light load to maximum load. This means that the proposed method is greater to the traditional method when it concerns to modifying the heating process.

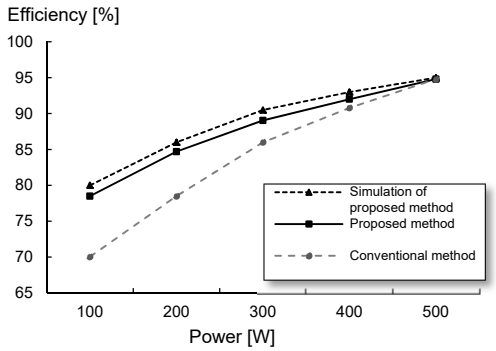

Fig.15. A comparative analysis of the the efficiency of the conventional method and the proposed method

Conclusions

In this research, an improved HBR topology is presented for use with induction cap sealing. The adjusted duty cycle control is offered for adjusting the inverter's output power. Experiments and simulation results have been used to verify that the proposed approach is valid. The advantages provided by the proposed control technique are as follows.

(1) Through a wide power adjustment range, the proposed control can be used of modifying the output power of a series resonant tank operating under ZVS conditions.

(2) The improved efficiency of power transfer to the load during the induction cap sealing process is achieved by the utilization of resonant-frequency tracking and duty cycle control, resulting in minimum loss.

(3) The control system has a simple structure and can be simply implemented. The circuit designs and control methodology developed in this research are suitable for a wide range of applications that necessitate the regulation of output power when load parameter fluctuations are present.

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