1. Volodymyr HRABKO[1], 2. Dmytro PROTSENKO[1], 3. Andrii BARTETSKYI[2], 4. Iryna GUNKO[2],
5. Ludmila SHVETS[2], 6. Kateryna CHMYKH[2], 7. Olena TRUKHANSKA[2], 8. Vadym RYABOSHAPKA[2]

Vinnytsia National Technical University (1), Vinnytsia National Agrarian University (2)
ORCID: 1. 0000-0002-4666-1758; 2. 0000-0002-5611-7262; 3. 0009-0001-7628-4789; 4. 0000-0002-2441-9469;
5. 0000-0002-4364-0126; 6. 0000-0001-8873-4436; 7. 0000-0001-8481-8878; 8. 0000-0003-1812-1030

System diagnostics of braking circuits of frequency-controlled asynchronous electric drives converters using FPGA

Abstract. This article explores the application of FPGA technology in diagnosing braking circuits for frequency-controlled asynchronous electric drive converters. FPGA enables real-time monitoring, rapid fault detection, and system protection, enhancing the reliability and safety of electric drive converters. It optimizes performance, minimizes downtime, and reduces maintenance costs.

Streszczenie. W artykule omówiono zastosowanie technologii FPGA w diagnostyce obwodów hamulcowych sterowanych częstotliwościowo asynchronicznych przekształtników napędu elektrycznego. FPGA umożliwia monitorowanie w czasie rzeczywistym, szybkie wykrywanie usterek i ochronę systemu, zwiększając niezawodność i bezpieczeństwo przekształtników napędu elektrycznego. Optymalizuje wydajność, minimalizuje przestoje i zmniejsza koszty konserwacji. (Diagnostyka systemowa obwodów hamulcowych przekształtników asynchronicznych napędów elektrycznych sterowanych częstotliwością z wykorzystaniem FPGA)

Keywords: system diagnostics, braking circuits, frequency-controlled, asynchronous electric drives, converters, FPGA technology.
Słowa kluczowe: diagnostyka systemu, obwody hamowania, sterowanie częstotliwością, asynchroniczne napędy elektryczne.

Introduction

In today's automated world, electric drive systems are essential in various industries due to their versatility and energy efficiency. However, they require meticulous maintenance for peak performance and safety, with the braking circuit playing a critical role in controlled deceleration and machinery stoppage.

The introduction of frequency-controlled asynchronous electric drives with converters has increased system complexity, emphasizing the need for robust diagnostics and monitoring. This article explores braking circuit diagnostics in these drives using Field-Programmable Gate Arrays (FPGAs), enabling real-time monitoring and analysis to enhance reliability and safety. Rapid fault detection and system protection reduce downtime and maintenance costs while optimizing performance.

Subsequent sections cover diagnostic principles, methodologies, and practical FPGA implementations, showcasing innovative solutions for improved industrial process efficiency and sustainability.

Analysis of literary sources and problem statement

Increasing the environmental friendliness of energy efficiency and the quality of production involves the use of energy-efficient technologies [1]. In particular, the frequency-controlled asynchronous electric drive has gained extremely wide application in industry due to its high energy characteristics. Inertial mechanisms with frequent braking of the electric drive create the need for additional equipment of the frequency-controlled asynchronous electric drive with a system of energy reset to the braking resistor. They are mainly lifting and transport mechanisms, urban electric transport, electric drives in the field of metallurgy, metalworking [2-3].

As a consequence of the use of frequency-controlled asynchronous electric drives with energy reset to the braking resistor, emerges a need in designing tools for diagnosing of braking frequency-controlled asynchronous electric drives [4]. Since premature or unexpected failure of the brake circuit of a frequency-controlled asynchronous electric drive can lead to production downtime, deterioration of product quality, damage to technological equipment, and can also pose a threat to the life and health of production personnel.

In article [5-6], an FPGA device based on a neurogenetic implementation with a back-propagation neural network is proposed for more efficient and almost instantaneous fault diagnosis. The authors note that thanks to the FPGA, a more energy-efficient and almost instantaneous diagnosis is achieved in comparison to other means, but the authors do not consider the diagnosis of the braking circuits of the frequency converter. In the article a hardware implementation of an FPGA-based fault diagnosis device is proposed, which allows real-time fault detection using information entropy and artificial neural networks as tools for analyzing of the information content of 3-axis vibration signals from a rotary machine during transient processes. But the proposed device does not allow determining the current state of the system in process of its operation, which makes it unsuitable for solving the task of diagnosing brake circuits of frequency converters. In [7-9], a device for diagnosing a frequency converter based on FPGA is proposed. The principle of operation is based on the analysis of the deviation of the line voltage from the standard value. The authors emphasize that the usage of FPGA allows to significantly increase the speed of signal processing by 50%. However, the authors do not consider the diagnosis of the brake circuits.

Purpose and tasks of research

The purpose of the work is to increase the reliability of the frequency-controlled asynchronous electric drive by creating a system for diagnosing its braking circuit based on a mathematical model of signal processing using logic-time functions.

Research results

Programmable logic integrated circuits (FPGAs), or FPGAs (field programmable gate arrays) are digital integrated circuits (ICs) consisting of programmable logic blocks and programmable connections between these blocks. The abilities to configure these devices allow development engineers to solve numerous different problems. Depending on the manufacturing method, FPGAs can be programmed either once or multiple times. Devices that can be programmed only once are called one-time programmable [10-15].

There is a large number of different types of digital integrated circuits, including such as "loose logic" (small components containing a few simple fixed logic functions), memory devices and microprocessors. In this case, interest is generated by programmable logic devices (PLDs), specialized custom integrated microcircuits ASIC (application specific integrated circuit), specialized integrated circuit, ASSP (application specific standard parts) and FPGA. Moreover, the term PLC combines two types of devices: simple programmable logic devices (simple PLCs) and complex programmable logic devices (complex PLCs) [16].

In work [17-18], a mathematical model of the system for diagnosing the brake circuit of the converter of the frequency-controlled asynchronous electric drive using logic-time functions (LCF) is proposed and described the principle by which a table of exemplary states of the brake circuit of the frequency-controlled asynchronous electric drive is formed is described (table 1). In the table of the states of the brake circuit of the converters of the frequency-controlled asynchronous electric drive (table 1), the number "1" corresponds to hitting the parameter into the tolerance zone; "0" – going off the tolerance zone of the corresponding diagnostic sign.

Table 1. States of the brake circuit of the converter of the frequency-controlled asynchronous electric drive

stand up	Diagnostic signs of the brake circuit				
	ΔUC	Uvs0	Ig	T°r	T°vs0
Q0	1	1	1	1	1
Q1	1	0	1	1	0
Q2	0	1	0	1	1
Q3	0	0	1	1	0
Q4	0	0	0	1	1

In table 1: Q0 – operational condition; Q1 – operational condition, with overheating of the power module; Q2 – faulty braking resistor; Q3 – critical condition; Q4 is a faulty condition. ΔUC – overvoltage on the filter capacitor; Uvs0 – voltage on the IGBT module; Ig – current through the braking resistor; T°r is the temperature of the braking resistor; T°vs0 is the temperature of the IGBT module.

According to Table 1, exemplary LPFs are formed and as a result of successive addition modulo two of two LPFs (1) from the formed and measured signals, which are diagnostic signs of the current state of the brake circuit, we obtain the resulting LPFs, from which we take as a diagnostic conclusion the LPF which has the smallest segment of existence.

In the general case, the operation of addition modulo two of two LCHFs $f_1(t, t_1, T_1)$ and $f_2(t, t_2, T_2)$ is described by expression (1) [9],

$$f_1(t, t_1, T_1) \oplus f_2(t, t_2, T_2) =$$

(1)
$$\begin{cases} t - t_m, & if \ t_m < t \le t_j, \\ t - (t_m + T_m), & if \ (t_m + T_m) < t \le (t_j + T_j), \\ 0, & if \ (t \le t_m) \wedge (t_i < t \le (t_m + T_m)) \wedge (t > (t_j + T_j)) \end{cases}$$

where $t_m = min\{t1, t2\}$, T_m is the duration of the segment of existence corresponding to the time coordinate tm, $t_j = max\{t1, t2\}$, T_j is the duration of the segment of existence corresponding to the time coordinate t_j.

For example, a graphic illustration of the addition modulo two of two LCHFs $f_1(t, t_1, t_2, \Delta_i, T_1, T_2)$ and $f_2(t, t_1, t_2, \Delta_i, T_1, T_2)$, is presented in fig. 1, and the analytical solution is described by expression (2).
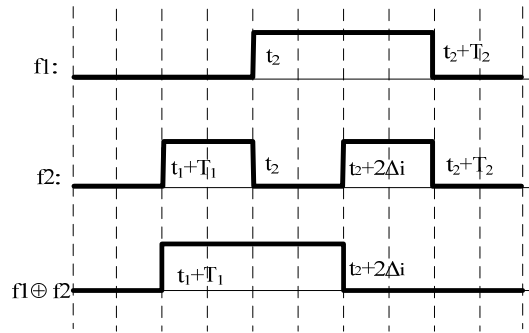

Fig. 1. Graphical illustration of the exclusive disjunction operation of two LCHFs

(2)
$$\begin{aligned} &f_1(t, t_1, t_2, \Delta_i, T_1, T_2) \oplus f_2(t, t_1, t_2, \Delta_i, T_1, T_2) = \\ &\begin{cases} t - (t_1 + T_1), & if \ (t_1 + T_1) < t \le (t_2 + 2\Delta_i), \\ 0, & if \ (t < (t_1 + T_1)) \wedge (t > (t_2 + 2\Delta_i)). \end{cases} \end{aligned}$$

In work [18-20], there was proposed a device for diagnosing brake circuits of converters of frequency-controlled asynchronous electric drives, which was implemented with digital hardware using standard blocks of discrete devices. Taking into account the requirements of modern instrumentation, energy efficiency, accuracy and speed, we implement this device using programmable logic. As a basis, we will take the Altera MaxII EMP240T100C5 FPGA, which will be programmed in the Quartus II 9.0 environment.

The structural diagram of the device for diagnosing brake circuits of converters of frequency-controlled asynchronous electric drives using FPGA is shown in Fig. 2.
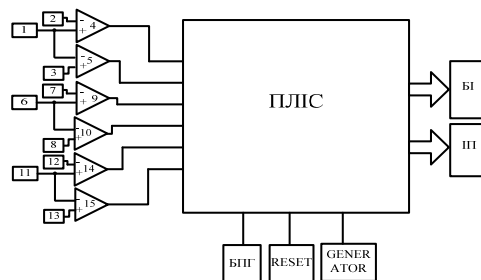

Fig. 2. Structural diagram of the device for diagnosing brake circuits of converters of frequency-controlled asynchronous electric drives using FPGA

In Figure 2: blocks from 1 to 15 are designed to determine whether the measured brake circuit signals belong to the range of permissible values and, accordingly, to convert input analog signals into digital information, FPGA is a programmable integrated logic circuit, BPG is a braking start block, RESET is a reset block of the circuit; GENERATOR – reference frequency generator; BI – display unit; IP – interface converter. As a result of the development of the software, a structural diagram of the device for diagnosing brake circuits of converters of frequency-controlled asynchronous electric drives in the Quartus II environment was obtained, shown in fig. 3.

The main program shown on the structure (see Fig. 3.) consists of six blocks, which represent the main functional parts of the scheme proposed in the second section of the mathematical model for diagnosing brake circuits of converters of frequency-controlled asynchronous electric drives with the use of LFC.

The "Selektor" block is designed to form the LCP of the current state and compare it with the LCP of exemplary states. The implementation of the block is shown in Fig. 4.
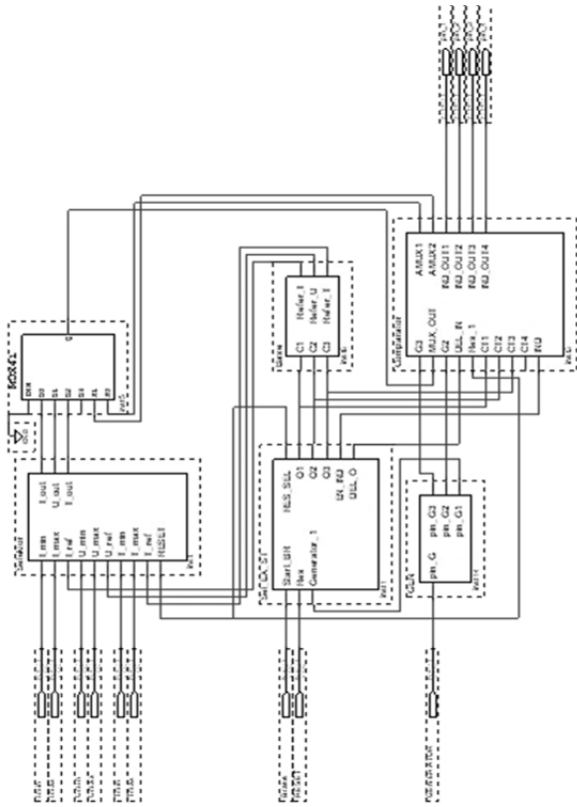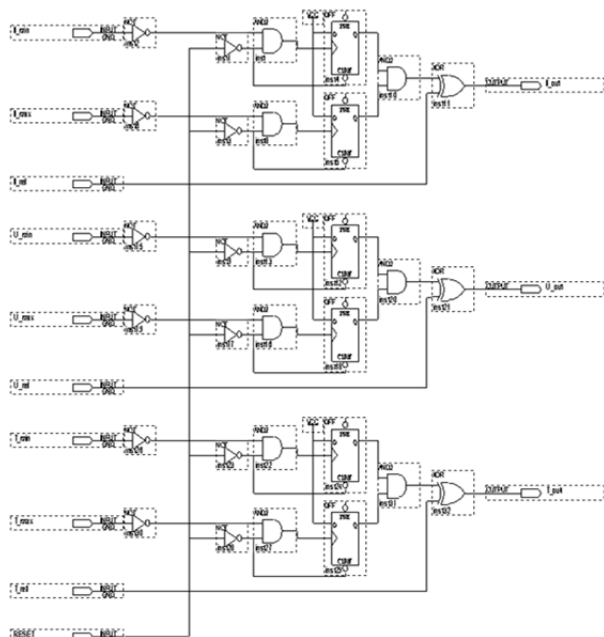
Fig. 3. Structural diagram of the device for diagnosing braking circuits of converters of frequency-controlled asynchronous electric drives in the Quartus II environment

Fig. 5. Structural diagram of the "Sel_EX_ST" block

Fig. 4. Structural diagram of the Selektor block

Fig. 6. Structural diagram of the "Base" block

The block "Sel_EX_ST" (Fig. 5.) is designed for the generation of sampling signals of the LPF exemplary states from the block "Base" (Fig. 6).

The "Comparator" block (Fig. 8) is designed to determine the segment of existence of the LFCs obtained as a result of the comparison by modulo two and to determine the LFCs with the smallest segment of existence. The "GEN" block (Fig. 7) is designed for the formation of reference frequencies that ensure the correct operation of the device.
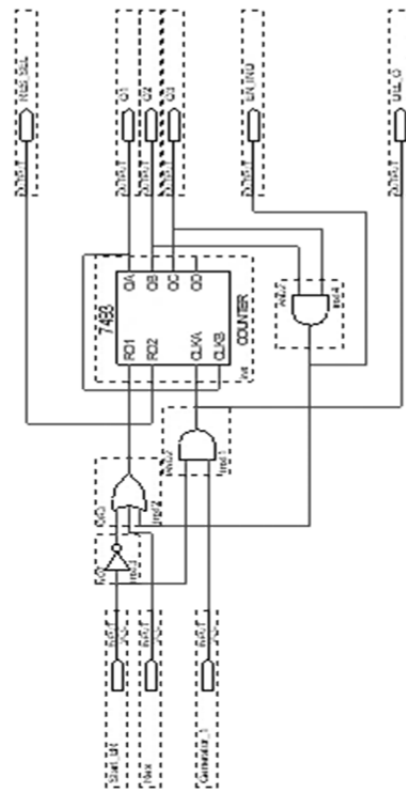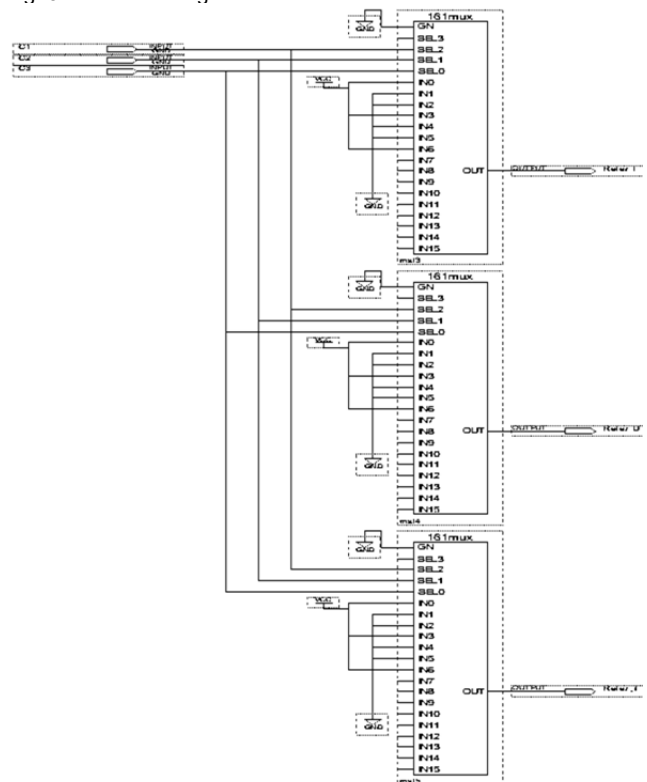
The rest of the elements and blocks used to build the circuit are standard elements of the Quartus II environment library, so their detailed review is irrelevant.

The functionality of the device is proven by the results of its testing, while in real conditions of operation of the frequency converter, which switches to the braking mode. At the same time, additional test disturbances were introduced to study the system response.
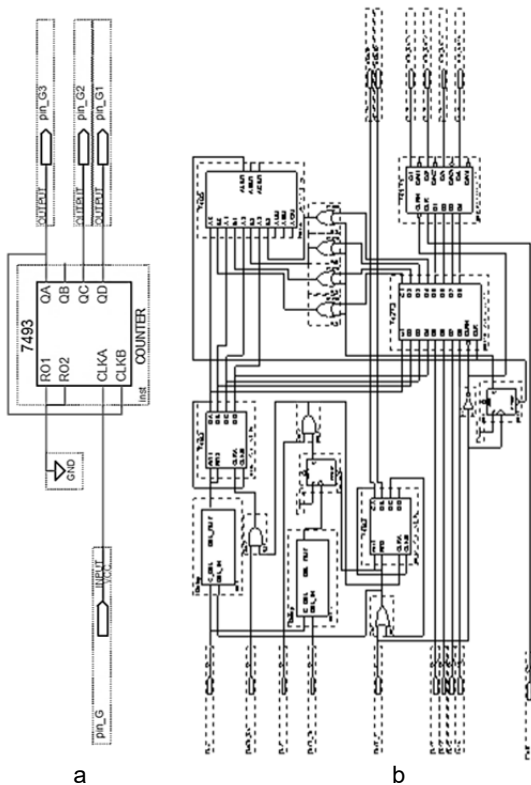
a   b

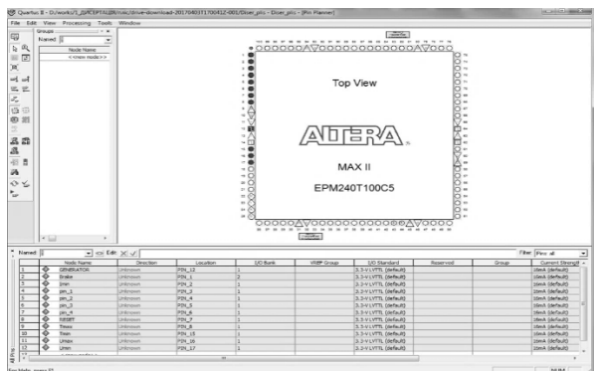Fig. 7. Structural diagram of the "GEN" block (a) and "Comparator" block (b)

Fig. 8. Input and output configuration window of the chip

Conclusions

This implementation allows to significantly increase the speed and the reliability of the device, since only one microcircuit is used, and also allows to reduce power consumption and size compared to the implementation on integrated microcircuits, which, accordingly, significantly reduces its cost.

Authors: HRABKO Volodymyr – *Dr. Eng. Sc., Professor, Vinnytsia National Technical University (95 Khmelnytske Shosse str., Vinnytsia, 21000, Ukraine);* PROTSENKO Dmytro – *PhD of Engineering, Associate Professor, Vinnytsia National Technical University (95 Khmelnytske Shosse str., Vinnytsia, 21000, Ukraine)*; BARTETSKYI Andrii – *PhD of Engineering, Senior lecturer, Vinnytsia National Agrarian University (Sonyachna str., 3, Vinnytsia, 21008, Ukraine);* GUNKO Iryna – *PhD of Engineering, Associate Professor, Vinnitsa National Agrarian University (Solnechnaya str., 3, Vinnitsa,Ukraine, 21008, e-mail: maniy@ukr.net);* SHVETS Ludmila – *PhD of Engineering, Associate Professor, Vinnitsa National Agrarian University (Solnechnaya str., 3, Vinnitsa,Ukraine, 21008, e-mail: shlv0505@i.ua);* CHMYKH Kateryna – *PhD Student (Engeneering), Vinnitsa National Agrarian University (Solnechnaya str., 3, Vinnitsa,Ukraine, 21008, e-mail: catherina099@gmail.com);*

TRUKHANSKA Olena – *PhD of Engineering, Associate Professor, Vinnitsa National Agrarian University (Solnechnaya str., 3, Vinnitsa,Ukraine, 21008, e-mail: seaswallow@ukr.net);* RYABOSHAPKA Vadim – *PhD of Engineering, Senior lecturer, Vinnitsa National Agrarian University (Solnechnaya str., 3, Vinnitsa,Ukraine, 21008, e-mail:* vadymryaboshapka@gmail.com).

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