1. Rafał KOPACZ[1]

Warsaw University of Technology (1).
ORCID: 1. 0000-0002-2054-9821.

doi:10.15199/48.2024.03.03

Quasi-two-level method as an universal approach for voltage balancing of series-connected SiC MOSFETs

Abstract. *This study showcases the quasi-two-level (Q2L) control method for voltage balancing of series-connected SiC MOSFETs. Medium and high voltage applications require stacking of power semiconductor devices in cells or series-connection in order to reach appropriate blocking capabilities. The simplified quasi-two-level method, only to ensure balancing among the series-connected transistors can be deemed as a universal method for voltage balancing of stacked power devices or cells. A generalized control strategy and a more specific application for a medium voltage dc-dc converter are presented, with both validated using experimental models at up to 1.5 kV dc voltage.*

Streszczenie. *Niniejsze studium przedstawia metodę sterowania quasi-dwupoziomowego (Q2L) w celu balansowania napięcia na szeregowo połączonych tranzystorach SiC MOSFET. Zastosowania średniego i wysokiego napięcia wymagają łączenia szeregowego półprzewodnikowych przyrządów mocy w celach, bądź bezpośrednio. Metoda quasi-dwupoziomowa, uproszczona tylko w celu zapewnienia zrównoważenia napięcia, może stanowić uniwersalną metodę balansowania napięć między szeregowo połączonymi tranzystorami. Na bazie eksperymentów, przedstawiona została uniwersalna metoda sterowania, a także konkretne zastosowanie w przekształtniku dc-dc średniego napięcia.* ***(Metoda quasi-dwupoziomowa jako uniwersalne podejście do balansowania napięcia szeregowo połączonych tranzystorów SiC MOSFET)***.

Keywords: multilevel converters. power electronics, series connection, SiC MOSFET.
Słowa kluczowe: energoelektronika, przekształtniki wielopoziomowe, szeregowe łączenie, SiC MOSFET.

Introduction

With the constant progression in wide-bandgap semiconductor technology, such as Silicon Carbide, new power devices have been successfully introduced into the market bringing many advantages compared to conventional Silicon-based products [1-4]. Namely, higher sustainable voltages, switching speeds, as well as lower power losses. These characteristics designate SiC power devices, especially MOSFETs, as the transistors of choice for medium voltage (MV) power electronics.

However, even though there are widely available SiC-based devices with blocking voltages at 3.3 kV [5], and devices rated as high as over 10 kV were presented in the literature [6, 7], neither is enough for direct application in a two-level system throughout the whole medium voltage spectrum. Therefore, a stacking approach, either in a straightforward series connection of transistors (Fig. 1a); or more sophisticated cell-based stacks, as in a modular multilevel converter (MMC) depicted in Fig. 1b, or a flying capacitor converter (FCC) as presented in Fig. 1c; is required [8]. However, these methods are characterized by several drawbacks.

Starting off, the simplest approach is the direct series connection or power transistors. Theoretically, stacking the devices in series provides the possibility to share the high voltage across the transistors. However, in reality, due to several factors, such as circuit and semiconductor non-idealities, the voltage is not split equally between the transistors, which may lead to the breakage of a device, and then the whole converter. Therefore, applying supplementary voltage balancing methods is a necessity, deeming the theoretically straightforward system more complicated [9]. The level of added complexity highly depends on the type of balancing method. For example, a relatively simple approach of adding passive snubber circuits [10] does not require additional control measures. However, at the expense of lowered power density and substantial power losses [11]. On the other hand, there are active voltage balancing methods based on actively delaying the control signals of the transistors [12] or modifications of the gate drive circuits [13, 14]. While these methods are essentially lossless, they require severe alterations in the control system and in the circuits, e.g., through additional measurements or sophisticated gate drivers.

One of the most common choices to achieve higher blocking capabilities is the use of multilevel topologies, such as the neutral-point-clamped converter [15] or FCC [16], or others [17]. In these systems, additional components combined with special modulation patterns assure safe voltages across the transistors. However, the extra parts, such as the flying capacitors in FCCs, are substantial in volume. Furthermore, the control of such systems is also complicated.

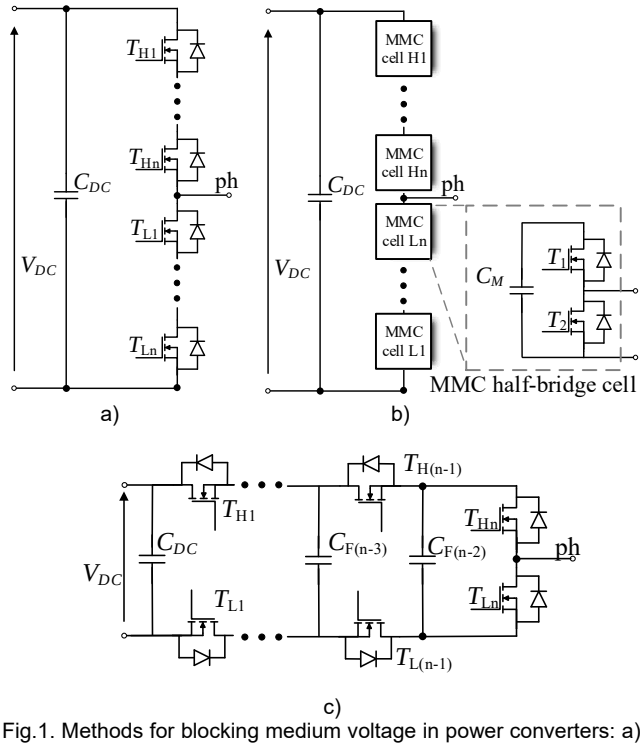


Fig.1. Methods for blocking medium voltage in power converters: a) direct series connection of transistors, b) modular multilevel converter (MMC) topology, c) flying capacitor (FC) topology.

Another often-considered approach is the MMC [18]. This method is akin to the basic multilevel converters but has some important differences. Similarly, as in the

previous systems, there are supplementary components that help to balance the voltages. However, in general, there are many more items – for example, considering the simplest half-bridge cell depicted in Fig. 1b, there are twice the transistors compared to the FCC assuming the same number of levels. On the other hand, in an MMC, each cell is identical, while in FCC, the voltages of the flying capacitors vary substantially. Hence, the modularity aspect of an MMC is a welcome addition reliability-wise, and thus these systems are frequently used in high-voltage systems, which have to operate dependably.

Quasi-two-level (Q2L) method was proposed as an alternative control method for MMC [19], which can substantially lower the cell capacitance requirement for the modules, which often was the source of a high volume of the systems. However, it can also be used in a simplified form, also in the FCC topology [20-22], just to balance the voltages across the capacitors and essentially be an alternative method for direct series connection. To this end, a universal method for applying the Q2L method is presented in this paper and validated experimentally up to 1.5 kV on a simple half-bridge circuit with inductive load, as well as using a specific application of a dc-dc non-isolated converter.

The paper is constructed as follows. After the brief introduction showcasing the state-of-the-art method for the construction of medium voltage converters, the second section describes the quasi-two-level method more thoroughly, focusing on the voltage balancing control aspect. Then, in the next section, a generalized case with a half-bridge circuit is studied. Further, in section four, a specific system is considered and validated experimentally for Q2L operation – a medium voltage dc-dc converter. Finally, the paper is concluded in the last section.

Quasi-two-level method

As mentioned before, Q2L method has been introduced as an alternative control method for MMCs, which can considerably lower the cell capacitance requirement [19, 23]. It can also be similarly applied to FCCs [24]. In this approach, the time in which each cell conveys the current is lowered drastically, which is depicted in Fig. 2. As can be seen, in a conventional MMC system, each cell can be inserted for up to $T_{i\_MMC}=(n-1)T_s/n$, where n is the number of cells/transistors in stack, and T_S is the switching period, creating the characteristic stepped voltage shape across the whole period (Fig. 2a). Thus, assuming dc-fed system, the capacitance must be substantial, so that it can deliver enough current without a voltage drop which could lead to dangerous situation for other cells. On the other hand, in the conventional Q2L approach, this stepped transition time is vastly lowered to $T_{i\_Q2L}=(n-1)T_{step}$, where T_{step} is minimally higher than the dead time, just to ensure reduced *dv/dt* ratio and balance the capacitor voltages – see Fig. 2b. Thus, the capacitances can be drastically lowered according to the equation below [24]

$$C_M = \frac{I_{tr}(n-1)T_i}{\Delta V}, \tag{1}$$

where C_M is the cell/flying capacitance, I_{tr} is the transition peak current, ΔV is the maximum allowable voltage ripple across the capacitors, and T_i is the insert time when the cell/transistor is active. Considering an exemplary system with 10 kHz switching frequency and 7 cells with 3.3 kV SiC MOSFETs, the insert time can be lowered from nearly 90 us to roughly 3 us, which can lead to reducing the stored energy in the capacitors for Q2L operation to 0.5% of the MMC equivalent [19].

Furthermore, when MMC systems are considered, the arm inductances are also vastly minimized when Q2L is applied, and the problem of circulating currents is also nearly entirely eliminated [24]. On the other hand, the effective output voltage of the Q2L-controlled system is essentially 2-level; thus, the ability to flexibly shape the current is lowered, and higher output inductance is required [19].

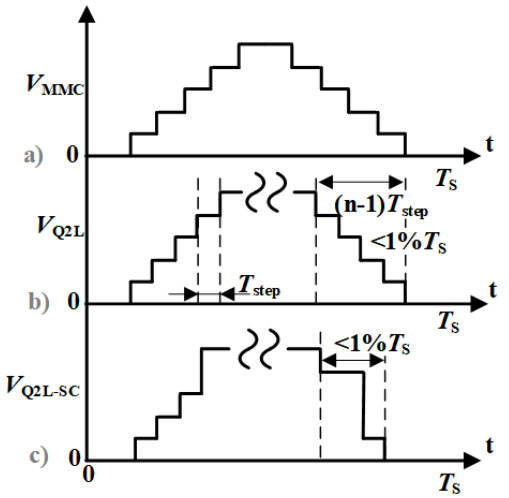


Fig. 2. Idealized voltages (phase to minus) for a) MMC/multilevel operation, b) conventional Q2L operation, c) Q2L applied as series-connection method.

However, the capacitance requirement can be lowered even further when the *dv/dt* aspect is left out, and the transitions are exclusively used just to balance the voltages across the transistors, as depicted in Fig. 2c [20, 22]. In this case, in an ideal situation, when no imbalance across the transistors occurs, the transition times are zero, and the system operates identically as a two-level series-connection-based system would behave. Of course, such a situation is not often seen, if ever – therefore, in practice, the transition time changes depending on the voltage error and thus are different in each transition. Nevertheless, since not all cells are inserted at each transition but only those that require balancing, the cell capacitance requirement is still lower than the conventional Q2L approach. On the other hand, since the transition time and order varies depending on the voltage balancing process, the *dv/dt* is not uniform, and thus this approach may not be perfect for common high voltage MMC applications, e.g., HVDC systems. However, for the lower spectrum MV applications that are considered further in the paper, it is not an issue. Furthermore, this simplified Q2L control should be rather compared with other methods to balance the voltages across series connected transistors, and not multilevel approaches, as it is characterized by same two-level output voltages deciding on the operation of the whole converter.

All in all, the simplified approach to use Q2L for series-connection of SiC MOSFETs is actually a very straightforward method, highly competitive against solutions for active voltage balancing, as it induces no additional power losses [8], requires less measurements compared to other approaches [8], and does not require any modifications in the gate drivers [13], nor high-speed control circuits for active delaying the signals [12].

Voltage balancing control loop

As mentioned, in the simplified Q2L approach for series connection, voltage balancing is the sole purpose of the Q2L operation. Thus, a balancing closed loop based on the voltage measurements across the capacitors needs to be formulated. Fig. 3 depicts a generalized control scheme for one Q2L-controlled leg. For the rest of the paper, FC topology is considered, as it contains fewer switches

compared to MMCs, and is more suitable for the lower spectrum of MV, taken into account further in the experimental study. However, the voltage control loop would be analogous to the MMC, and thus the scheme in Fig. 3 can be considered a general strategy for systems with Q2L applied as a series-connection method.

In general, in FC converters, there are states which affect the status of the flying capacitor – see Table 1. Considering the simplest case of a half-bridge circuit shown in Fig. 4a, the flying capacitor can be either charged or discharged in the middle state, depending on the current sign and the switching signals. When the current $i_L > 0$, during F1 and F2, the flying capacitor is charged and discharged, respectively. On the other hand, when $i_L < 0$, the situation is reversed; F1 discharges the capacitor, while F2 adds charge. Thus, for certain applications where the output current changes its sign, e.g., inverters, the current has to be measured and used as an input for the state machine. Furthermore, the reference DC voltage has to be measured, as well as the voltage at each individual flying capacitor. The voltage error is used for a PI controller to determine the insertion time (length of states F) T_i.

Table 1. Basic states of a three-level FC leg when $V_{FC}=V_{DC}/2$

State	T_{H1}	T_{H2}	T_{L1}	T_{L2}	v_{ph} (half-bridge)	v_{ph} (dc-dc)
1	1	1	0	0	$+V_{DC}/2$	V_{DC}
0	0	0	1	1	$-V_{DC}/2$	0
F1	1	0	1	0	$V_{DC}/2$	$V_{DC}/2$
F2	0	1	0	1	$V_{DC}/2$	$V_{DC}/2$

The scheme presented in Fig. 3 is shown for a three-level system investigated further in the experimental study. However, for a converter with more states, such a control loop must be used for each flying capacitor. The only change is the ratio by which the DC voltage is divided to create the reference value for the flying capacitor voltage.

Case study 1 – medium voltage half-bridge leg with an inductive load

At first, let us consider a general case with a half-bridge circuit with an inductive load, where the current flows in both directions, similar to common inverter applications. The parameters of the system are depicted in Table 2, while the scheme and a photograph of the are showcased in Fig. 4. In this setup, a simple square-wave control leads to a triangular shaped inductor current, where the Q2L transition occurs at both positive and negative current. This experimental realization allows for operation without much effort from the DC source, as only the losses in the system are supplied.

Table 2. Parameters of the half-bridge system

DC voltage	1500 V
Load switched current	300 A
Switching frequency	12.8 kHz
Load inductor	2 x 110 µH
DC capacitance	10 x 150 µF
Flying capacitance	820 nF (C0G)
Power transistors	2 x CAB450M12XM3/ 1200 V, 2.6 mΩ

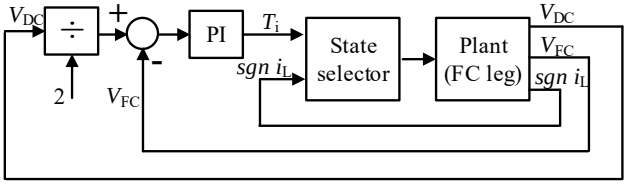
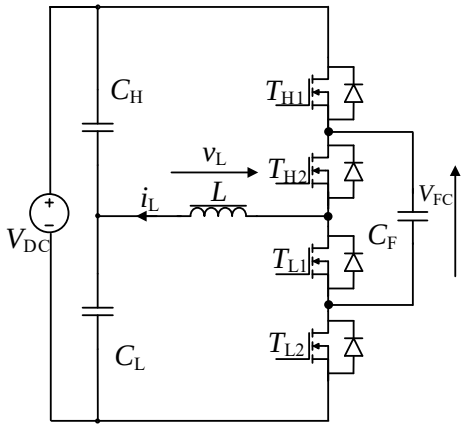


Fig. 3. Generalized voltage balancing control scheme for one Q2L-controlled flying capacitor leg – a three-level example.

a)



b)

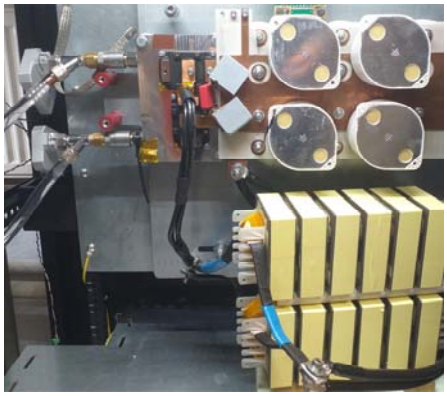
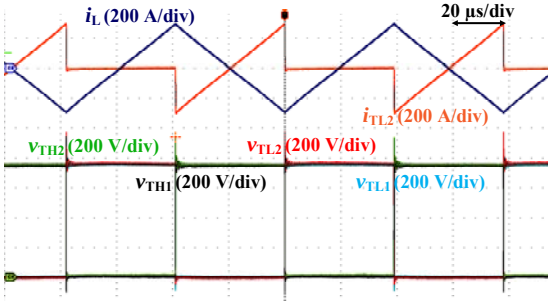


Fig. 4. Experimental system for the medium voltage half-bridge leg with an inductive load controlled with the Q2L method: a) schematic, and b) photograph.

a)



b)

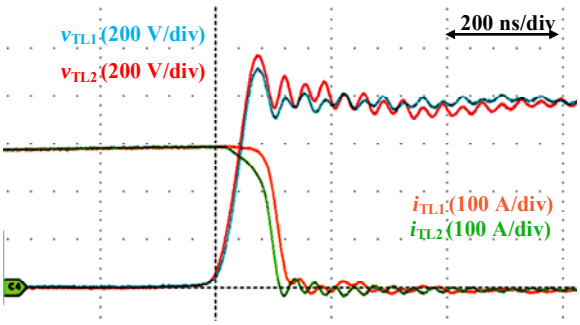


Fig. 5. Experimental results for half-bridge circuit operated with Q2L control according to the parameters in Table 2: a) general view, b) zoomed view at turn-off.

SiC MOSFET power modules from Wolfspeed are used as the switches (CAB450M12XM3). The switching frequency of the system is established at 12.8 kHz, a typical range for power converters with SiC MOSFETs rated at several hundreds of kW, which would exhibit similar conditions are tested in this system. The mentioned

frequency, along with the inductance of 55 µH (two 110 µH inductors in parallel), allows to reach roughly 300 A of switched current. Five 150 µF DC-link capacitors from Ducati per half of the DC-link are applied to achieve a stable DC voltage. Since the expected inserted time is very low, the flying capacitance C_F can be minimal – here, 820 nF is built from small SMD C0G capacitors in a series-parallel connection. Furthermore, additional measurements for the DC and flying capacitor voltages are required. However, since the voltage is constant, it is not a challenging aspect. Considering the notable size of other passive components and the power modules, the whole impact of the additional components required for the Q2L operation on the total volume is negligible.

Exemplary experimental results for a test performed at 1.5 kV are depicted in Fig. 5. As can be seen, the inductor current is triangular, and the transistors are soft-switched at peak negative current and hard-switched at peak positive current (I_L ~= 300 A peak). Most importantly, the voltage across the transistor is nearly perfectly balanced due to the use of the active control depicted in Fig. 3, with the inserted times in the range of tens of ns, which is a negligible value compared to the total switching period T_S=78 µs. The system behaves as anticipated – identically to the series-connected circuits or two-level equivalents using single high-voltage transistors, with no supplementary power losses [8].

Case study 2 – medium voltage non-isolated dc-dc converter

The second considered circuit for the validation of the Q2L method applied to balance the voltage across the series-connected SiC MOSFETs is a bidirectional, non-isolated soft-switching converter [21, 22, 25], also designed for 1.5 kV DC voltage. The core parameters of the system are showcased in Table 3, while the scheme and the photo of the converter are depicted in Fig. 6. The system is essentially based on the same FC leg as in the half-bridge system, and the same states shown in Table 1 are valid, with the difference in the phase voltages, as here there is no middle point in the DC-link. In this case, the phase terminal is connected to the inductor responsible for buck/boost operation, which further feeds the output capacitor connected between the inductor and the minus point of the FC leg.

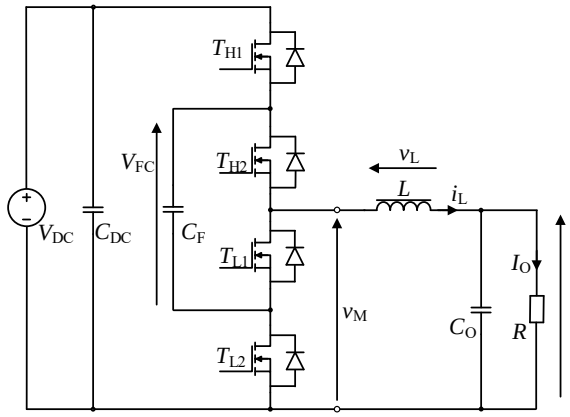
Table 3. Parameters of the dc-dc converter

DC voltage	1500 V
Switching frequency	40 ÷ 260 kHz
Inductor	30 µH
DC input/output capacitance	6 µF
Flying capacitance	330 nF
Power transistors	2 x FF11MR12W1M1_B11 1.2 kV and 11 mΩ

In this system, the switching frequency is notable due to soft-switching behavior, and varies depending on the load, with the peak at 260 kHz [22]. Therefore, the rest of the passive components are relatively small: the inductance is 30 µH, and the DC capacitors are 6 µF for both the input and output of the converter. Finally, the flying capacitor is minuscule – 330 nF capacitance is enough to provide minimal ripples. Again, measurements of DC and FC voltages are employed to provide proper signals for the closed-loop voltage control.

For FC-based dc-dc converters, either continuous conduction mode (CCM), discontinuous conduction mode (DCM), or critical conduction mode (CRM) is employed, and the inductor current can be either always positive or have a specified switched current value, that is known arbitrarily. This is the case for the considered dc-dc converter, which operates in near-CRM mode, with the current being always negative at turn-on and always positive at turn-off. Thus, the current measurement is not required for the Q2L voltage balancing control loop, simplifying the scheme depicted in Fig. 3 even further.

a)



b)

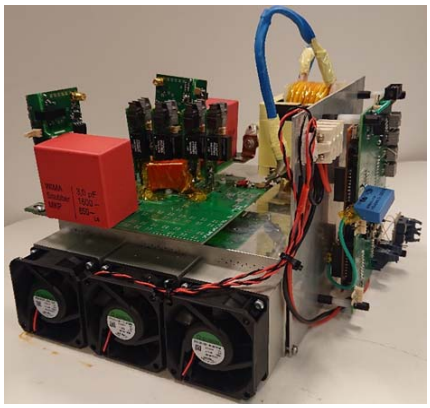
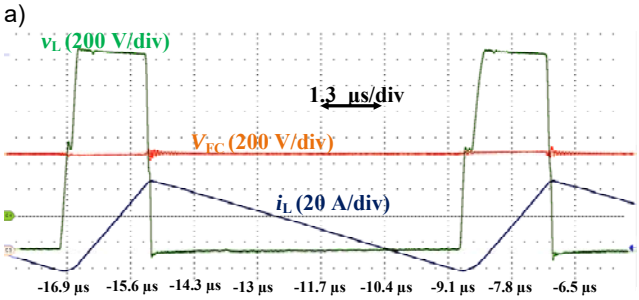


Fig. 6. Experimental system for the medium voltage non-isolated, soft-switched dc-dc converter employing Q2L control for voltage balancing: a) schematic, and b) photograph.

a)



b)

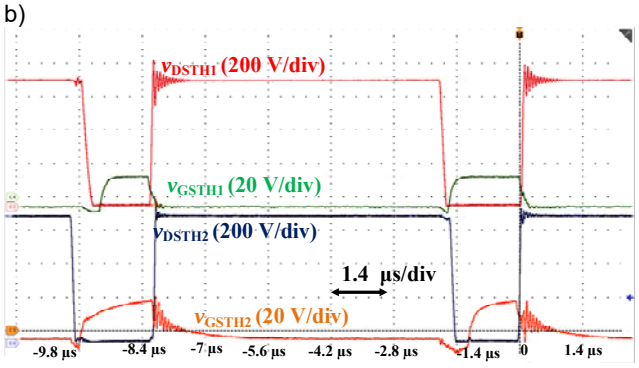


Fig. 7 Exemplary experimental results of the dc-dc converter: a) general view, and top transistor pair view (b). From the top: inductor voltage (v_L) and current (i_L); flying capacitor voltage (V_{FC}); gate-source voltages of top-side transistors (v_{GSTH1}, v_{GSTH2}); transistor drain-source voltages (v_{DSTH1}, v_{DSTH2}) of top-side switches.

Exemplary waveforms, for the dc-dc converter operating at 1.5 kV, voltage gain of 0.2, with a load resistance of 17.2 Ω, 5.5 kW power at 122 kHz switching frequency is depicted in Fig. 7. As can be seen, the voltage of the flying capacitor is very stable, with minimal voltage ripples below 5% of the nominal voltage ($V_{DC}/2$). Furthermore, observing the voltage across the inductor, a characteristic Q2L shape with the middle state being used briefly during the transitions can be seen. In this experiment, the inserted time was equal to roughly 45 ns. Inductor current i_L achieved approximately 27 A RMS value with peak-to-peak current at 70 A. Additionally, in Fig 7b, the voltages across the top-pair transistors can be observed. The drain-source voltage follows the balanced value of the flying capacitor, and thus the MOSFETs operate in a safe range. Moreover, soft-switching behavior can also be seen. Altogether, the Q2L control assures proper voltage sharing across the transistors, does not induce much realization effort, and does not introduce extra losses – the considered dc-dc converter prototype reaches 99.5% peak efficiency [25].

Conclusion

This paper presents the simplified quasi-two-level method as a universal approach for voltage balancing of series-connected SiC MOSFETs, especially considering state-of-the-art medium voltage power electronics applications. It is shown that the control allows for low-effort voltage balancing of series-connected fast-switching transistors without a notable increase in volume and no supplementary power losses. The concept is experimentally validated using two different systems operating at notable currents and voltages up to 1.5 kV: a half-bridge circuit with an inductive load and a dc-dc converter. Overall, the Q2L method applied for series connection can be effectively and competitively employed against other state-of-the-art approaches for active voltage balancing and conventional two-level systems.

***Author**: Rafał Kopacz, MSc., Warsaw University of Technology, Institute of Control and Industrial Electronics, Koszykowa 75, 00-662 Warsaw, E-mail: rafal.kopacz@pw.edu.pl.*

REFERENCES

[1] X. She, A. Q. Huang, L. Ó, and B. Ozpineci, “Review of Silicon Carbide Power Devices and Their Applications,” IEEE Transactions on Industrial Electronics, vol. 64, no. 10, pp. 8193-8205, 2017.

[2] G. Iannaccone, C. Sbrana, I. Morelli, and S. Strangio, “Power Electronics Based on Wide-Bandgap Semiconductors: Opportunities and Challenges,” IEEE Access, vol. 9, pp. 139446-139456, 2021.

[3] L. Zhang, X. Yuan, X. Wu, C. Shi, J. Zhang, and Y. Zhang, “Performance Evaluation of High-Power SiC MOSFET Modules in Comparison to Si IGBT Modules,” IEEE Transactions on Power Electronics, vol. 34, no. 2, pp. 1181-1196, 2019.

[4] D. Zięba, J. Rąbkowski, „Dynamic performance evaluation of ultra-fast SiC MOSFET power module – a comprehensive approach“, vol. 5, Przegląd Elektrotechniczny, 2023.

[5] A. Marzoughi, J. Wang, R. Burgos, and D. Boroyevich, “Characterization and Evaluation of the State-of-the-Art 3.3-kV 400-A SiC MOSFETs,” IEEE Transactions on Industrial Electronics, vol. 64, no. 10, pp. 8247-8257, 2017.

[6] L. Wang, Q. Zhu, W. Yu, and A. Q. Huang, “A Medium-Voltage Medium-Frequency Isolated DC–DC Converter Based on 15-kV SiC MOSFETs,” IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 1, pp. 100-109, 2017.

[7] D. Rothmund, T. Guillod, D. Bortis and J. W. Kolar, "99.1% Efficient 10 kV SiC-Based Medium-Voltage ZVS Bidirectional Single-Phase PFC AC/DC Stage," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 7, no. 2, pp. 779-797, June 2019.

[8] P. Trochimiuk, R. Kopacz, K. Frąc and J. Rąbkowski, "Medium Voltage Power Switch in Silicon Carbide—A Comparative Study," in IEEE Access, vol. 10, pp. 26849-26858, 2022.

[9] S. Zhao, X. Zhao, Y. Wei, Y. Zhao, and H. A. Mantooth, “A Review of Switching Slew Rate Control for Silicon Carbide Devices Using Active Gate Drivers,” IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 9, no. 4, pp. 4096-4114, 2021.

[10] R. Kopacz, D. Peftitsis and J. Rabkowski, "Experimental study on fast-switching series-connected SiC MOSFETs," 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe), Warsaw, Poland, 2017, pp. P.1-P.10.

[11] P. Trochimiuk, R. Kopacz, G. Wrona and J. Rąbkowski, "Medium voltage power switch based on 1.7 kV SiC MOSFETs connected in series inside power modules," 2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe), Genova, Italy, 2019, pp. P.1-P.10.

[12] P. Trochimiuk, R. Kopacz, G. Wrona, and J. Rąbkowski, “Active Voltage Balancing of Series-Connected 1.7 kV/325 A SiC MOSFETs Enabling Continuous Operation at Medium Voltage,” IEEE Access, vol. 9, pp. 8604-8614, 2021.

[13] A. Marzoughi, R. Burgos, and D. Boroyevich, “Active Gate-Driver With dv/dt Controller for Dynamic Voltage Balancing in Series-Connected SiC MOSFETs,” IEEE Transactions on Industrial Electronics, vol. 66, no. 4, pp. 2488-2498, 2019.

[14] X. Lin, L. Ravi, R. Burgos, and D. Dong, “Hybrid Voltage Balancing Approach for Series-Connected SiC MOSFETs for DC-AC Medium-Voltage Power Conversion Applications,” IEEE Transactions on Power Electronics, pp. 1-1, 2022.

[15] A. Nabae, I. Takahashi, and H. Akagi, “A new neutral-point-clamped PWM inverter,” IEEE Trans. Ind. Applicat., vol. IA-17, no. 5, pp. 518-523, Sep./Oct. 1981

[16] T. A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," PESC '92 Record. 23rd Annual IEEE Power Electronics Specialists Conference, Toledo, Spain, 1992, pp. 397-403 vol.1, doi: 10.1109/PESC.1992.254717.

[17] R. Kopacz, M. Harasimczuk, R. Sobieski, and J. Rąbkowski, "Three-Level Interleaved Non-isolated DC/DC Converter as a Battery Interface in an EV Charging System with Bipolar DC-Link," vol. 5, Przegląd Elektrotechniczny, 2023.

[18] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard and P. Barbosa, "Operation, Control, and Applications of the Modular Multilevel Converter: A Review," in IEEE Transactions on Power Electronics, vol. 30, no. 1, pp. 37-53, Jan. 2015.

[19] I.A, Gowaid, et al., „Analysis and design of a modular multilevel converter with trapezoidal modulation for medium and high voltage DC-DC transformers“, IEEE Transactions on Power Electronics 30(10), 5439–5457, 2015.

[20] M. Schweizer and T. B. Soeiro, "Heatsink-less Quasi 3-level flying capacitor inverter based on low voltage SMD MOSFETs," 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe), Warsaw, Poland, 2017, pp. P1-P.10 Heatsink-less Quasi 3-level flying capacitor inverter based on low voltage SMD MOSFETs." pp. P1-P.10.

[21] R. Kopacz, P. Trochimiuk, G. Wrona and J. Rąbkowski, "High-Frequency SiC-Based Medium Voltage Quasi-2-Level Flying Capacitor DC/DC Converter With Zero Voltage Switching," 2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe), Lyon, France, 2020, pp. P.1-P.10

[22] R. Kopacz, M. Harasimczuk, P. Trochimiuk, G. Wrona and J. Rąbkowski, "Medium Voltage Flying Capacitor DC–DC Converter With High-Frequency TCM-Q2L Control," in IEEE Transactions on Power Electronics, vol. 37, no. 4, pp. 4233-4248, April 2022.

[23] S. Milovanovic, D. Dujic, „Comprehensive analysis and design of a quasi two-level converter leg“, CPSS Transactions on Power Electronics and Applications 4(3), 181–196, 2019.

[24] S.C. Mersche, R. Schwendemann, M. Hiller, „Validation of the quasi-two-level operation for a flying capacitor converter in medium-voltage applications“, Energies 16(6), 2797, 2023.

[25] R. Kopacz, M. Harasimczuk, P. Trochimiuk and J. Rąbkowski, "Investigation of Soft-Switching QSW Technique in DC/DC SiC-Based Flying Capacitor Converter With Q2L Control," in IEEE Transactions on Industrial Electronics, vol. 70, no. 9, pp. 9035-9045, Sept. 2023.