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Dynamic performance evaluation of ultra-fast SiC MOSFET power module – a comprehensive approach

***Abstract**. The article describes a comprehensive approach to dynamic performance determination tests of SiC MOSFET power modules. Experimental verification was performed using ultra-fast switching (1,2 kV, 495 A) module from Microsemi. The obtained results are compared to results acquired by measurements performed with compliance to a commonly-used standard that does not consider phenomena that significantly impact switching processes of fast-switching SiC MOSFET power modules.*

***Streszczenie.** W artykule przedstawiono metodykę badań parametrów dynamicznych modułów tranzystorowych nowej generacji bazujących na tranzystorach MOSFET z węglika krzemu (SiC). Przeprowadzono badania eksperymentalne dla bardzo szybko przełączającego modułu tranzystorowego firmy Microsemi (1,2 kV, 495 A). Otrzymane wyniki porównano z wynikami uzyskanymi na podstawie powszechnie wykorzystywanego standardu wyznaczania parametrów dynamicznych tranzystorów MOSFET, który nie uwzględnia szeregu zjawisk znacząco wpływających na procesy łączeniowe szybko przełączających tranzystorów SiC MOSFET. (**Kompleksowe podejście do badań parametrów dynamicznych szybko przełączających modułów tranzystorowych SiC MOSFET**).*

Keywords: SiC MOSFET, fast-switching, power modules, dynamic performances.
Słowa kluczowe: SiC MOSFET, szybko przełączające, moduły tranzystorowe, parametry dynamiczne.

Introduction

In recent years, Silicon Carbide (SiC) semiconductors have already become widely acknowledged successors of silicon-based semiconductors in many application areas. SiC MOSFETs successively establish their position as a top-performance choice for power electronics converters like photovoltaic inverters, traction battery chargers, high-power auxiliary power supplies, or traction inverters dedicated to the railway, electric buses, and electric cars, including Formula E [1-9]. SiC MOSFETs application enables elevated switching frequencies while offering low conduction losses. As an effect, SiC-based power electronics converters often exhibit efficiencies and power densities unreachable with devices based on silicon (Si) semiconductors. However, as new-generation SiC MOSFETs can switch load currents of hundreds of amps in times of the order of tens of nanoseconds, new challenges related to accurate measurements and identification of parameters spring up [10]. Preparation of a sophisticated testbench with minimized parasitic inductances and exact measuring rig setup has become challenging like never before and has a tremendous impact on the accuracy of the obtained results [11]. Time alignment is a crucial issue in the case of high-bandwidth measurement equipment and precise probes. Moreover, the commonly-used methods of determining dynamic performance, i.e. based on the IEC 60747-8 standard, do not consider phenomena that significantly impact switching processes [12,13]. Thus, the results obtained may be affected by significant errors. Highly efficient gate drivers also play an increasingly important role as high current capabilities combined with rapid rise/fall times are needed to fully use the dynamic performance potential of fast-switching SiC MOSFET power modules. With a low output resistance gate driver, these transistor sets can switch nominal currents of hundreds of amps with little or even without external gate resistance, with voltage slope steepness exceeding 50 kV/µs. Thus, lower switching energies are achieved, increasing the efficiencies of power converters. Considering it all, data provided by SiC MOSFET power module manufacturers in datasheets often might be insufficient or inaccurate. Additional experiments are needed to characterize and model the actual behaviour of the device properly.

This paper describes a comprehensive approach to dynamic tests of fast-switching SiC MOSFET modules. A new-generation Microsemi MSCSM120AM042CT6LIAG 1200 V, 495 A SiC MOSFET power module with very low internal parasitic inductance of 3 nH [14] and rapid switching capabilities was tested using the widely-used double-pulse test (DPT) technique. The experimental results are presented and discussed, including a comparison of the proposed approach to the standards.

Parasitic parameters of SiC MOSFET power modules and their impact on rapid switching processes

In SiC MOSFETs, power losses primarily relate to the resistive nature of the channels while conducting current. In the case of an idealized transistor (without parasitic inductances, capacitances, and internal connections resistances), the instantaneous losses can be expressed as the product of the drain-source voltage and the drain current. However, an actual MOSFET is far from an idealized one. At first, the device internal structure exhibits capacitances between all three electrodes, which tend to be strongly non-linear and dependent on the voltage [15]. Power modules often are based on multiple semiconductor chips connected in parallel, and, in effect, the resulting parasitic capacitances become substantial. Such additional capacitances in the power module structure, in the case of fast-switching SiC MOSFETs, cause a significant capacitive current flow during rapid switching processes [10]. Unfortunately, this affects the actual loss measurements. At the turn-on process, a sum of anti-parallel SiC diode junction capacitance and the parasitic output capacitance of the MOSFET discharges through the channel, increasing the actual turn-on switching energy [16].

What is more, the parasitic capacitances of the opposite diode and MOSFET are being charged, and the charging current flows through the MOSFET channel that is turning on, further increasing its switching energy.

Furthermore, all power module external connection terminals, internal connections between chips and copper traces (bonding wires or copper clips) exhibit parasitic inductances and resistances. During switching processes, these inductances make the dynamic performance determination process even more complex. The reason is the voltage measured across the module differs from the actual voltage across the chips generally, not to mention accurate voltages across particular chips considering all internal connections and asymmetries inside the power

module. These voltage differences are caused by the voltages induced on parasitic inductances. The complex internal coupling of magnetic fields inside the power modules also substantially affects actual voltage values across particular chips. It is very challenging to precisely measure and derive the model of a complex multi-chip internal structure of a power module under test, and it requires advanced measurement equipment like Vector Network Analyzer with dedicated fixtures. A different approach may be applied in order to estimate the actual voltages across the chips with parasitic inductances taken into account.

Nowadays, manufacturers of the most recent SiC MOSFET power modules often provide information about the parasitic inductance of the main current route across the power module, according to IEC 60747-15:2012 standard, section 5.3.2 in datasheets [17]. The Microsemi MSCSM120AM042CT6LIAG SiC MOSFET power module under test features a very low internal parasitic inductance of 3 nH only. Taking into account results obtained by Wang et al. in [18], a reasonable assumption is that the internal structure of the module with that low parasitic inductance has to be highly symmetrical and with a magnetic field cancellation layout. In this case, the value of parasitic inductance of the main current route provided by the manufacturer can be divided by half and used for further calculation. However, this approach may lead to meaningful errors in power modules with highly nonsymmetrical layouts. All in all, measurements of the parasitic inductances are preferred to obtain accurate results.

What also becomes a challenge to estimate is the actual gate-source voltage of the SiC MOSFET under test. To achieve fast switching processes, external gate resistors are minimized. As a result, a voltage divider between the gate driver output and the gate electrode in the transistor is formed with the major voltage drop over the internal resistance of the gate electrode itself. The gate-source voltage measured with a probe on the power module connection points is far different than the actual on-chip gate-source voltage. In addition, during the switching transitions, the on-chip gate-source voltage is affected by a reverse transfer capacitance of a transistor (a highly non-linear voltage-dependent parasitic capacitance between the drain and the gate electrodes). As the SiC MOSFETs gates input capacitances are relatively low, it significantly increases the complexity of the actual gate-source voltage estimation process and behavioural modeling of SiC MOSFET power modules. All things considered, the simplified schematic of the power loop of the double-pulse test testbench, including the most significant parasitic inductances, parasitic capacitances, and the resistances of cables, busbars, and internal connections in the power module under test, has been presented in figure 1.

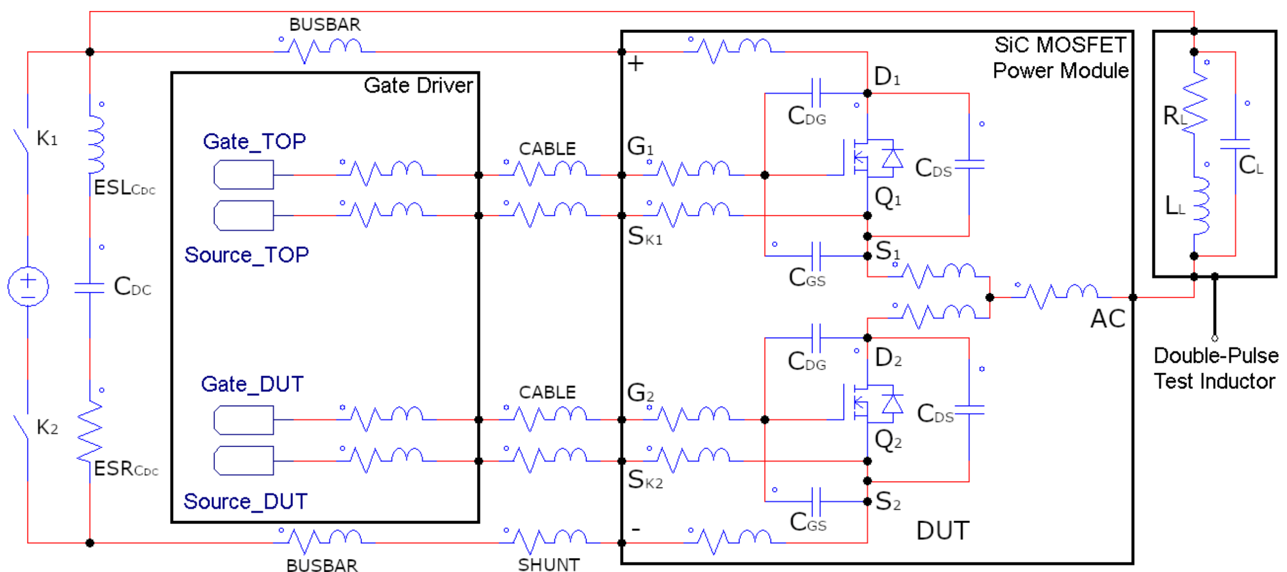

Fig.1. The simplified schematic of the double-pulse test testbench power loop including parasitic parameters

Switching-related high-frequency oscillations and their impact on switching energies

As the transistors switching speeds increase, so is the steepness of the voltage and current waveforms slopes. Steep slopes trigger post-switching high-frequency oscillations in the power loop with significant amplitudes. The commonly-used method of switching energy determination process described in the IEC 60747-8 standard does not mention the oscillation phase. It also does not define whether the 10% transits of the maximum amplitude of the current waveform should be the first 10% transit or the last 10% transit of the waveform as the transistor switches. In effect, the standard may be interpreted in two ways leading to different results [19]. What is more, with parasitic inductances and capacitances minimized both in the power loop and the power module itself, oscillations often appear in the frequencies of dozens of megahertz. As recent best-in-class flexible Rogowski coils exhibit limited bandwidth to 50 MHz, high oscillations frequencies make it challenging to estimate additional power losses precisely due to high-frequency phase shifts. On the other hand, coaxial shunt resistors do not entirely solve the problem, as inserting it into the power loop significantly affects the overall parasitic inductance. It changes its resonant frequency and affects the switching waveforms substantially (increasing the turn-off switching energy and lowering the turn-on switching energy). In the case of fast-switching SiC MOSFET power modules, the question arises whether these oscillations significantly affect the actual switching losses or not. Occurring oscillations decay with time due to damping caused by resistances of connections in the power module under test and the whole power loop. Based on the oscillation decay time, an equivalent resonant circuit may be derived [20]. Thus, the equivalent resistance of the resonant circuit can be used to estimate the additional losses in the oscillation phase. However, these additional losses are dissipated not only in the power module but also in the whole power loop,

so the presence of a coaxial shunt resistor will affect the damping factor substantially and has to be taken into consideration.

Dynamic performance determination of a fast-switching SiC MOSFET power module

In order to determine the dynamic performance of the fast-switching SiC MOSFET power module, a sophisticated double-pulse test testbench (fig.2) has been prepared based on the Advanced Conversion 700D590 power ring film capacitor. The Microsemi MSCSM120AM042CT6LIAG 1200 V, 495 A SiC MOSFET power module was connected with laminated busbars designed in such a way that it is possible to insert a coaxial shunt resistor into the power loop. The coaxial shunt resistor (Powertek SDN-414-10 with 2 GHz bandwidth) was mechanically modified in order to minimize additional parasitic inductance inserted into the power loop. This resulted in the total power loop parasitic inductance of 17,7 nH without the coaxial shunt resistor installed in the power loop and 25,7 nH when it is inserted. As a load inductance, a custom-made air core 50 μH inductor characterized by a relatively low parasitic capacitance (80 pF) was applied. A modified high-performance low output impedance gate driver from MEDCOM company has been used to drive MOSFET gates with voltages equal to +20/-5 V, as recommended by the manufacturer. No additional external gate resistor was inserted into the gate loop to achieve the fastest switching possible (R_G = 0 Ω). A connection between the gate driver output and the MOSFET under test gate and source connection terminals was made using a short high bandwidth coaxial cable in order to minimize parasitic inductance in the gate loop. For the gate-source voltage measurements, an optically isolated voltage probe Tektronix TIVH02L was used. That probe is characterized by a high common-mode rejection ratio (CMRR) for high-frequency oscillations. High CMRR is crucial for accurate measurements of low voltage signals during rapid-switching processes with multi-megahertz oscillations propagating in the power loop and radiating out of it. The on-chip gate-source voltage has been estimated based on the gate current measurement as a voltage drop over gate driver output resistance. Tektronix THDP0200 differential voltage probes have been used for the drain-source voltage measurements. For the MOSFET current measurements, a PEM CWT Ultra Mini 30 MHz Rogowski coil current probe was applied along with the modified Powertek SDN-414-10 coaxial shunt resistor. To ensure repeatability and accuracy of current measurements, a dedicated 3D-printed plastic coil formers have been manufactured to keep the conductor central in the Rogowski coil loop. All voltage and current probes output signals were precisely time-aligned using a method described in [10]. It enabled time alignment as precise as 320 ps, which corresponds to 3,125 GS/s sampling in a Tektronix MSO46 oscilloscope used. As the power module under test is the 1200 V class device, an operating point with the power supply voltage equal to 600 V was chosen. Selected turn-on and turn-off waveforms from the 400 A switching DPT showing a comparison of obtained SiC MOSFET under test source current waveforms with the usage of Rogowski coil current probe and modified coaxial shunt resistor are presented in figure 3 and figure 4. The comparison of measured current waveforms shows that the main slopes for both turn-on and turn-off processes are similar. Thus, both methods can be used for switching energy determination in compliance with the IEC 60747-8 standard. However, the shape of the current waveform obtained by the Rogowski coil current probe is distorted, especially in the oscillation phase.

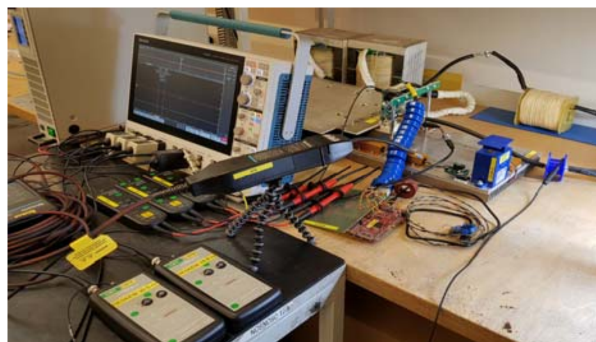

Fig.2. The double-pulse test testbench used for dynamic performance evaluation of ultra-fast SiC MOSFET power modules

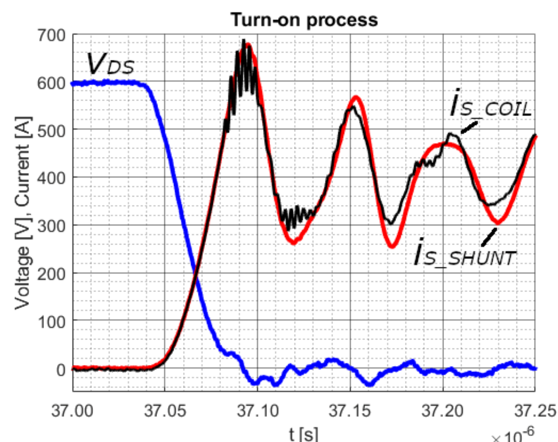

Fig.3. Selected turn-on waveforms of the drain-source voltage v_{DS} and the source current of the SiC MOSFET under test measured with the Rogowski coil current probe (i_{S_COIL}) and current shunt resistor (i_{S_SHUNT})

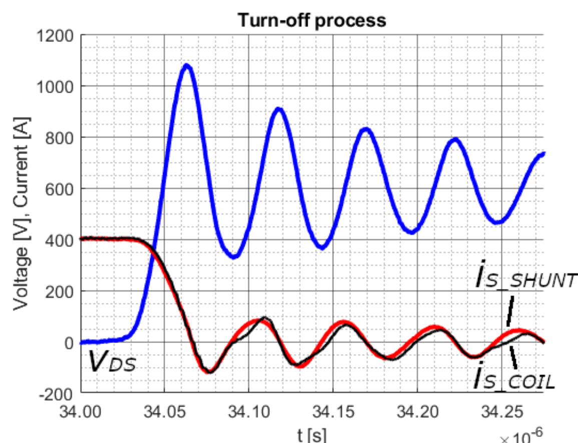

Fig.4. Selected turn-off waveforms of the drain-source voltage v_{DS} and the source current of the SiC MOSFET under test measured with the Rogowski coil current probe (i_{S_COIL}) and current shunt resistor (i_{S_SHUNT})

In addition, a phase shift can be observed. These deformations make it impossible to proceed with the next steps of the accurate dynamic performance determination of a fast-switching SiC MOSFET power module, so the current waveform obtained with the current shunt resistor is used as a reference. It is worth noticing that the drain-source voltage slope maximum steepness during the turn-off process exceeds 52,5 kV/μs. In the case of that fast switching processes, high electromagnetic interferences (EMI) radiation may occur. A high level of EMI may lead to high interferences while performing measurements with probes, so special care has to be taken in measurement rig

placement. Transmission line effects also have to be taken into consideration, and proper termination is essential. With correctly performed measurements and obtained waveforms, other phenomena must be considered. Looking at both turn-on and turn-off processes, the drain-source voltage measured across external power module terminals as the MOSFET turns on does not represent the actual on-chip drain-source voltage, as it is affected by additional internal parasitic inductances. Knowing the internal parasitic inductance of the power module under test and assuming its symmetrical internal structure, an actual on-chip drain-source voltage has been estimated based on the additional voltage drop over internal parasitic inductance during dynamic processes, as in equation 1.

$$v_{DS_CHIP}(t) = v_{DS}(t) - L_{S_SiC}\frac{di_S(t)}{dt} \quad (1)$$

where: v_{DS_CHIP} – estimated on-chip drain-source voltage, v_{DS} – drain-source voltage measured on power module terminals, L_{S_SiC} – parasitic inductance of internal connections of the transistor under test (Q_2), i_S – transistor under test source current measured with a current shunt resistor.

Comparisons of the measured drain-source voltage waveform and the estimated on-chip drain-source voltage have been presented in figure 5 for the turn-on process and in figure 6 for the turn-off process.

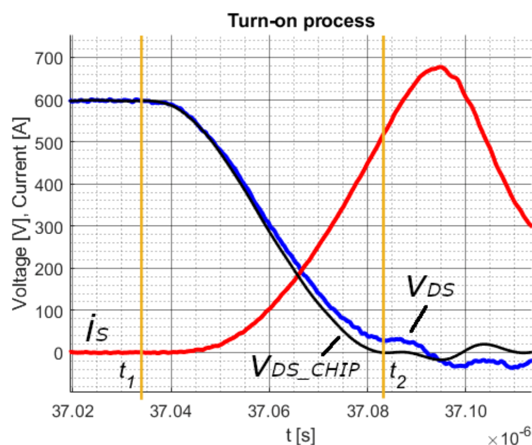

Fig.5. The comparison of the measured drain-source voltage waveform v_{DS} and the estimated on-chip drain-source voltage v_{DS_CHIP} during the turn-on process

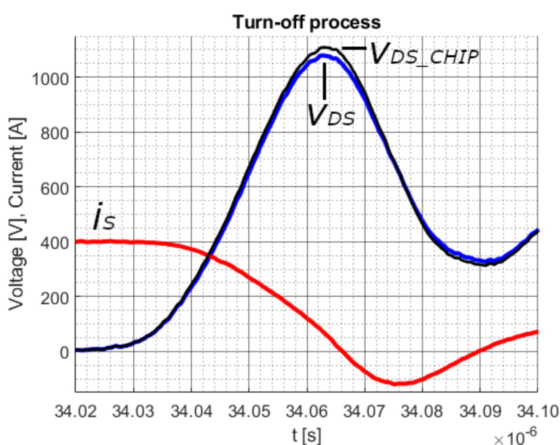

Fig.6. The comparison of the measured drain-source voltage waveform v_{DS} and the estimated on-chip drain-source voltage v_{DS_CHIP} during the turn-off process

Considering the power module under test, the difference is not significant as total parasitic inductance is very low (3 nH). However, in a case of a power module with a higher parasitic inductance value, not taking into account the actual on-chip drain-source voltage might lead to an incident in which its amplitude exceeds the drain-source voltage blocking capability. Then, it could lead to avalanche conduction mode, and possible permanent damage. Moreover, during the turn-on process, the charged parasitic output capacitance C_{OSS} discharges through the resistive MOSFET channel, increasing the actual turn-on energy. The problem is that phenomenon is not possible to measure with a probe outside the module, and the dissipated energy has to be estimated based on the energy stored in the nonlinear parasitic output capacitance or measured using calorimetric methods. That energy can be estimated on the basis of the characteristic of parasitic output capacitance as a function of drain-source voltage. The characteristic may be obtained by measurements or from the datasheet of the power module. Estimated energy stored in parasitic output capacitance can be expressed by equation 2.

$$E'_{OSS} = V_{DS}\int_0^{V_{DS_OFF}} C_{OSS}(v_{DS})dv_{DS} \quad (2)$$

where: E'_{OSS} – estimated energy stored in C_{OSS}, V_{DS_OFF} – constant drain-source voltage in the off state, C_{OSS} – a sum of parasitic capacitances between drain-gate and drain-source terminals.

Considering that precise measurements of individual parasitic capacitances were performed, a more accurate E_{OSS} estimation can be derived from equation 3.

$$E_{OSS} = V_{DS}\int_0^{V_{DS_OFF}} C_{DS}(v_{DS})dv_{DS} + V_{DG}\int_0^{V_{DG_OFF}} C_{DG}(v_{DG})dv_{DG} \quad (3)$$

where: E_{OSS} – estimated energy stored in C_{OSS}, C_{DS} – nonlinear parasitic capacitance between drain and source, V_{DG_OFF} – constant drain-gate voltage in the off state, C_{DG} – nonlinear parasitic capacitance between drain and gate, v_{DG}. – drain-gate voltage.

In the case of SiC MOSFET tested with the voltage up to 600 V, the estimated energy stored in C_{OSS} (E_{OSS}) was determined to be equal to 1,386 mJ. The resulting turn-on switching energies (E_{ON}) of the power module under test determined on the basis of the equation 4 for the 600 V operating point are presented in the figure 7.

$$E_{ON} = \int_{t_1}^{t_2} v_{DS_CHIP}(t)i_S(t)dt + E_{OSS} \quad (4)$$

Limits of integration t_1 and t_2 are shown in figure 5 as vertical lines. They were set in a way in relation to voltage and current waveforms that maximizes the instantaneous power losses integration period. This results in higher switching energies than in the case when the IEC 60747-8 standard rule for limits of integration would be applied. In the case of the turn-off process, the same attitude for limits of integration setting has been applied (t_3, t_4 in figure 9).
What should be emphasized is that in the case of tested power module, the actual turn-on energy for the operating

point of 600 V, 400 A, is over two times higher than the turn-on energy determined using the IEC 60747-8 standard. As the switching current becomes lower, that relation is further increased. It shows that not considering the E_{OSS} may lead to a severe underestimation of the turn-on energy of the fast-switching SiC MOSFET. During the turn-off process, the drain-source voltage rises, and the non-linear parasitic output capacitance C_{OSS} is charged, which means a current flows through it. The problem is the source current being measured outside the transistor by a current probe contains both channel current and capacitive current. As the capacitive current component does not flow through the resistive channel of the transistor, it should not be taken into account during the turn-off energy determination process. The capacitive current component has to be separated, and the MOSFET channel current has to be determined.

That can be done by subtracting the instantaneous values of the capacitive current component from the instantaneous values of measured source current of the MOSFET under test. The capacitive current component can be determined based on the C_{OSS} as a function of the drain-source voltage, as described in [10]. In effect, the MOSFET channel current i_{CH} is expressed by equation 5.

$$i_{CH}(t) = i_S(t) - C_{DS}(v_{DS_CHIP}(t))\frac{dv_{DS_CHIP}(t)}{dt} + \\ -C_{DG}(v_{DG_CHIP}(t))\left(\frac{dv_{DS_CHIP}(t)}{dt} - \frac{dv_{GS_CHIP}(t)}{dt}\right) \quad (5)$$

where: v_{GS_CHIP} – estimated on-chip gate-source voltage.

That results in a waveform representing the estimated channel current, shown in figure 8. It is worth noticing that the amplitude of the capacitive current component (C_{OSS} current) in the case of a rapid turn-off process of the SiC MOSFET power module exceeds 130 A. If the commonly-used method of turn-off switching energy determination was used, it would result in a significant error. In the case of lower switching currents, the difference gets higher as the voltage slope steepness does not fall significantly. As the MOSFET channel current has been calculated, the turn-off switching energies (E_{OFF}) have been determined according to equation 6 and presented in figure 9.

$$E_{OFF} = \int_{t_3}^{t_4} v_{DS_CHIP}(t) i_{CH}(t) dt \quad (6)$$

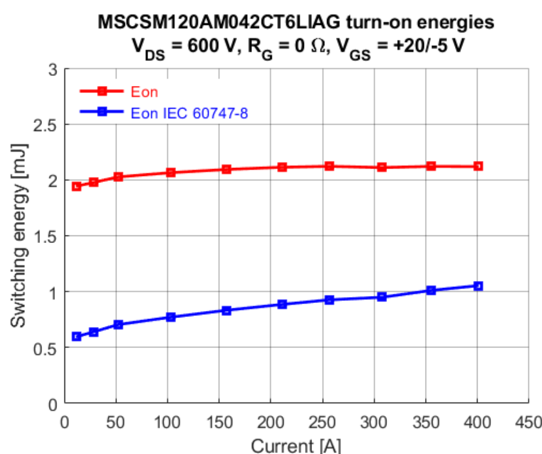

Fig.7. Turn-on switching energies of SiC MOSFET under test determined using two methods

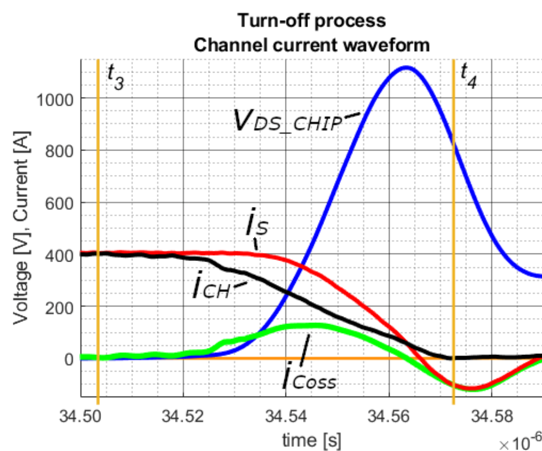

Fig.8. Calculated SiC MOSFET under test channel current waveform during the turn-off process

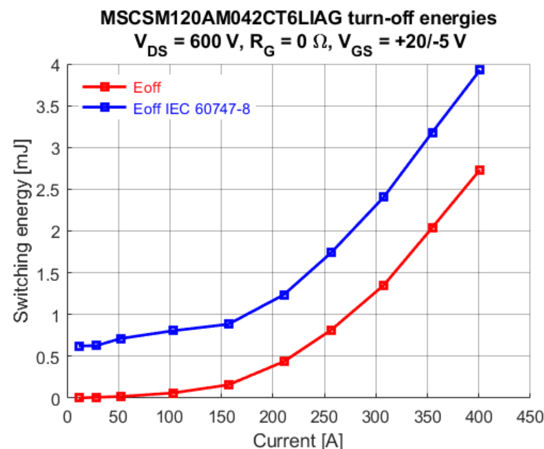

Fig.9. Turn-off switching energies of SiC MOSFET under test determined using two methods

Considering the post-switching oscillation phase, simplified equivalent circuits after full turn-on and turn-off were derived as proposed in [20]. Then, the energy dissipated in the equivalent resistance was calculated. For the operating point of 600 V, 400 A it results in 587,4 μJ of additional power losses related to the switching processes (E_{OSC}). Note that only a fraction of that energy is dissipated inside the power module, and E_{OSC} is strongly dependent on resistance in the power loop. In the case when the coaxial shunt resistor is not installed in the power loop, E_{OSC} drops to 195,6 μJ per switching cycle (E_{ON} +E_{OFF}). All in all, as that additional energy is related to the switching processes of the SiC MOSFET power module under test, it should be taken into account in the whole power loop switching losses determination process. To sum up, total power loop switching-related energies (E_{SW}), including the power module under test, are expressed by equation 7.

$$E_{SW} = E_{ON} + E_{OFF} + E_{OSC} \quad (7)$$

Total switching energies determined with the proposed method and the commonly-used method based on the IEC 60747-8 standard have been presented in figure 10. Comparison shows significant underestimation of determined switching energies when using IEC 60747-8 method. For the 210 A switched current, the determined switching energies are 28,7% higher than in the case when the IEC 60747-8 standard method is used. The lower the load current, the higher the difference.

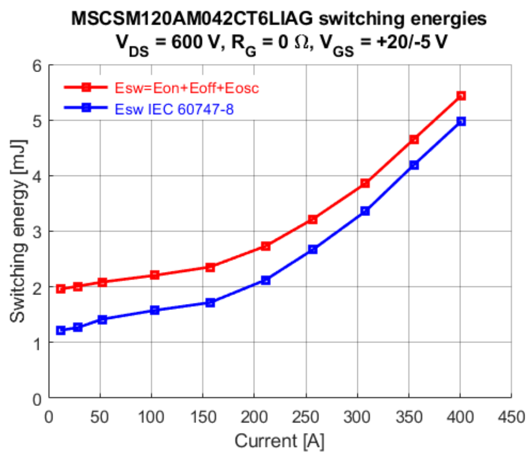

Fig.10. Total switching-related energies determined with the proposed method and the IEC 60747-8 standard method

Special care has to be taken in soft-switching topologies in which only one switching transition (turn-on or turn-off) is under zero-voltage or zero-current conditions. In such converters, switching energies determination with the IEC 60747-8 standard method might lead to significant errors, as shown in figure 7 and figure 9.

Conclusions

Obtained results show that commonly-used methods (based on IEC 60747-8 standard) for dynamic performance determination, in the case of new-generation SiC MOSFET power modules, might not be reliable and may lead to significant errors. In this paper, a comprehensive approach to dynamic performance determination tests of fast-switching SiC MOSFET modules is proposed and experimentally verified.

In practical applications of fast-switching SiC MOSFET power modules, parasitic inductances in the power loop can be minimized to the order of single nH, lowering the drain-source overvoltages during the turn-off processes. At the same time, the resonant frequency of the power loop can exceed 50 MHz, making it even more challenging to determine the dynamic parameters of the new-generation SiC MOSFET power modules due to the limited bandwidth and rise/fall times of Rogowski coil current probes currently available on the market, as coaxial shunt resistors significantly affect parameters of the power loop. Alternatively, in the case of the fast-switching losses determination process, calorimetric methods of power loss measurements might be the right direction. Thus, further studies are needed, especially because future generations of SiC MOSFETs are expected to exhibit even more dynamic switching characteristics.

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