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Inexpensive, high-performance STM32-based software PLL for series-resonant inverters

***Abstract**. This paper presents an inexpensive, high-performance STM32-based software phase-locked loop (PLL) system suitable for series-resonant inverters (SRIs) with various control methods. The paper shows how to achieve high resolution in setting the voltage-current time-shift with the proposed PLL using the microcontroller of the STM32G4x4 line, shows the features of the operation and implementation of this PLL. The proposed software PLL is implemented in the same microcontroller that controls the SRI output current, which makes it possible to simplify the structure of the SRI control system.*

***Streszczenie.** W niniejszym artykule przedstawiono niedrogi, wysokowydajny system oparty na oprogramowaniu STM32 z pętlą synchronizacji fazowej (PLL), odpowiedni dla falowników rezonansowych (SRI) z różnymi metodami sterowania. Artykuł pokazuje jak osiągnąć wysoką rozdzielczość w ustawianiu przesunięcia czasowo-prądowego z proponowanym PLL z wykorzystaniem mikrokontrolera linii STM32G4x4, pokazuje cechy działania i realizacji tego PLL. Proponowane oprogramowanie PLL jest zaimplementowane w tym samym mikrokontrolerze, który steruje prądem wyjściowym SRI, co pozwala na uproszczenie struktury układu sterowania SRI. (**Niedrogie, wydajne oprogramowanie PLL oparte na STM32 do szeregowych falowników rezonansowych**)*

Keywords: digitally controlled oscillator, inverter, microcontroller, phase-locked loop, phase-shift, timer.
Słowa kluczowe: sterownik PLL, częstotliwość sterowana cyfrowo.

Introduction

Phase-locked loops (PLLs) are closed-loop feedback systems commonly used in many applications, including phase synchronization between voltage and current at the output of a series-resonant inverter (SRI). To reduce switching losses in SRI transistors, the PLL must accurately set the desired value of a phase-shift (time-shift) between the voltage and current at the SRI output.

Phase synchronization can be implemented by using: special integrated circuits in combination with the discrete components [1-3] (hardware or analog implementation); microprocessors (software implementation) [4-6]. The hardware implementation is less flexible compared to the software implementation in connection with the need to change the analog components used to tune the operating frequency range or with the need to change the value of the dead-time between the control signals of the SRI transistors during the operation. As a consequence, the software implementation of the PLL seems to be more suitable than a hardware one. On the other hand, the software implementation with a microprocessor (a microcontroller or a digital signal processor) requires a high time-resolution of the controlled oscillator.

In addition to microprocessors, a software PLL can be implemented using field-programmable gate arrays (FPGAs) [7-9]. But programming complexity and weaker integrated peripherals are a barrier and justify the use of microprocessors.

Recently, with the development of new microcontrollers (MCUs) and digital signal processors (DSPs), they have become very suitable for industrial control due to their high-speed performance, wide range of peripherals, and low cost. Thus, DSPs [5] and MCUs [6] have been used to create software PLLs that, in addition to the main task of phase synchronization, provide an adjustable dead-time.

Moreover, the software PLL can be implemented in the core of the SRI control system, which is very convenient, but difficult to implement using a hardware PLL with many control methods. Thus, only one DSP/MCU is needed to provide SRI output current/power regulation and PLL implementation.

Typically, newer DSPs/MCUs have timers that can be clocked significantly above the system clock frequency, allowing for the higher time resolution of the controlled oscillator.

At the same time, the phase angle between voltage and current at the SRI output depends on the quality factor of the resonant circuit. As a consequence of this, the accuracy of setting the desired value of the time-shift is several times less than the time-resolution of the used controlled oscillator. Thus, the accuracy of setting the desired value of the time-shift with the software PLLs mentioned in the above works is more than 100 ns, which, in the case of using new silicon carbide transistors, is close to, or even more than, the recharge time of the output capacitances of these transistors. As a result, in order to avoid non-zero-voltage-switching owing to a change in time-shift, the PLL must set the moment of the beginning transistors turn-off too far from the moment of zero-current crossing, which leads to an increase in switching losses in the transistors.

The present paper is built upon the previous study [10] and extends the results by presenting an improved structure of the SRI controls system with the software PLL, and also describes in more depth the features of operation and implementation of this PLL. Additional experimental results have been presented that show the accuracy of setting the phase-shift between the voltage and current at the SRI output using various control methods of the SRI output current.

Description and operation principles of a software PLL

In its basic configuration, the phase-locked loop consists of three functional blocks: a phase detector (PD), a loop filter (LF), and a controlled oscillator. The phase detector compares the phase difference of the input signals, one of which is a reference signal, and the other is a feedback signal (which is the signal generated by or derived from the controlled oscillator of the PLL). The main function of a loop filter (usually a low pass filter) is to integrate the phase detector signal to provide loop stability, which also determines how quickly the loop achieves lock. In the case of a software PLL (SPLL), all or almost all of these functional blocks are software implemented in a source code.

There are several approaches to measuring the phase-shift (time-shift) between the output voltage v_O and the output current i_O of the SRI, which affects the block diagram of the SPLL system (Fig. 1):

- The first approach is a direct measurement of the phase-shift between υ_O and i_O (Fig. 1a) [3-5]. In this case, two zero-crossing detectors are needed to form the input signals for the PLL system (υ_{SQ} and i_{SQ} are square-wave voltage signals in the desired voltage range, which are derived from υ_O and i_O, respectively), where the current signal is used as a reference signal and the voltage signal is a feedback signal derived from the control signals generated by the digitally controlled oscillator (DCO).
- The second approach differs in that instead of directly measuring υ_O, the compensator signal (derived from the signals generated by the PLL) is used as a reference signal (Fig. 1b) [3, 6, 11]. The compensator is used to account for the propagation delay between the signals generated by the PLL and the υ_O signal.
- Third: the delay provided by the compensator can be taken into account programmatically, which makes it possible to simplify the structure of the PLL (Fig. 1c).
- The fourth approach is similar to the previous one, but differs in that the DCO generates an additional signal with some time-shift, which already takes into account the delay (Fig. 1d). This allows the PLL not to calculate the absolute value of the time-shift between the input signals of the PD, but only to determine which of the signals is leading.

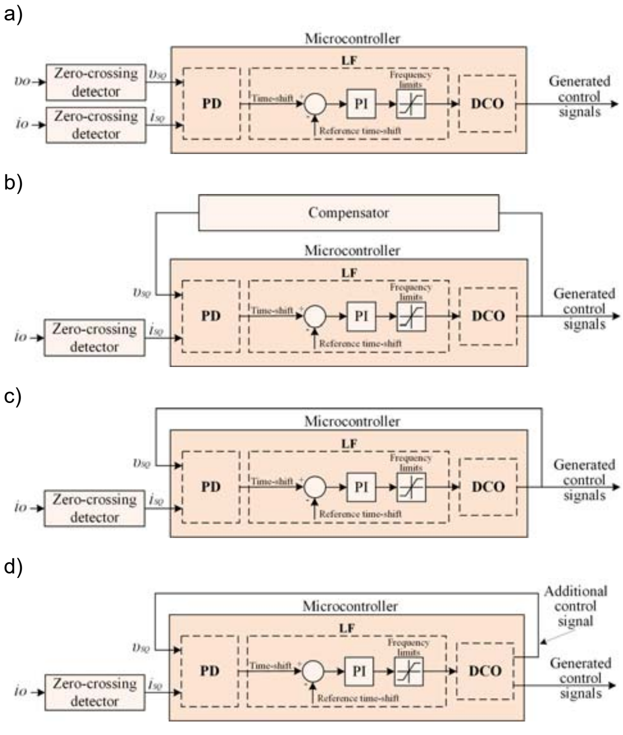


Fig.1. Block diagrams of the SPLL systems.

Direct measurement of the phase-shift when using the odd (3rd or 5th) harmonic operation [12, 13], the pulse-density-modulation (PDM) control method [9, 14, 15], or control methods based on them [16-18], is difficult owing to different frequencies of υ_O and i_O or the presence of the zero-voltage state at the SRI output during a free-wheeling interval.

The block diagram of a PLL system with a compensator requires additional components and is, therefore, less attractive due to the possibility of using block diagrams that take into account the delay (Figs. 1c and 1d).

In the case of SPLL systems, the phase-detector can operate in the following ways: 1) by detecting the edges of the input signals using MCU/DSP capture registers and calculating the difference between the values of these registers (Fig. 2a) [5], or 2) by determining only the leading signal (Fig. 2b) [6].

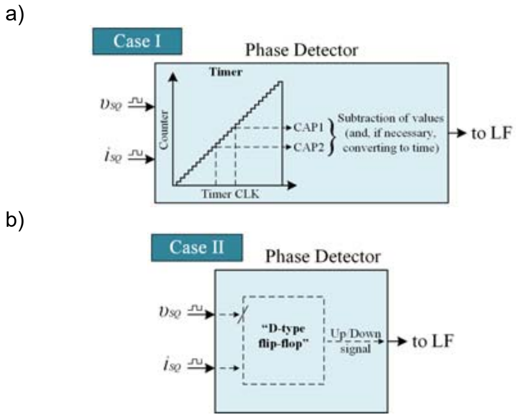


Fig.2. Phase-detector operating principles.

In the first case, the difference between the values of the capture registers is calculated. It is not necessary to change the difference value if the additional signal is used and it is shifted by a certain time. But, if the feedback signal is one of the control signals generated by the DCO, or if the additional signal is insufficiently shifted, the difference must be calculated taking into account the delay.

In the second case, only the leading signal is determined, which avoids calculating the difference between the values of the capture registers. On the other hand, in order to correctly determine the leading signal, the MCU/DSP must generate an interrupt on the rising/falling edge of one of the PD inputs and immediately read the logical state of the other PD input, this is essentially close to the operation of a D-type flip-flop. Thus, the determination of the leading signal consists in detecting the mentioned logical state at a given moment in time. However, interrupt generation and its processing take some time, and, as a consequence, it affects the correct detection of the leading signal. In order to avoid this problem and the loss of useful operating time of the MCU/DSP, it is expedient to implement the PD by using a D-type flip-flop outside of the MCU/DSP.

The loop filter structure is similar for both cases of PD operation. But in the case of the leading signal detection, the LF doesn't need a summing point, and therefore the integrator or proportional integrator (PI) changes the DCO counter value not by the integrated difference, but by some set value.

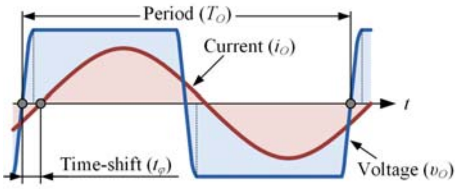


Fig.3. The time-shift between υ_O and i_O.

Time-shift setting accuracy

To reduce switching losses in the SRI transistors, recharging of the output capacitances of the transistors should be completed close to the zero-current crossing point, but a little earlier, before turning-on the next transistors [14, 18] (Fig. 3). The recharge time of the capacitances depends, among other things, on the SRI output current and the operating frequency. Therefore, the dead-time between the control signals of the SRI transistors should be changed during operation.

The correct setting of the dead-time value and the moment when the transistors start to turn off (the time-shift between the output voltage and the output current) depends on the resolution of the DCO.

The phase angle between the output voltage υ_O and the output current i_O of the SRI is expressed as follows:

$$\varphi = \arctan\left(\frac{\omega_O L - \dfrac{1}{\omega_O C}}{R}\right) = \arctan\left(Q\left(\frac{\omega_O}{\omega_r} - \frac{\omega_r}{\omega_O}\right)\right) \tag{1}$$

where ω_O is the angular operating frequency; $\omega_r = 1/\sqrt{LC}$ is the angular resonant frequency of the resonant circuit; Q is the quality factor of resonant circuit; R, L, and C are equivalent elements of the series resonant circuit connected to the inverter output.

The time-shift between υ_O and i_O is given by

$$t_\varphi = \frac{T_O}{2\pi}\arctan\left(Q\left(\frac{T_r}{T_O} - \frac{T_O}{T_r}\right)\right) \tag{2}$$

where T_O is the period of υ_O, which is set by the DCO; T_r is the period of the resonant oscillation.

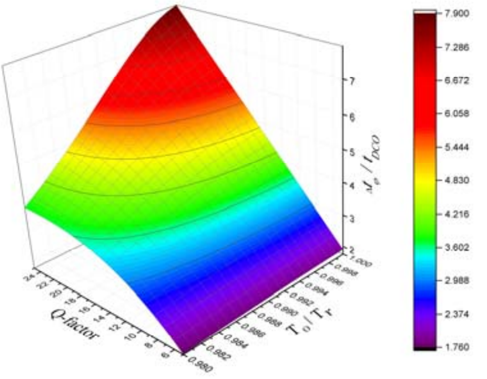
The influence of the DCO resolution can be estimated through the offset $_\Delta t_\varphi$ between two adjacent values of T_O. It should be noted that in order to ensure the equal duration of half-periods of T_O, the duration of T_O must be changed by a time multiple of twice the DCO resolution. Thus, the offset can be expressed as follows:

$$_\Delta t_\varphi = t_\varphi\left(Q,\left(T_O - t_{DCO}\right)\right) - t_\varphi\left(Q, T_O\right) \tag{3}$$

where t_{DCO} is the time step of T_O, a multiple of twice the DCO resolution.

It is convenient to analyze the dependences $_\Delta t_\varphi(t_{DCO})$ through the relative dependence:

$$\frac{_\Delta t_\varphi}{t_{DCO}} = \frac{t_\varphi\left(Q,\left(T_O - t_{DCO}\right)\right)}{t_{DCO}} - \frac{t_\varphi\left(Q, T_O\right)}{t_{DCO}}. \tag{4}$$



Were calculated for the following values: $L = 0.539$ [μH], $C = 4.7$ [μF].

Fig.4. Dependence of $_\Delta t_\varphi/t_{DCO}$ on the following parameters: on the Q-factor of the resonant circuit and on the ratio T_O/T_r.

Due to the fact that switching occurs near zero-current and $t_{DCO} << (T_O/2)$, the relative dependence of $_\Delta t_\varphi/t_{DCO}$ is almost a linear function of t_{DCO}. Therefore, Fig. 4 shows the relative dependence $_\Delta t_\varphi/t_{DCO}$ on the quality factor in the range from 5 to 25 and on the T_O/T_r relationship (which specifies the initial phase-shift) for a t_{DCO} value of 10 ns.

As it can be seen in this figure, at Q = 25 the change in t_{DCO} leads to an increase in the offset $_\Delta t_\varphi$ of up to 8 times. Therefore, to provide some desired value of $_\Delta t_\varphi$, the DCO resolution must be at least 16 less.

Proposed STM32-Based Software PLL

The STM32 family of 32-bit microcontrollers (combining very high performance, real-time capabilities, digital signal processing, and low-power, low-voltage operation) is designed for a wide range of applications. Many STM32 microcontrollers have timers that allow forming complex signals.

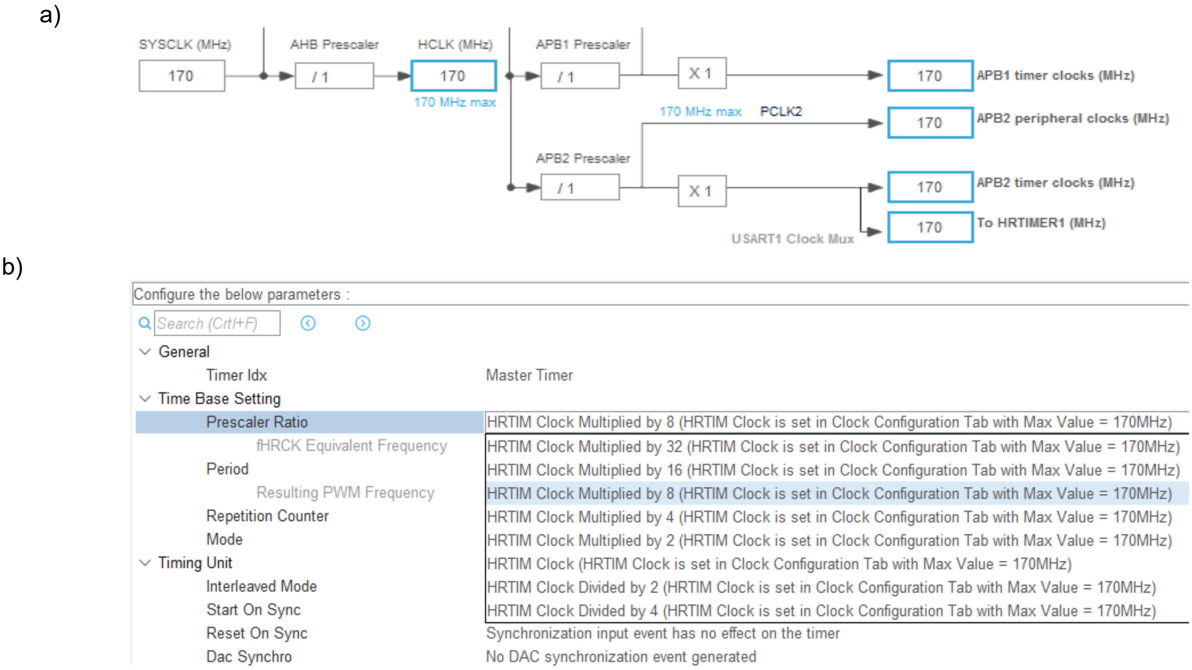
It is possible to use the asymmetric mode of the advanced-control timer to generate center-aligned PWM signals with a programmable phase-shift [10, 19]. In this case, only one advanced-control timer is required to generate four control signals. But t_{DCO} cannot be less than the system clock. Furthermore, in this mode, the timer counts UP-DOWN, so the minimum value of the DCO resolution is at least four times the DCO resolution. Moreover, calculating the values of the timer registers when the frequency changes are quite complex. Thus, this solution is more suitable for generating control signals when the operating frequency of the SRI is constant.

Another solution is to use the advanced-control timer in the edge-aligned mode. In this case, the timer channels must operate in the combined PWM modes [10]. Compared to the solution mentioned above, the minimum value of t_{DCO} is only twice the value of the DCO resolution, but the timer uses four channels to form two control signals. Thus, four control signals require two advanced-control timers, which are not available in all STM32 microcontrollers. Moreover, in order to avoid the problem of the time perception between two timers, one of them should be the master for the second, and the second should work as a slave.

Both of these solutions for forming the transistors control signals in the case of using the PDM or PS-PDM (combining the phase-shift (PS) control method with the PDM control method) control methods require an additional logic block and control signals to form the PDM envelope. Besides, for high-frequency applications, the resolution of their timers leaves much to be desired.

The third solution is to use the high-resolution timer (HRTIM) of STM32 microcontrollers. The HRTIM is available in the STM32F3, STM32G4, and STM32H7 microcontroller families, but not in all MCUs of these families [20, 21]. The HRTIM input frequency can reach the system clock frequency (Fig. 5a), and the HRTIM output (equivalent) frequency of the STM32F3 and STM32G4 microcontroller families can be significantly increased (up to 32 times) by multiplying the HRTIM clock frequency (f_{HRTIM}) (Fig. 5b), which is an unavailable option in microcontrollers of the STM32H7 family. Thus, the best result in timer resolution (up to 184 ps) can be achieved with microcontrollers of the STM32G4 family.

The HRTIM includes six timing units (timers A, B, C, D, E, and F), each timing unit holds the control of two outputs. To achieve the desired output frequency for the signals generated by the HRTIM, the HTRIM equivalent frequency (f_{HRCK}) must be decreased by setting the period values in the HRTIM registers. On the other hand, there are restrictions on the maximum values of these registers, and as a consequence, on the minimum value of the output frequency. Thus, HRTIM time resolutions and frequency limits versus HRTIM equivalent frequencies are shown in Table 1.



Configure the below parameters :

- General
  - Timer Idx: Master Timer
- Time Base Setting
  - Prescaler Ratio: HRTIM Clock Multiplied by 8 (HRTIM Clock is set in Clock Configuration Tab with Max Value = 170MHz)
  - fHRCK Equivalent Frequency
  - Period
  - Resulting PWM Frequency
  - Repetition Counter
  - Mode
- Timing Unit
  - Interleaved Mode
  - Start On Sync: Synchronization input event has no effect on the timer
  - Reset On Sync
  - Dac Synchro: No DAC synchronization event generated

HRTIM Clock Multiplied by 32 (HRTIM Clock is set in Clock Configuration Tab with Max Value = 170MHz)
HRTIM Clock Multiplied by 16 (HRTIM Clock is set in Clock Configuration Tab with Max Value = 170MHz)
HRTIM Clock Multiplied by 8 (HRTIM Clock is set in Clock Configuration Tab with Max Value = 170MHz)
HRTIM Clock Multiplied by 4 (HRTIM Clock is set in Clock Configuration Tab with Max Value = 170MHz)
HRTIM Clock Multiplied by 2 (HRTIM Clock is set in Clock Configuration Tab with Max Value = 170MHz)
HRTIM Clock (HRTIM Clock is set in Clock Configuration Tab with Max Value = 170MHz)
HRTIM Clock Divided by 2 (HRTIM Clock is set in Clock Configuration Tab with Max Value = 170MHz)
HRTIM Clock Divided by 4 (HRTIM Clock is set in Clock Configuration Tab with Max Value = 170MHz)

Fig.5. HRTIM clocking: a) dependency of the HRTIM input clock on the HRTIM system clock; b) the option of the HRTIM output frequency prescaling.

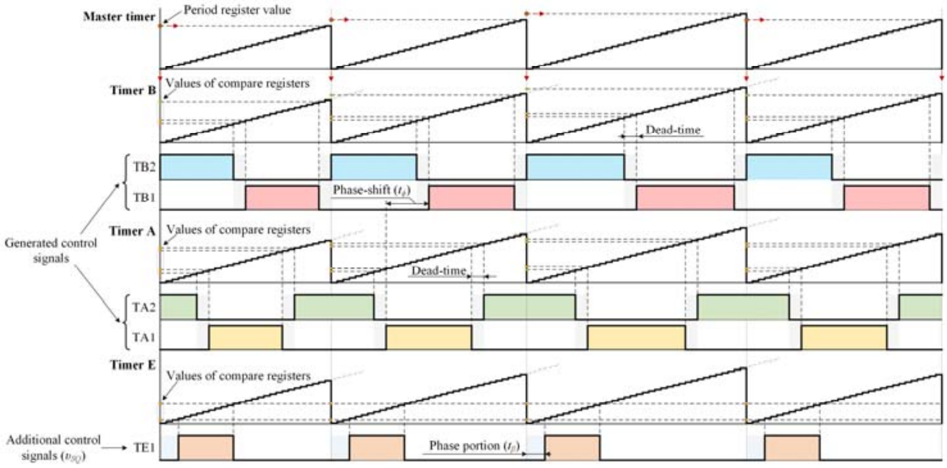

Master timer
Period register value
Timer B
Values of compare registers
Dead-time
TB2
TB1
Phase-shift (t_ϕ)
Timer A
Values of compare registers
Generated control signals
Dead-time
TA2
TA1
Timer E
Values of compare registers
Additional control signals (v_{SQ})
TE1
Phase portion (t_β)

Fig.6. An example of generating control signals using the HRTIM for the PS control method.

Table 1. HRTIM time resolutions and frequency limits versus HRTIM equivalent frequencies

Equivalent frequency (f_{HRCK}), for f_{HRTIM} = 170 [MHz]	Resolution [ns]	Minimum frequency [kHz]
170 x 32 = 5.44 GHz	0.184	83.05
170 x 16 = 2.72 GHz	0.368	41.515
170 x 8 = 1.36 GHz	0.735	20.755
170 x 4 = 680 MHz	1.47	10.377
170 x 2 = 340 MHz	2.94	5.188
170 MHz	5.88	2.594
170 / 2 = 85 MHz	11.76	1.297
170 / 4 = 42.5 MHz	23.53	0.649

Fig. 6 shows an example of generating the control signals using the HRTIM for the PS control method; the master timer, the timers A, B, and E are used. The master timer is used to set the duration of the voltage period by changing the value of its period register. The values of other timers' period registers are set to the maximum value but are reset when the end of the main timer period is reached. Thus, by changing only the value of the period register of the master timer, the periods of other timers become the same as those of the master one. The formation of the control signals waveforms is provided by setting values in the compare registers of the timers A and B. The formation of the control signals waveforms is provided by setting the values of the compare registers of the timers A and B. By changing the values of these registers, it is possible to adjust the phase-shift (time-shift) and dead-time. The timer E generates the additional control signal, which is used as the PLL feedback signal. Due to this signal, the propagation delay is compensated and the phase portion (where the voltage and current at the inverter output are in the opposite direction to ensure the ZVS operation) is provided. Within a running period, all values of timers' registers must be updated before the next period.

The control signals using the HRTIM for the PDM control method can also be obtained in the same way as shown in [22]. And with the HRTIM, it is also possible to generate control signals for other control methods such as pulse-width modulation, asymmetric duty cycle, asymmetrical voltage-cancelation, combined PS-PDM, 3rd-5th order harmonics operation, etc.

It should be noted that it is expedient that all variants of shapes of the control sequences for the PDM control method are stored in the MCU code. This somewhat complicates the source code of the MCU program but allows one to significantly simplify the structure of the logical block or completely abandon its use (Fig. 7).

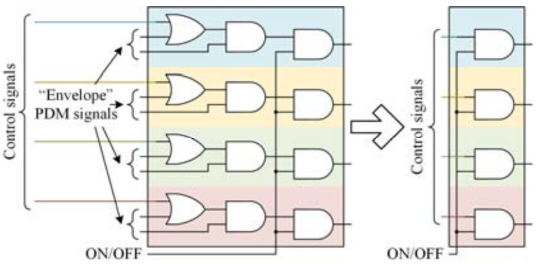


Fig.7. Logical block simplification.

Fig. 8 shows a block diagram of the SRI control system, in which two main tasks (PLL and current control) are implemented by one MCU core. The presented control system is based on the STM32G474 microcontroller of the STM32G4x4 line, and the PLL part of the control system corresponds to the PLL shown in Fig. 1d, except for the PD (the D-type flip-flop is outside the MCU).

Three data values (required frequency, dead-time (T_{DT}), and PDM) are considered by HRTIM when generating control signals. In the case of a high value of Q-factor of the resonant circuit when the load parameters of the SRI change relatively slow, the required T_{DT} value can be calculated indirectly through the average rectified value (ARV) of the SRI output current, otherwise, by directly determining the peak current value. The PDM pattern and/or the phase-shift value are selected according to the error signal from the differential amplifier. The task signal (reference value of the SRI output current) is fed to the amplifier from the digital-to-analog converter of the MCU and is increased/decreased by external signals from an N-coder. Thus, the reference value is adjusted with high precision, which depends only on the resolution of the DAC.

The presented block-functional structure of the MCU is focused on the use of PDM, PS, or PS-PDM control methods. But it can easily be modified to provide other control methods.

Experimental results

The proposed STM32-based software PLL system was tested using an experimental prototype of an induction heating system for melting applications (Fig. 9). The accuracy of the phase-shift setting was evaluated using the following inverter control methods: PDM, PS, and PS-PDM.

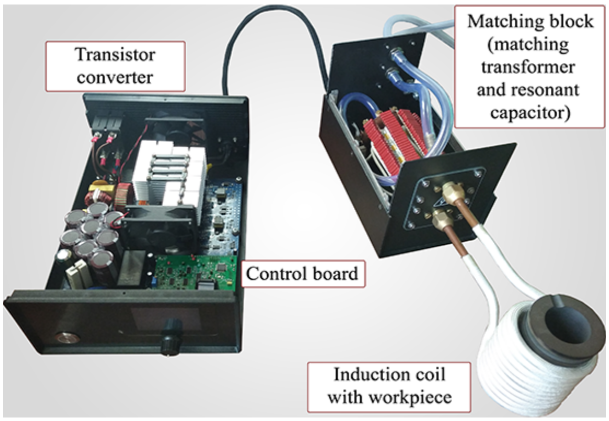

Transistor converter
Matching block (matching transformer and resonant capacitor)
Control board
Induction coil with workpiece

Fig.9. The prototype of an induction heating system for melting applications.

The inverter operating frequency range of the SRI was set from 25 kHz to 50 kHz. Therefore, the HRTIM prescaler was chosen to provide the minimum operating frequency of 25 kHz. Thus, the equivalent frequency of the HRTIM was 1.36 GHz, which allows makes it possible to obtain the resolution of up to 0.735 ns, therefore, t_{DCO} is 1.47 ns. In steady-state mode, the PLL system using a D-type flip-flop will always be cycling between increasing and decreasing the operating frequency. Thus, it should be expected that the offset $_{\Delta}t_{\varphi}$ between two adjacent values of T_O at Q equal to 25 should be at least to 12 ns.

Fig. 10 shows the circuit diagrams of the current sensor, zero-current crossing detector, and D-type flip-flop of the SRI control system blocks used in the prototype. The measured value of $_{\Delta}t_{\varphi}$ during the experiments was determined as the maximal time of deviation of the zero-current crossing detector output signal i_{SQ} relative to the additional control signal υ_{SQ} (see Fig. 10).

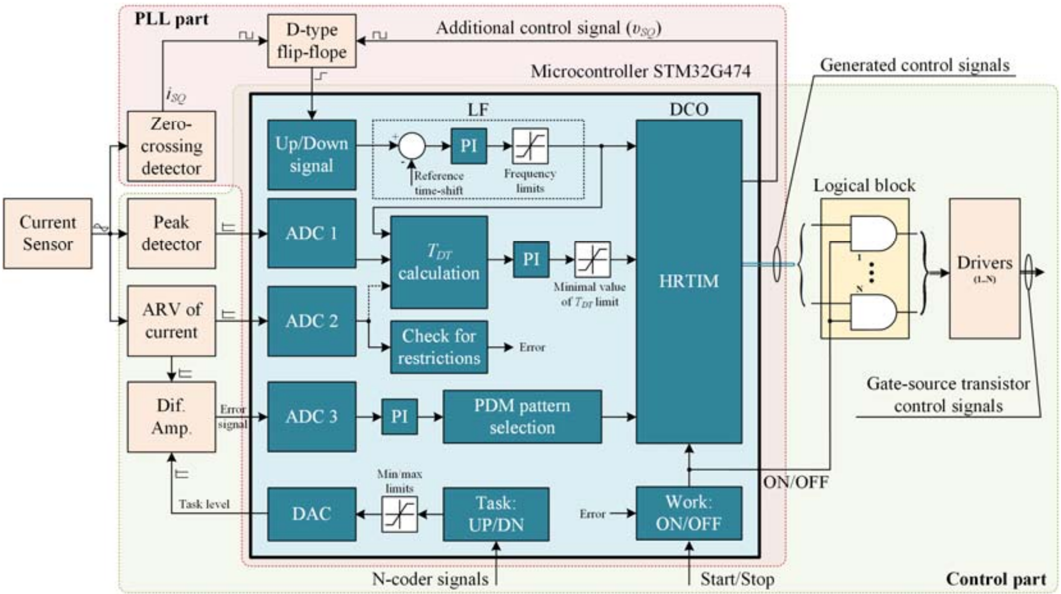


Fig.8. The block diagram of the SRI control system.

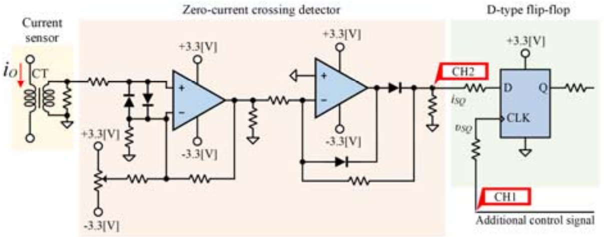


Fig.10. Circuit diagrams of some blocks of the SRI control system.

Fig. 11 shows the experimental results of the measuring Δt_{φ} with various control methods (channels 1 and 2 of the oscilloscope – i_{SQ} and υ_{SQ}, respectively). It should be noted, that in order to obtain a high value of the Q-factor ($Q \approx 22$), the experimental prototype worked without a workpiece in the induction coil; and to limit current, the input voltage of the SRI was reduced to 65 V; the dead-time value was set constant; the values of the phase-shift and pulse-density were set manually.

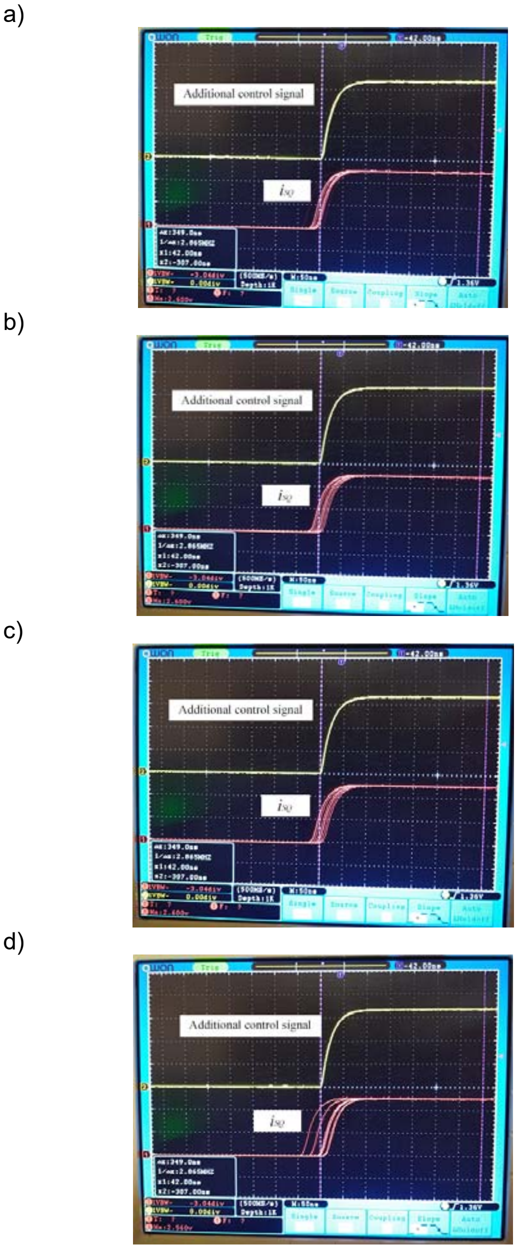

a)
Additional control signal
i_{SQ}
b)
Additional control signal
i_{SQ}
c)
Additional control signal
i_{SQ}
d)
Additional control signal
i_{SQ}

Fig.11. The measured value of the time offset in experiments using inverter output current control methods: a) operation with phase-shift equal to 0 and pulse-density equal to 1, b) PS, c) PDM, d) PS-PDM.

In the case of operation without current regulation (phase-shift is 0 and pulse-density is 1), the value of Δt_{φ} was close to 25 ns (Fig. 11a). In cases where the control methods are in effect, the value of Δt_{φ} is higher. Thus, its value is close to 40 ns when using the PS control method (Fig. 11b), to 65 ns when using the PS-PDM and PDM control methods (Figs. 11c and 11d, respectively).

The discrepancy between the expected and measured values of Δt_{φ} can be explained by the influence of the current amplitude on the correct determination of the zero-crossing point. As the current amplitude decreases, the determination of the zero-crossing point is less correct. There is also a discrepancy between frequencies of the current and the voltage at the output of the SRI when using PS-PDM and PDM control methods due to the presence of a free-wheeling interval. For these reasons, the output signal of the D-type flip-flop changes less frequently (Fig. 12, channels 1 and 2 of the oscilloscope – the output signal of the D-type flip-flop and υ_{SQ}, respectively), which leads to an increase in the value of Δt_{φ}.

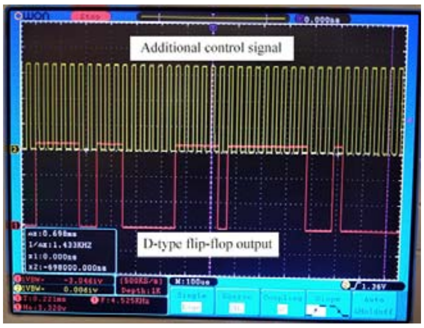


Fig.12. Changing the output signal of the D-type flip-flop in relation to the additional control signal.

Theoretically, Δt_{φ} can be further decreased at a higher minimum operating frequency, twice for the minimum operating frequency of 41.515 kHz, and four times for the minimum operating frequency of 83.05 kHz.

Conclusion

This paper proposes an inexpensive, high-performance STM32-based software PLL suitable for SRIs with various control methods. The experimental results show that using the proposed PLL, it is possible to obtain the time offset between the voltage and the current at the output of the SRI in the range from 25 to 65 ns, depending on the control method used, and it can be further decreased at a higher minimum operating frequency. Besides, the proposed software PLL is implemented in the same microcontroller that controls the output current of the SRI, which makes it possible to simplify the structure of the SRI control system. Thus, the main core of the control system is a microcontroller of the STM32G4 family that costs about 7$ and several additional integrated circuits.

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