Khaled A. Mahafzah[1], Qais Al Azzam[2], Ibrahim Altawil[3]
Al-Ahliyya Amman University (1), Irbid District Electricity Company (2), Yarmouk University (3)
ORCID: 0000-0003-3996-7588, 0000-0000-0000-0000, 0000-0000-0000-0000

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A Soft Switched Single Ended Primary Inductor Converter Power Factor Correction Circuit for Low Power Applications

Abstract. *The current study aims at investigating a Single Ended Primary Inductor Converter Power Factor Correction (SEPIC PFC) circuit of low power applications such as the adapters of laptops and mobiles. The SEPIC PFC is designed in CRitical Conduction Mode (CRM) to drive 30W load. A closed loop control circuit is designed to maintain 15V-DC constant output voltage with Constant On Time (COT). The designed circuit is validated by LTSPICE software with a switching frequency up to 260kHz. A Zero Current Switching (ZCS) for the power switch is achieved, thus reducing the switching losses. The design considerations of SEPIC PFC are discussed. The simulation results show that the proposed design has nearly a unity power factor and a satisfying efficiency result over the line voltage range.*

Streszczenie. *Obecne badanie ma na celu zbadanie obwodu korekcji współczynnika mocy konwertera indukcyjnego z pojedynczą końcówką (SEPIC PFC) w zastosowaniach o niskim poborze mocy, takich jak przejściówki do laptopów i telefonów komórkowych. SEPIC PFC został zaprojektowany w trybie krytycznego przewodzenia (CRM), aby zasilać obciążenie o mocy 30 W. Obwód sterujący z zamkniętą pętlą jest zaprojektowany do utrzymywania stałego napięcia wyjściowego 15 V DC przy stałym czasie włączenia (COT). Zaprojektowany obwód jest walidowany przez oprogramowanie LTSPICE z częstotliwością przełączania do 260kHz. Osiągnięto przełączanie zerowego prądu (ZCS) dla przełącznika zasilania, zmniejszając w ten sposób straty przełączania. Omówiono zagadnienia projektowe SEPIC PFC. Wyniki symulacji pokazują, że proponowana konstrukcja ma prawie jedność współczynnika mocy i zadowalający wynik wydajności w całym zakresie napięcia linii. (Obwód korekcji współczynnika mocy przekształtnika z przełączaną indukcyjnością do zastosowań o małej mocy)* ***(Wybór procedury optymalizacyjnej dla systemu CAD)***

Keywords: SEPIC PFC, CRitical Conduction Mode (CRM), Constant On Time (COT), Efficiency, Low power
Słowa kluczowe: poprawa współczynnika mocy, przekształtnik, przełączalna indukcyjność

Introduction

An AC-DC converters are essential electrical power conversion interfaces between various electrical load and AC power grid. They are widely employed in different applications, including, but not limited to, Adjustable Speed Drives (ASDs), Switch Mode Power Supplies (SMPS), and battery energy storage. The main disadvantages of the widespread applications, such as poor power quality, poor power factor, and low efficiency, have forced the researchers to develop new power factor correction techniques. [1]-[2].

Several PFCs were designed in different operation modes. They are Continuous Conduction Mode (CCM), CRitical conduction Mode (CRM) or Boundary Condition Mode (BCM), and Discontinuous Conduction Mode (DCM), e.g., [3]-[12]. Converter topology was selected as per the respective application areas with various output power range from few watts to kilowatts. The power factor was improved. Hence, the total harmonics distortion (THD) met the international standards.

The PFCs in CCM of operation was suffering from hard switching, as the inductor current remains continuous over the switching period. However, it offered minimum current ripple and less Electromagnetic Interference (EMI) compared with other PFC's operating modes. Nevertheless, in CRM operation, zero current turn off of the semiconductor devices was achieved. Moreover, the demerit of CRM was that the switching frequency was varying over a wide range. This resulted in decreasing the efficiency and the complexity of EMI filter design[13]. Nonetheless, ZCS resulted in no reverse recovery in the diode. CRM was simple to control and its cost was low because of using less components[14].

The popularity, in addition to its other advantages- of the fly-back converter makes this topology more prefarable than SEPIC converter. Inspite that not of SEPIC topolgy has some attractive features such as, reducing the voltage stress on the power switch,being more efficient than the fly-back converter at the same operating conditions[10].

However, SEPIC was become more suitable topology to be deployed as the front-end AC-DC PFC converter. It can boost or buck the input voltage [14]. Because of high voltage conversion gain and input current continuity, it attracts attention from modern applications, especially those which involve renewable energy, fuel cells, battery chargers and photovoltaics[15],[16]. A comprehensive comparison of different published works with the present one is summarized in Table 1.

A SEPIC PFC which operates in CRM was presented [17]. The calculations and simulation results proved that the line current was pure sinusoidal waveform when the input to output voltage ratio (design factor) was zero, the line current will be distorted as this ratio, increased. This means that the SEPIC at Boundary Conduction Mode (BCM or CRM) cannot achieve unity power factor performance except at extreme conditions. *Therefore, This paper adds the following main contributions to the previously published ones (see Table 1): (i)The SEPIC PFC is designed for rated load of 30 Watt/15 V output voltage. This design decreases more the load voltage, thus, reducing the size of the used semiconductors. (ii) This PFC is operated in CRM to ensure the ZCS of the switch. Hence, ZCS improves the PFC's Efficiency. Other designs are operated mostly in CCM or DCM. (iii) The range of switching frequency in this paper is the highest. Keeping a high efficinecy under these operating condition is a big milestone. (iv) The paper summurizes a comprehensive criterias to select the best parameters for a practical designs resulting in lower THD compared to published ones. (v) A clooses loop control with type II compensation is designed to maintain the load voltage and to switch at ZCS.*

This paper is organized as follows: Section two analyzes the working principle of SEPIC PFC in Critical Conduction Mode. Section three presents the calculation of switching frequency and discusses the selection of optimal circuit components. In Section four, zero current detection and control loop are discussed. Section five discusses the power losses in SEPIC PFC circuit at operating conditions. Section six presents the results of simulations. Finally, the conclusions are drawn in Section seven.

Operation Princible in CRM with COT

The conventional SEPIC PFC is shown in Figure 1 (A). The circuit consists of Diode Bridge Rectifier (DBR) in front of conventional SEPIC converter. The status of switch M in Figure 1 determines the PFC's mode of operation as follows:

Table 1. Comparesion between Different SEPIC PFCs over Universal Voltage.

Ref.	f_s [KHz]	V_o [V]	P_o [W]	Current Mode	THD %	Efficieny %
[17]	112.3-142.6	210	100	CRM	4.9-18.1	89.9-91.5
[18]	40	400	4K	DCM	4	75-90
[19]	100	100	100	DCM	6-8	92
[20]	50	30	21	DCM	12.6	91.6
[21]	65	60	100	DCM	-	93.5
[22]	200	400	2K	CCM	<2	96.6
[23]	20	100	500	CCM	-	95.5
This Work	20-250	15	30	CRM	2.5-13.6	86.1-90

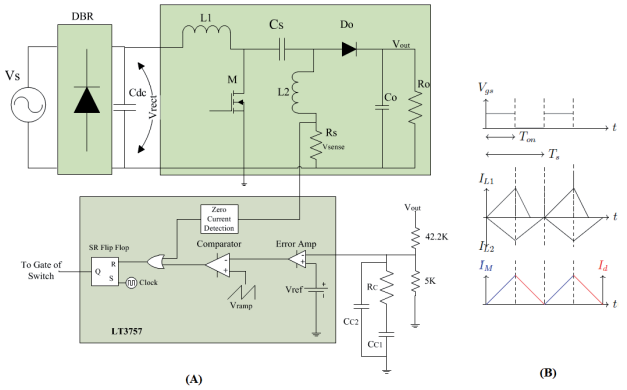

Fig. 1. (A) SEPIC PFC, (B) Current Waveforms.

- When the MOSFET M is turned on (during T_{on}), the rectified voltage (V_{rect}) is applied to L_1. Capacitor Cs (which has voltage equals to V_{Cs}) is in parallel with inductor L_2. Diode D_o is in blocking mode. The current in the switch M is as follow:

$$I_M(t) = I_{L1-on}(t) + I_{L2-on}(t) \tag{1}$$

where:

$$I_{L1-on}(t) = \frac{V_s(t)}{L_1}t,\ 0 < t < T_{on} \tag{2}$$

and,

$$I_{L2-on}(t) = \frac{-V_{Cs}}{L_2}t,\ 0 < t < T_{on} \tag{3}$$

Where $V_s(t) = V_m sin(2\pi f_{line} t)$ and $f_{line} = 50$Hz.
- When the MOSFET M is turned off, D_o starts conducting. Inductors L_1 and L_2 store energy which is later transfered to the load through the diode D_o. The current in the diode D_o is the sum of inductors' currents. Thus:

$$I_{Do}(t) = I_{L1-off}(t) + I_{L2-off}(t) \tag{4}$$

where:

$$I_{L1-off}(t) = I_{L1-on}(T_{on}) + \frac{V_s - V_o}{L_1}t,\ T_{on} < t < T_s \tag{5}$$

and,

$$I_{L2-off}(t) = I_{L2-on}(T_{on}) + \frac{V_o}{L_2}t,\ T_{on} < t < T_s \tag{6}$$

Figure 1(B) illustrates the inductors' currents waveformes. As seen in the figure, slopes of I_{L1} and I_{L2} are differes from each others depending on inductances.

To study the SEPIC PFC in CRitical Conduction Mode, there are some assumptions have been made [17]:

- The line voltage is assumed to be pure sinusoidal.
- It is assumed that the current is constant during any switching cycle. This is due to large inductances and because the switching frequency is more higher than the line frequency.
- The constant K_s is defind as V_m/V_o. Where, V_m is the peak of AC line voltage and V_o is the load voltage.
- To guarantee the ZCS (Critical Conduction Mode), the initial values of inductors' currents are set to zero.
- In steady state analysis, the average inductors' voltages are zero. Also, the average capcitors' currents are zero.

The switch's M turn on time T_{on} is estimated if the input and the output power are equal to each other. By using ($P_{out} = P_{\text{in}}\eta$) the average input power becomes is given by:

$$P_{in} = \frac{1}{\pi}\int_0^{\pi} v_s(\theta) i_s(\theta) d\theta \tag{7}$$

where, $i_s(\theta)$ is the input line current and given as follow:

$$i_s(\theta) = \frac{V_m sin\theta}{L_1}\frac{V_o}{V_o + V_m sin\theta}T_{on} \tag{8}$$

Solving for T_{on} using (7) and (8) gives:

$$T_{on} = \frac{2P_o}{\eta\sqrt{2}V_m f_{line}}\int_0^{T_{line}} \frac{sin^2\theta}{1 + K_s \mid (sin\theta) \mid} d\theta \tag{9}$$

where $T_{line} = f_{line}^{-1}$ and $K_s = V_m/V_o$. Therefore, the turn off time T_{off} is given by:

$$T_{off} = T_{on}\sqrt{2}K_s \mid sin\theta \mid \tag{10}$$

where:

$$T_s = T_{on} + T_{off} \tag{11}$$

where $T_s = f_s^{-1}$.

Figure 2 compares the average line current (dashed waveforms) with the standard sine wave (solid waveforms). As seen in this figure, the average line current in case of high line voltage (red-dashed) is generated at $K_{s-high} = 20.67$. However, the blue dashed curve in Figure 2 illustrates the average line current, which is generated at low line voltage and $K_{s-low} = 7.57$.

Power Factor and Total Harmonics Distortion

The power factor is estimated by:

$$P_{in} = \frac{P_o}{\eta} = V_{line-rms} I_{line-rms} cos\theta \tag{12}$$

where $cos\theta$ is the power factor of the line current (input current). Accordingly, it is given by:

$$cos\theta = \frac{P_o}{\eta V_{line-rms} I_{line-rms}} \tag{13}$$

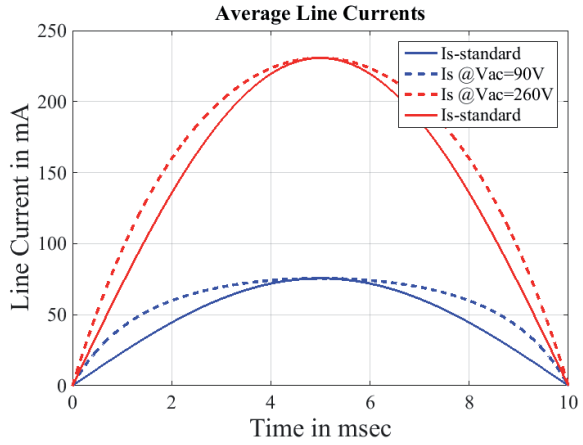

Fig. 2. Average Line Currents at Low Line Voltage (blue) and High Line Voltage (red).

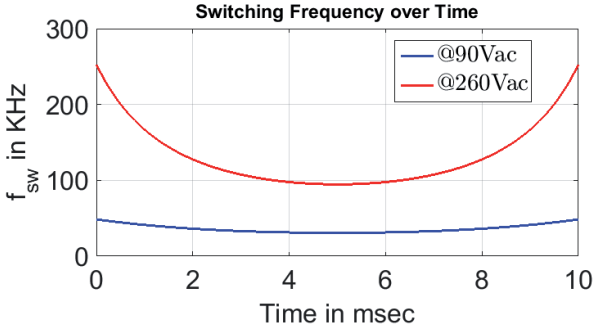

Fig. 3. Switching frequency over time, for low and high line voltages.

Therefore, The Total Harmonics Distortion (THD) is given by (assuming that displacement factor is one):

$$THD = \sqrt{\frac{1}{cos\theta^2} - 1} \tag{14}$$

Design Procedure

Importantly, the switching frequency, SEPIC inductors L_1 and L_2 and coupling capacitor C_c are selected in according to the next discussion.

Maximum Switching Frequency Determination

To find the maximum switching frequency for the switch M, it is usually estimated based on 9, 10 and 11 as:

$$T_s = T_{on} + T_{off} = T_{on} + T_{on}\sqrt{2}K_s sin\theta \tag{15}$$

Thus,

$$T_s = T_{on}(1 + \sqrt{2}K_s sin\theta) \tag{16}$$

and T_{on} determines the peak value of the inductors' currents as follows:

$$I_{pk} = \frac{V_m}{L_{eq}} T_{on} \tag{17}$$

and L_{eq} is the equivalent inductance of parallel L_1 and L_2.

This group of equations gives designers the freedom to select the maximum switching frequency. They then estimate the ratio between the two inductors in SEPIC circuit.

Hence, the switching frequency is estimated by:

$$f_s = \frac{\eta V_m^2 M(K_s)}{2L_{eq}P_o(1 + K_s sin\theta)} \tag{18}$$

where, L_{eq} is the equivelant of paralell inductance between L_1 and L_2, $M(K_s)$ is the integration shown in (9).

The equivalent inductance is estimated when the maximum switching frequency is set by the designer dependening on the selcted simeconductor switch e.g., Si-MOSFETs and Wide Gap Band MOSFETs, etc.

Figure 3 shows the variable switching frequencies of the SEPIC PFC in both limits of the line voltages. The switching frequency, in case of high line voltage (red curve), is located within the range 100KHz up to 250KHz. The blue curve in Figure 3 shows the switching frequency, in case of low line voltage, is between 20KHz up to 50KHz.

SEPIC Inductances: L_1 and L_2

To select the inductances values L_1 and L_2, according to [17], the inductor current shift I_o is given by:

$$I_o = \frac{1}{2}T_{on}V_s(t)\left(\frac{1}{L_2}\frac{V_o}{V_o + V_s(t)} - \frac{1}{L_1}\frac{V_s(t)}{V_s(t) + V_o}\right) \tag{19}$$

However, in this paper, inductor current shift is set to zero ($I_o = 0$) to gurantee Critical Conduction Mode operation. Thus:

$$L_2 = L_1\frac{V_m sin\theta}{V_o} \tag{20}$$

From (20), the maximum inductance of L_2 when θ is at $\frac{\pi}{2}$ and V_o is constant.

Coupling Capacitances C_c

Finally, the capacitance of C_s as seen in Figrue (1)(A) is selected to reduce the ripple in the voltage V_{Cs}. Thus, it is given as follow:

$$\Delta V_{Cs}(\theta) = \frac{LeqI_{pk}^2}{2C_s}\frac{sin^2\theta}{1 + K_s sin\theta} \tag{21}$$

Normally, C_s must pass a high RMS current when it is compared with the output one. In one hand, for the low power SEPIC PFC, the RMS current which passes through the capacitor is relatively small. On the other hand, the voltage rating of the SEPIC capacitor must be higher than the peak of input voltage.

Control Loop and Zero Current Detection

The overall SEPIC PFC circuit is shown in Figure 1(A). To operate the PFC in CRM-COT, IC $LT3757$ is used [27]. The feedback voltage is directly connected to error amplifier through a voltage devider. The closed loop parameters are connected to compensation voltage V_c pin. The compensation loop parameters are selected to stabilized the load voltage loop by using RC circuit. Based on PFC controller datasheet, it is recomended to design a type II compensation network which has two poles and one zero. One of the poles is assumed to be infinity because it actually depends on equivelant output resistance of the error amplifier which is assumed to be very large resistance. Table 2 summarizes the design parameters.

To detect the zero current crossing point, L_2 is grounded by a senseing resistance. the switch M is turned on when the inductor current I_{L2} crosses the zero. Actually, the voltage across R_{sens} is zero.

Table 2. Selection of a cloosed loop parameter.

Ploe/Zero	f range [KHz]	Depends on	Selected values
$Zero1$	0.144 - 67.7	R_c, C_{c1}	$f_{z1} = 1.5$K $R_c = 10.5K\Omega$, $C_{c1} = 10n$F
$Pole2$	3.2 - 3200	R_c, C_{c2}	$f_{p1} = 30.3$K, $C_{c1} = 500p$F

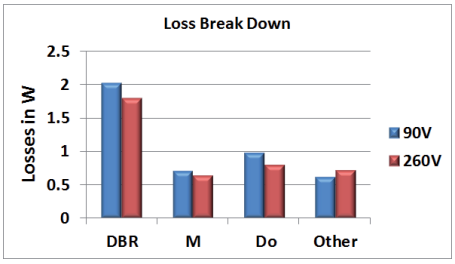

Fig. 4. Loss Break Down for SEPIC PFC.

Power Losses

There are three types of losses in the SEPIC PFC; conduction, switching and control losses. To calculate the losses in the circuit, the equations in [24] and [25] are used.

Figure 4 shows the loss break down of the SEPIC PFC at low (blue) and high (red) line voltages, respectively. As seen in the figure, the DBR has the highest loss contribution. This is related to the forward voltage V_f of the diode in the bridge rectifier.

The MOSFET M has the total losses shown in separated columns. Somehow, the losses in the MOSFET are close to each other in both cases of the line voltages. The diode D_o has more contribution than the losses in the selected MOSFET M. Finally, the losses labeled by $other$ in Figure 4 are related to the losses in the internal DC resistances of the selected inductors L_1 and L_2.

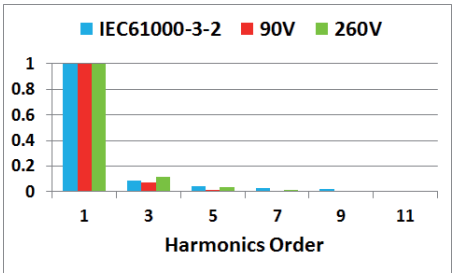

Fig. 5. Harmonics content in the input current.

Experimental Results

The experimental results have been conducted based on LTSPIC software. This software offers real simulation of different components. It is produced by simeconductor manufacture *Linear Technology*.

SEPIC PFC Specifications

The circuit specifications are: $P_{out} = 30$ Watt, $V_{out} = 15$ V and $R_o = 7.5\ \Omega$. This circuit was tested under the universal line voltage 90-260 VRMS voltage. The selected components in this simulation are shown in table 3.

Waveforms Analysis

Obvously, from Figure 6, the load voltage is 15 V DC for both line voltages. Moreover, it is clear that the line current in Figure 6 is for high line voltage. Furthermore, the line current in both cases has a sinusoidal envelope as expected. As seen in Figure 7, the turn on instant of the switch M happens when the drain current $I_{d,M}$ is nearly zero. Hence, the switch M is

Table 3. The Selected Components for SEPIC PFC.

Component	Value
DBR	4*$RFN2L4S$
$L1$	47uH
$L2$	52uH
$MOSFET$	$IPB65R420CFD$
C_c	1uF, 400V
D_o	$RFN2L4S$
C_o	110uF
PFC controller IC	$LT3757$

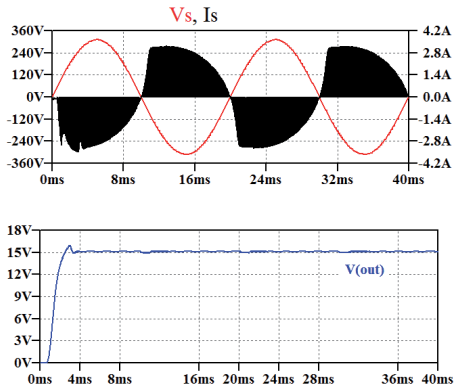

Fig. 6. Line voltage, line current and output voltage, at high input voltage.

turned on under zero current switching (ZCS). Accordingly, the switching losses in the circuit are reduced.

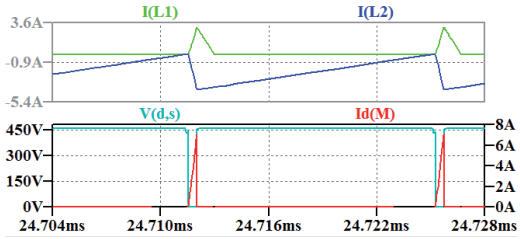

Fig. 7. Inductor L_1 and L_2 currents, switch voltage and current.

Power Factor and Total Harmonics Distortion

Table 4 compares the power factor of the circuit in both line voltages. However, in both cases it exceeds 99%. The total harmonics distortion is in the range between 2.5% and 13.57% for low and high line voltages, respectively. Moreover, Figure 5 shows the harmonics contents in the input current. Noticeably, the harmonics contents are accepted according to IEC61000-3-2 standard.

Efficiency of the Circuit

The efficiency of the designed SEPIC PFC is shown in Figure 8. The efficiency increases when the line voltage rises. The efficiency of the circuit is 86.1% at low line voltage up to 89.9% at high line voltage. The fact behind the increased efficiency is that the Constant On Time decreases when the line voltage increases. So, the On Time is $1.88\ \mu$ sec when

the RMS line voltage is 90 V. Whereas, it is decreased to 0.43 μsec when the RMS line voltage is 260 V. See (9).

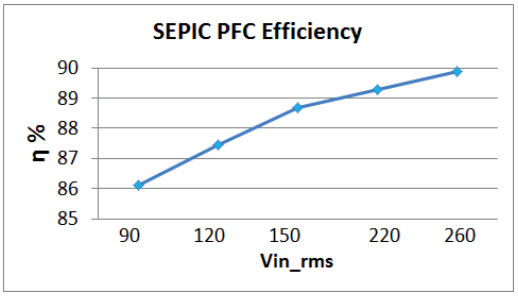

Fig. 8. A 30W SEPIC PFC efficiency.

Table 4. Summury of Simulation.

V_{rms}	90V	260V
T_{on} usec	1.88	0.43
PF %	99.79	99.1
THD %	2.5	13.57
η %	86.1	89.9

Conclusion

In current paper, Single Ended Primary Inductor Converter Power Factor Correction (SEPIC PFC) has been designed and investigated. The power ciruit is designed to supply a 30 W, 15 V to be used as lab tops and mobiles chargers. The SEPIC PFC is operating in Critical Conduction Mode (CRM) with Constant On Time (COT) to achieve ZCS of the power switch.

The simulation results have been verified using LTSPICE software. The efficiency of the circuit reaches 90% at high RMS line voltage. Whereas, the power factor of the line current maintains more than 99% over the line voltage. Accordingly, the Total Harmonics Distortion (THD) is 13.57% at high line voltage and it decreases to 2.5% in case of low line voltage. Table 4 summurizes the results.

Authors: *Dr. techn. Khaled A. Mahafzah, M. Sc. Qais Al Azzam, Ph.D. Ibrahim Altawil,*
Department of Electrical Engineering,
Medium Voltage Networks Department,
Department of Electrical Power Engineering,
Amman, Jordan,
Corresponding Author: Khaled A. Mahafzah, email: k.mahafzah@ammanu.edu.jo,

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