

Design of 8T SRAM using 14nm FINFET Technology

Abstract: FinFETs are superior to CMOS because of their low power consumption and ability to function at low voltage. The power consumption of today's digital systems has grown due to an exponential increase in transistor count. Furthermore, due to short channel effects, the performance of typical CMOS devices degrades at lower technology nodes. In sub-14 nm technology, FinFETs have greater control over a gate and outperform CMOS designs. FinFET devices feature a greater Ion current and better extensibility than typical CMOS devices. The quasi planar FinFET structure's simple production technique drew a lot of attention. Static leakage current is decreased by up to 90%, and it is more compact. Because of its area of performance, reduced leakage power, intra-die variability, and lower retention voltages, it is employed more than other FETs in SRAM cell design. In this work, an 8-bit SRAM is built and made in FinFET 14nm, the time delay for read and write operations are computed, as well as the leakage power for the design, and the performance is compared to existing technology.

Streszczenie. FinFET są lepsze od CMOS ze względu na niski pobór mocy i zdolność do pracy przy niskim napięciu. Zużycie energii przez dzisiejsze systemy cyfrowe wzrosło z powodu wykładniczego wzrostu liczby tranzystorów. Ponadto, ze względu na efekty krótkich kanałów, wydajność typowych urządzeń CMOS spada w węzłach o niższej technologii. W technologii poniżej 14 nm FinFET mają większą kontrolę nad bramką i przewyższają konstrukcje CMOS. Urządzenia FinFET charakteryzują się większym prądem jonów i lepszą rozciągliwością niż typowe urządzenia CMOS. Prosta technika produkcji quasi-planarnej struktury FinFET przyciągnęła wiele uwagi. Statyczny prąd upływu jest zmniejszony nawet o 90% i jest bardziej kompaktowy. Ze względu na swój obszar działania, zmniejszoną moc upływu, zmienność wewnątrz matrycy i niższe napięcia retencji, jest on stosowany częściej niż inne tranzystory FET w projektowaniu ogniw SRAM. W tej pracy zbudowano i wykonano 8-bitową pamięć SRAM w technologii FinFET 14nm, oblicza się opóźnienie czasowe dla operacji odczytu i zapisu, a także moc upływu dla projektu, a wydajność porównuje się z istniejącą technologią. (**Konstrukcja 8T SRAM przy użyciu technologii 14nm FINFET**)

Keywords: FinFET SRAM, Static leakage current, CMOS, Subthreshold leakage.

Słowa kluczowe: pamięć SRAM, technologia CMOS,

Introduction

Due to short channel effects, scaling technology has limited the working of Complementary Metal Oxide Semiconductor (CMOS) designs, necessitating the use of post-silicon devices. FinFET has control over the gate in sub-14nm technologies, outperforming CMOS designs. Furthermore, FinFET devices scale better than bulk CMOS. FinFET stands for Fin Type Field-Effect Transistor [1]. It is a switching device, like a MOSFET (Metal Oxide Semiconductor Field Effect Transistor). FINFET, on the other hand, is not a planar and has a three-dimensional structure. The channel is surrounded by several gates. This design will help in the reduction of a variety of short channel effects such as DIBL, sub threshold leakage, and so on. It has a higher I_{on}/I_{off} ratio. FinFETs can be short-gated or independent-gated [2]

SRAM (Static Random Access Memory) memory is the significant key segment in scaling down CMOS technology due to its high demand. For both read and write operations, a standard cell involves six transistors [3]. It can save space. In this situation, the BL functions as an In-Out line, suggesting that read and write may be achieved with one B_L [4]. Though logic may be made stable, extra hardware, such as a sense amplifier, is required. As a result, the read output is erratic. An 8-T SRAM with one B_L is also works. The reasoning, however, cannot be kept in a good state [5].

It can be accomplished in a variety of ways. While writing and reading, bit-line charges must be released. As a result, issues with data retention develop. To circumvent this, reading and writing activities are carried out on different lines [6]. The operations are done without interruption once the appropriate lines are activated. As a result, today's SRAM cells employ 8T and 9T designs. The operation speed and power consumption decrease as the channel length decrease. The transient analysis is performed on CMOS 180 and 45 nm platforms [7].

The suggested existing circuit is tested by simulating it, and the circuit is subjected to transient analysis. The current circuit is made up of eight transistors. The primary purpose is to obtain the read. This is a Single bit cell (SRAM).

Only single bit can be read and written at a time [8]. The suggested circuit in this study employs eight transistors. The output acquired using the existing circuit is compared to the output obtained using the proposed circuit. When studying logic "1" it was determined that the current circuit has 900 mV. This issue is much minimized when a transient investigation of the proposed circuit with equal length and width parameters is performed [9]. This circuit eliminates the issue of altering the width requirements. For the same width, the projected output may be achieved by the specified circuitry. The simulation tool is Cadence virtuoso. [10]

The main problem with normal SRAM is that it employs large-scale technology in its design in order to achieve smaller size with lower supply voltage and less variance in source potential. The discrepancy becomes more unstable as the design need raises the count of devices with small in size to administer greater occupying spaces. The design of an SRAM is governed by its stability, as well as the consuming power and time taking necessary to read or write with a cell.

In various schematics, improved and updated technologies are commonly used to minimize the power taking while in the changeover state and also in the on and off state, and updated methods are used to speed up the operation. The multi-gate voltage FINFET technique is most likely the greatest solution for reducing power consumption while boosting switching speed.

FinFET SRAM is the greatest way to provide a 14nm-sized transistor design with modern VLSI technology to compensate for the need for a superior storage system. The conventional transistor design will confront several short channel issues that can be totally eliminated by the current FinFET design.

In contrast to typical MOSFETs, FinFETs do not have arbitrary dopant fluctuations. After comparing with the FinFET circuits, CMOS has a greater supply voltage and fewer energy and product delay points, resulting in voltage stability with FinFET. At the same time, SRAM may suffer from the existing in high amount of small size cache

memory in the chip area, and the chip consuming power uses the most energy. The design and simulation of the 8T SRAM cell using 14 nm FinFETs is performed using Cadence Virtuoso Tools.

Design and Theory
Conventional 6T SRAM

One of the issues with 6T SRAM is that logic-0 recorded during the read may simply be overwritten by logic-1 when the voltage at node V₁ reaches the V_{th} of NMOS N₁ to bring node V₂ down to logic-0 and even pushes node V₁ up to logic-1 due to positive feedback [11]. As a result, when the cell changes state, the reading operation produces an unexpected result. The current generation of 8T SRAM has six transistors for write operations and two transistors for reading operations [12]. To accomplish the

read function, two NMOS transistors are coupled in series in this setup. The 8T SRAM is seen in Figure 1 [13].

The Read_write logic is connected to the gate of the NMOS transistor, allowing the read operation to take place. One disadvantage of the circuit is that any variation in the voltage stored in QB is replicated at the RBL output [14]. Figure 1 depicts an 8T SRAM cell. The logic circuit is unable to restore to its initial condition. Although altering the width of the transistors would partially fix the circuit, it will have an effect on the total area, which will continue to expand [15]. When the present circuit is developed and transient analysis is performed, the strong logic-0 and logic-1 outputs cannot be produced when reading bits from memory. This research proposes a novel 8T SRAM architecture that eliminates the aforementioned limitations of 7T SRAM Cell [16].

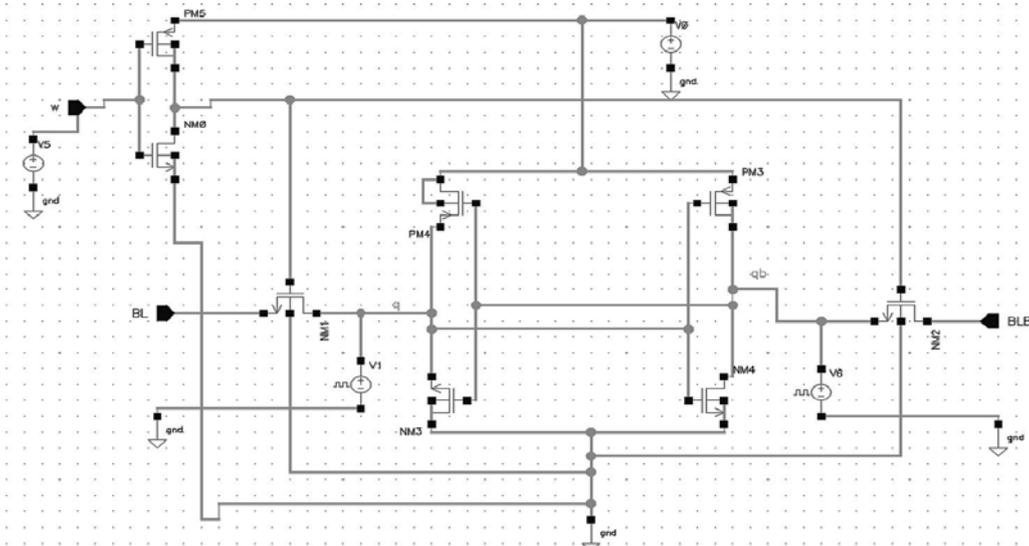


Fig.1 8T SRAM using 14nm FinFET Technology-Read circuit

8T SRAM Cell Design In 14nm FinFET

As illustrated in Figure 1, the recommended SRAM cell has 8 transistors, NM0-NM4 and PM3-PM5. Four transistors NM3, NM4, PM3, and PM4 form a Latch setup to keep data, which will remain in the loop until accessed. The internal nodes Q and QB are accessed by two transistors NM1-NM2. NM1 and NM2 connect the cell's internal nodes Q and QB [17]. PM5 and NM0 work together to generate an inverter that regulates node C's voltage, while NM1 and NM2 connect the cell's internal nodes to the bit_lines, where Q and QB nodes play a key role in reading and write operations, PM5 and NM0 work together to generate an inverter that regulates node C's voltage, and NM1 and NM2 connect the cell's internal nodes to the bit_lines. This is always pre-charged to V_{dd} when bit_line and bit_linebar are utilized in reading operations. The CS line is linked to PM3 and PM4 source terminal, while the WL line is connected to PM5's and NM0's gates. The origins of PM3 and PM4 are different from typical designs [18]. The source of PM3 and PM3 are connected to a dynamic V_{DD} line, which is boosted to a greater voltage during a read operation to provide a greater noise margin, in contrast to the standard design [19] with 14nm FinFET technology in Cadence Virtuoso.

Results and Discussion

Read operation

For read operations to be performed, always the word_line in SRAM must be raised high. Memory must initially hold some value to conduct a read operation. Take into consider memory with Q=1 and QB=0 as an example. Increases the word line into a high to complete the read

procedure. With a node voltage of V_{DD}, the output lines bit and bit_b is first pre-charged. Because Q and B_L are both high, there will be no drop in the circuit. There will be a potential difference between Q" and also at the node voltage at bit_b for Q=0 and bit as high, resulting in a drop in bit b voltage. As a result, the current will flow and the circuit will discharge. The sensing amplifier is linked to bit and bit_b; it functions as a comparator; thus, the output is 1 when the bit is low. As a result, when Q=1 was used as an input, the output was 1.

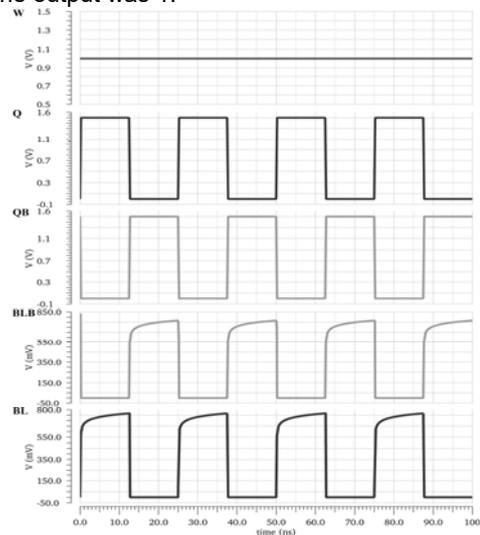


Fig. 2. Output and control signals of Read Operation.

Write Operation

At the beginning of a write cycle, the logic to be written is kept on the bit_lines. To place a 0 on the bit_line, set the bit_linebar to 1 and the BL bar to 0. To make a 1, the bit_lines' values are reversed. After the value to be stored is passed in. The bit_line input drivers are intended to be significantly more powerful than the cell's relatively weak transistors, allowing them to easily overcome the prior state of the cross-coupled inverters. write is substantially easier than the read in the suggested architecture. While the WL

is being dragged down, the writing operation begins by rising to V_{DD} . One BLS is being dragged to the ground, and the other is being held at V_{DD} . When the node is powered on, NM3 and NM4 are charged to V_{DD} [24]. When node C is charged to V_{DD} , both NM3 and NM4 are charged. When NM3 and NM4 are activated, input data is copied into memory, in the same manner, it would be in a conventional 8T SRAM [25].

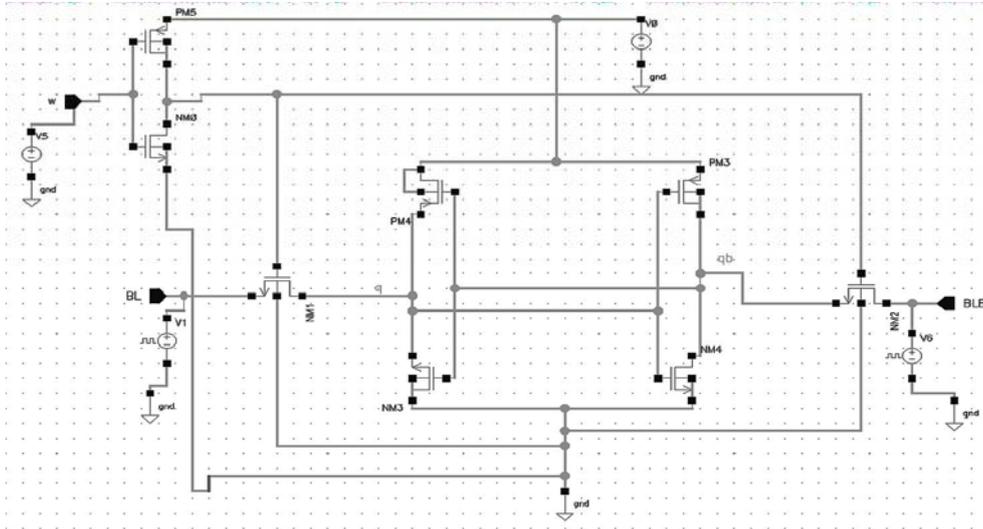


Fig. 3. 8T SRAM using 14nm FinFET Technology-Write circuit

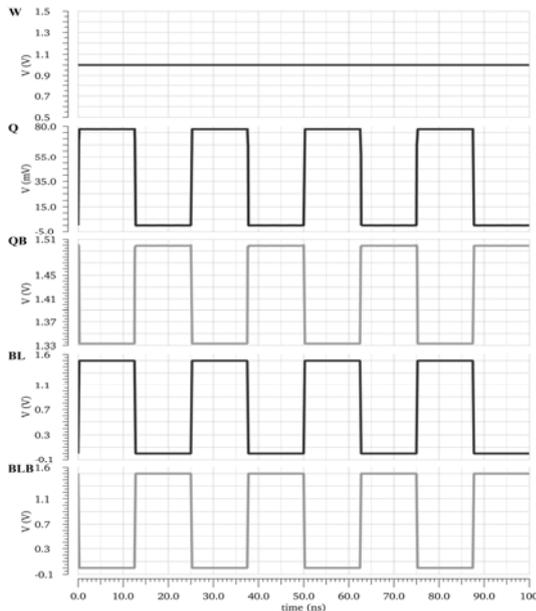


Fig. 4. Input and control signals of Write Operation.

Table 1: Performance Comparison between CMOS 180nm and 45nm SRAM cells and 8T SRAM Cell with FinFET 14nm technology

Parameter	CMOS 180 nm [20]	CMOS 45 nm [21]	Proposed FinFET 14nm
Leakage Power	27.26 μ W	67 μ W	1.036 μ W
Read Delay	77.8 ps	28.6 ps	6.3 ps
Write Delay	6.5 ns	749.47ps	74.16 ps

Time delays have been reduced in comparison to existing SRAMs. Table 1 displays the power leakage for multiple 8T SRAM technologies. FinFET has the least leakage power when compared to CMOS 180 and 45nm

technologies, and also shows read and write delays FinFET-based SRAM has better values compared to others.

Conclusion

This study describes the design of an 8T SRAM cell in 14nm FinFET. The design was completed by demonstrating consistent output recovery on write and read operations. This study also includes a thorough assessment of two standard 6T and 8T SRAM cells based on numerous well-investigated FinFET devices in the 14nm region.

Furthermore, delays have been studied and compared to earlier models, and 8T SRAM cells employing 14nm FinFET technology are stable for read operations, which was not the case in the previous designs like in 6T and 7T SRAM Cell. For CMOS and FinFET technology, the leakage power for this recommended design has been evaluated.

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