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Efficiency optimization of totem pole PFC with Gallium Nitride semiconductors

Abstract. *Novel Gallium Nitride wide bandgap semiconductor devices are capable of improving efficiency of power converters. This article presents a practical optimisation of GaN converter application in the totem-pole power factor conversion converter. As the bottom side cooled devices are used, the article shows integration of switching device and gate driver on a single insulated metal substrate board, attractive for high power density power supply solutions. Measured efficiency data together with analysis of losses distribution and optimization at specific operating conditions are included. Design files of printed circuit board, created in free tool KiCad, used for evaluated prototype are part of this publication.*

Streszczenie. *Nowatorskie urządzenia półprzewodnikowe z azotkiem galu o szerokiej przerwie energetycznej są w stanie poprawić wydajność przekształtników mocy. W artykule przedstawiono praktyczną optymalizację zastosowania konwertera GaN w przekształtniku konwersji współczynnika mocy. Ponieważ stosowane są urządzenia chłodzone od spodu, artykuł przedstawia integrację urządzenia przełączającego i sterownika bramki na pojedynczej izolowanej płycie z metalowym podłożem, co jest atrakcyjne dla rozwiązań zasilających o dużej gęstości mocy. Uwzględniono dane dotyczące zmierzonej sprawności wraz z analizą rozkładu strat i optymalizacją w określonych warunkach pracy. (**Optymalizacja wydajności przekształtnika PFC z półprzewodnikami z azotku galu**)*

Keywords: power electronics, GaN, GaN totem pole, GaN efficiency optimization, GaN cooling, GaN on insulated metal substrate IMS.
Słowa kluczowe: pr\ekształtnik, azotek galu, warunki chłodzenia.

Introduction

Rising demand for power in many industries, especially automotive, lighting and server/telecom requires innovative technology steps to make the growth sustainable. On one hand, development of carbon-dioxide free/environmentally friendly energy sources to cover the rising demand for electricity, on the other hand pushing for improvement of existing solutions to make them more effective, therefore less energy demanding.

Novel semiconductor wide bandgap devices using new materials, as Silicon Carbide and Gallium Nitride, have capability to increase efficiency of power converts in industries named above. The aim of this article is to present an optimized efficiency power factor correction converter using Gallium Nitride semiconductors in the totem pole configuration, with synchronous rectification in the low-speed branch.

Hardware description

As the majority of nowadays produced electronic devices have to contain power factor correction, the totem pole topology suitable for middle range power is used. GaN Systems GS66516 e-mode power HEMT is used for high-speed switching branch (Fig.1-Q1,Q2), combined with Silicon Laboratories driver SI8271 suitable for e-mode GaN driving voltage levels. The bias for both, high and low side driver, is galvanically isolated over a minimized interwinding capacitance transformer. To reach the maximum switching speed, an optimization of driving paths, together with implementation of negative driving voltage is necessary. The driver configuration is designed differently in comparison with GaN MOSFET manufacturer. The gate drive resistors values are optimized (R_{on}=4.7Ohm, R_{off}=0Ohm) what leads to a significantly increased switching speed.

Major challenge of designing with GaN is the low inductive layout and a good cooling of minimized surface mount packages. Packages are typically available in top and bottom cooling versions, based on the location of the cooling pad. As the top side cooled devices are not very practical in terms of production process, bottom side cooled devices are usually the case seen in many applications. To use the best available technology to resolve the cooling challenge and gain the maximum performance of semiconductors, the dual-layer insulated metal substrate (IMS) board is used where the substrate is made of copper base material. The stack-up of IMS board contains optimized thermal vias bridging the middle layer [9], to improve overall thermal performance.

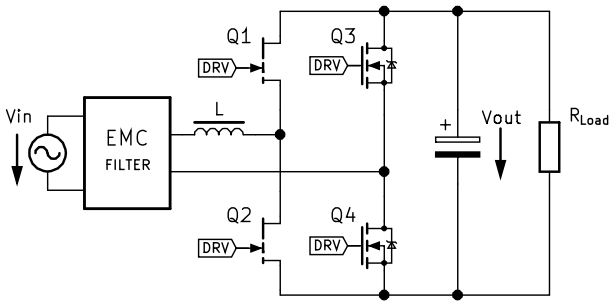

Fig. 1. Simplified schematic of Totem-Pole PFC converter

Single sided SMT board is subsequently adhesively coupled with thermal conductive interface to an aluminium heatsink. Thermal resistance case-heatsink with the optimized IMS equipped with a basic high voltage prepreg-core material reaches $R_{\vartheta c\text{-}h}$=0.81KW^{-1} (Fig.2). The design of the heatsink is obviously depending on the respective ambient conditions.

Fig. 2. Tested protype – isolated metal substrate board with GaN (GS66516B) half-bridge and insulated gate drivers

Low inductive design of switching loops with high di/dt is essential to avoid overvoltage stress of the switching devices and potential EMC problems. By using a special manufacturing process, the metal part of IMS (1.5mm thick copper plate) can be connected to ground (Fig.3). Placing vias between top two layers and substrate in respective nodes, results to minimized parasitic inductance in the switching loop without significant layout effort and space constraints. In addition, the base plate is connected to the "silent" node, which can provide shielding function for other circuits in the device and improve performance in radiated electromagnetic spectrum.

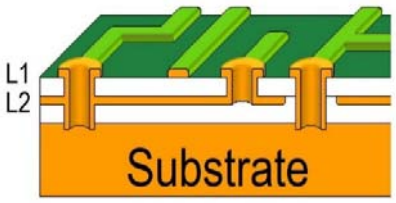

Fig.3. Stack up of PCB used for prototype (cross section)

The drawback of this solution is an increased capacity of the switch node to the ground plane, which creates additional switching losses. In the demonstrated prototype, the capacitance between switching node and the substrate of the board reach 57pF, resulting in power loss 0.64W at 70kHz (400V bus voltage), which was proven to be acceptable. The base material used to build the stack up is the ceramic-filled epoxy laminate 92ML, with thermal conductivity 1.6Wm^{-1}K^{-1} in Z direction (10x more than FR4). Since the e-mode FET drivers are single channel types, it is necessary to add an interlock circuit to make sure that two switches will be never driven high at the same time, especially during high dv/dt input transitions (like surge).

Optimization process

To ensure reliable operation of the system we can assume that the power module is typically loaded at 50% of nominal power during its lifetime. This is the common case in server applications, where redundancy is essential characteristic and the power modules are operated mostly in parallel configuration. Therefore, the goal is to optimize efficiency at half load. The way to achieve this target is to reduce the converter losses ΔP at this condition:

$$\Delta P = \Delta P_M + \Delta P_L + \Delta P_{AD} \quad (1)$$

where ΔP_M are power stage losses, ΔP_L are inductor losses and ΔP_{AD} are additional losses. Additional losses include the rest loss-components: conduction and capacitive losses in PCB, input filter, control circuit power consumption together with gate driving losses. As the input filter and the control circuits design might vary based on application requirements, the focus of this study is the power stage and inductor losses.

Power stage losses ΔP_M are defined according to the following expressions:

$$\Delta P_M = \Delta P_{R_{GaN}} + \Delta P_{SW_{GaN}} + \Delta P_{R_{Rect.}} \quad (2)$$

$$\Delta P_{R_{GaN}} = R_{DSon,GaN} \cdot I_{GaN,RMS}{}^2 \quad (3)$$

$$\Delta P_{R_{Rect.}} = R_{DSon,Rect} \cdot I_{Rect,RMS}{}^2 \quad (4)$$

Where $\Delta P_{R_{GaN}}$ represents conduction losses in GaN devices (Fig.1-Q1,Q2), $\Delta P_{R_{Rect.}}$ are conduction losses in synchronous rectifier (Fig.1-Q3,Q4). The currents $I_{GaN,RMS}$ and $I_{Rect,RMS}$ in (3) and (4) are integrated over half period (T/2) of line voltage, as the duty cycle and the amplitude of the current are time dependent.

Switching losses $\Delta P_{SW_{GaN}}$ are present only in one device in half-bridge during half period of line voltage (Fig.1-Q2 for the positive Vin, Q1 for the negative Vin) as the opposite device is commutated by load current, therefore operating in Zero Voltage Switching mode.

Tab. 1. Available GaN devices

Manufacturer part number	Declared R_{DSon} @ 25°C	Cooling plate
VisIC V22N65A	22mΩ/650V	Top
GaN Systems GS66516B	25mΩ/650V	Bottom
Infineon IGO60R070D1	70mΩ/600V	Top/Bottom

As bottom side cooling was preferred and minimized IMS board size was the target, GS66516B device was chosen due to the best overall match (Tab.1). The active synchronous rectification in low speed branch (Fig.1-Q3,Q4) utilize Silicon MOSFETs with cost-performance balanced channel resistance (22mΩ) instead of passive diode rectifier, which reduces conduction losses significantly.

The most significant advantage of GaN semiconductors is the fast switching speed, where they outperform the Silicon competitors with remarkable difference. Switching losses are defined according to (5)-(7).

$$\Delta P_{SW_{GaN}} = f_{SW} \cdot (E_{on} + E_{off}) \quad (5)$$

where:

$$E_{on} = \int_0^{t_{on}} u_{DS(t)} \cdot i_{D(t)} \cdot dt \quad (6)$$

$$E_{off} = \int_0^{t_{off}} u_{DS(t)} \cdot i_{D(t)} \cdot dt \quad (7)$$

Fig.4. Thermal camera picture of the power stage during operation at full power 3kW – GaN half bridge on insulated metal substrate board (left), synchronous rectifiers (middle) and photo of prototype (right)

Device manufacturers typically specify E_{on} and E_{off} dissipated during switching transients for specific conditions. These values can be scaled to actual operating conditions based on [8]. This method is used for estimation of power losses in the following chapter. Any inaccuracy in this estimation might lead to an increase of assigned additional losses during analysis and vice versa. Note, that any parasitic elements in the circuit might lead to voltage/current oscillations and increased switching losses. Therefore, the proper, low inductive, design of power path with short connection to low impedance bus capacitors is crucial.

Optimization of switching losses was done by tuning gate resistors of both GaN devices, while monitoring the gate-source and the drain-source voltages for possible problems related to high dv/dt transitions. Switching losses have been stepwise reduced up to the point where efficiency peak achieved level well over 99% while switching node voltage waveforms performed a clean and smooth transition without remarkable oscillations.

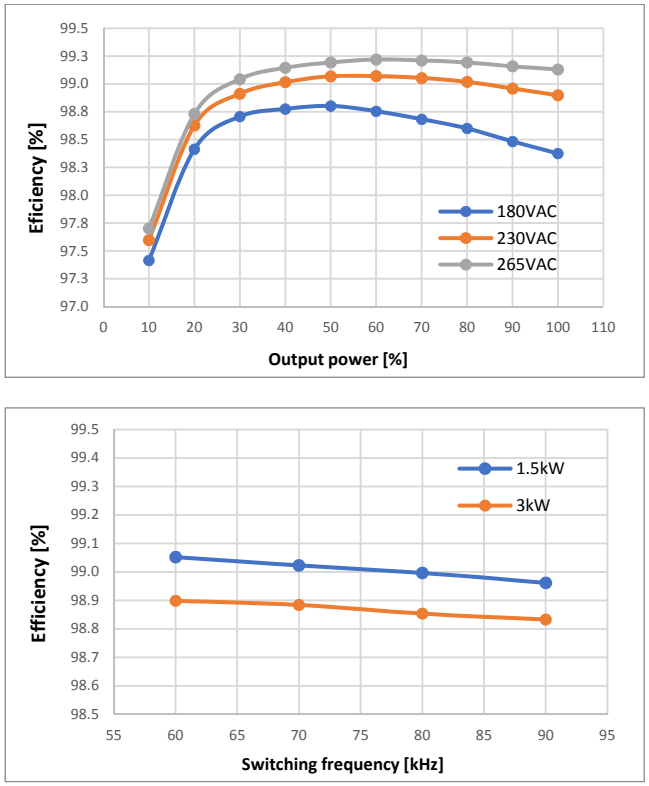

Fig.5. Efficiency curves of tested prototype for various input voltage and load conditions (at 60kHz - left) and various switching frequencies at nominal input voltage 230VAC (right). Both graphs show efficiency without auxiliary converter and input filter power loss, 100% of power equals to 3000W.

Inductor optimization

As the core and copper loss of inductor in totem pole topology is one of the major contributors to overall performance, the optimization of wire diameter, number of turns and core material for 50% load at nominal input voltage is necessary. Formula for conduction power losses:

$$R_w = f(\vartheta, N);\ i_{L(t)} = f(V_{IN,RMS}, P_{out}, N, t) \quad (8)$$

$$I_{IN,RMS} = \sqrt{\frac{2}{T}\int_0^{\frac{T}{2}} {i_{L(t)}}^2\, dt} \quad (9)$$

$$\Delta P_{Cu} = R_w . {I_{L,RMS}}^2 \quad (10)$$

where resistance of winding R_w is function of temperature (ϑ) and number of turns (N), while considering fixed area of window for selected core shape (copper fill factor 0.4). The RMS value of inductor current depends on output power and input voltage of the converter. The RMS current is also ripple dependent, therefore $L = L(i_L(t))$ is also taken account. Core losses are calculated using empirical formula provided by manufacturer of the core as a function of flux and frequency:

$$\Delta P_H = f(B, f_{sw});\ B = f(i_L(t), N) \quad (11)$$

core losses through half of the line period can be calculated:

$$\Delta P_{Core} = \frac{2}{T}\int_0^{\frac{T}{2}} V_e . \Delta P_H(B_{(t)}, f_{sw})\, dt \quad (12)$$

where V_e is total core volume, f_{sw} is switching frequency of the converter. Sum of formula (10) and (12) gives total power dissipation per inductor. The total losses of the inductor including its components are plotted on Fig.6. The plot is valid for typical operating conditions of the converter (230VAC, 50% load) and fixed switching frequency (f_{sw}=60kHz):

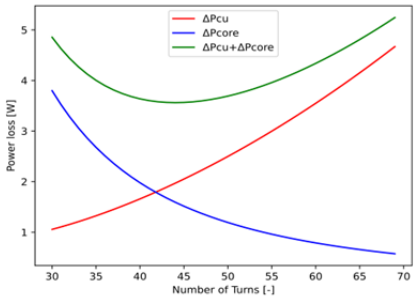

Fig.6. Total Inductor power losses vs. number of turns

Final design point use 40 turns and the core Changsung High Flux 43μ (2x).

Dead time and reverse conduction

During the deadtime between Q1 and Q2 conduction, the passive switch is shortly in reverse conduction while the gate voltage is still negative. For e-mode and GIT transistor structure is the source-drain voltage in reverse conduction mode directly depended on the Gate-Source bias [5]:

$$V_{SD} \sim (V_{TH} - V_{GS}) + I_{SD} . R_{SD} \quad (13)$$

where V_{SD} is the reverse drain-source voltage, V_{GS} is gate bias, V_{TH} is gate threshold voltage (~1.4V) and R_{SD} is off-state resistance in reverse operation. As the negative gate driving bias V_{GS} during off state is used in the optimized prototype, the reverse conduction losses are not negligible. For this reason, optimization of reverse conduction time is essential, with respect to variation of maximum/minimum propagation delay of the gate driver. Impact of optimization is well described in article [3] for a similar Gallium Nitride power transistor. Deadtime for tested protype is set to 50ns for rising and falling edge, which is visible on the Fig.8.

Measurement on prototype

Efficiency data displayed in Fig.5 were measured with calibrated power analyser Yokogawa WT3000. Input power is measured directly at totem pole input – in series with inductor. Output power is measured at bulk voltage, circuit is loaded with high voltage electronic load Chroma 63204. As the internal shunts of WT3000 are used to measure the current, voltage sense lines are connected in a way to exclude cable losses from the result. To avoid disturbance of connected instruments during voltage transient caused

by synchronous rectifier (zero crossing of AC voltage) and current flowing over capacity of connected instruments to Ground, a low pass filter is placed in series with electronic load. Input of totem pole converter is equipped with two stage EMC filter.

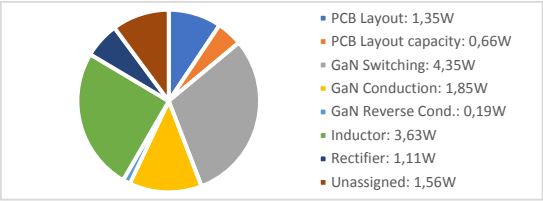

Fig.7. Power losses distribution at nominal operating conditions

To completely understand distribution of losses during operation of the converter, a mathematical model is created and losses are evaluated (Fig.7) with intention to compare the measured results. Difference between calculation and actual measurement is assigned to “Unassigned”. The difference might be caused by the measurement precision or a variance in actual components parameters vs. datasheet.

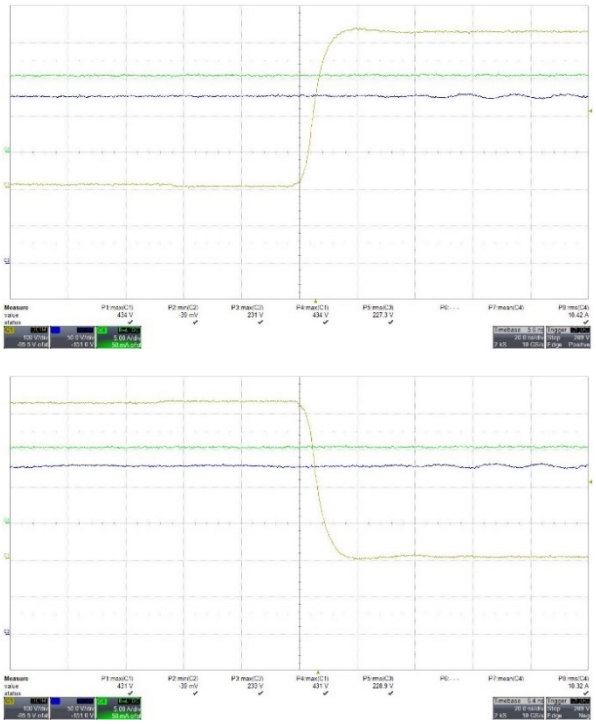

Fig.8. Switching waveforms during converter operation – drain-source of low side switch in totem pole configuration (yellow), input current (green) and bulk voltage sensed by differential probe (blue)

From losses distribution it is obvious, that even for GaN devices the switching losses are dominating. As in hard switching converts are losses linearly depended on operating switching frequency, further increase will lead only to lower efficiency, which is confirmed by measured data in Fig.5. Therefore, the choice of operating switching frequency depends on optimization criteria priority: efficiency versus power density. In this study the space for the inductor was given and the target was to maximize efficiency within the given space limitations.

Control

Presented converter is controlled by Texas instruments floating point DSP. Corresponding waveforms during operation at nominal conditions are captured on Fig.9.

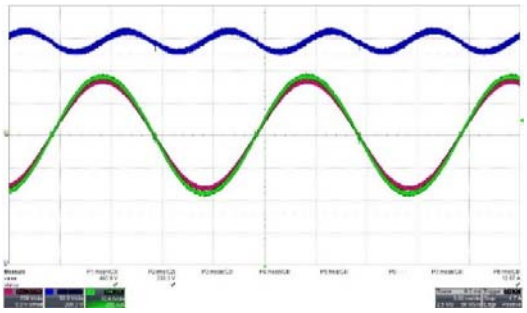

Fig.9. Input voltage, bulk voltage and the current waveform at nominal input voltage and 3kW output power (90kHz switching frequency)

Conclusion

Novel Gallium Nitride wide bandgap devices provides lower switching losses compared to Silicon counterparts. This article presents an advanced prototype using latest generation of GaN transistors from GaN Systems, using state of the art insulated metal substrate technology of printed circuit board, optimized for bottom side cooled surface mount packages. The IMS PCB provides at the same time high voltage basic isolation to the heatsink, which brings several advantages to the design.

The results clearly show that even CCM operated GaN converter achieves efficiency level of 99%, making it very competitive to the resonant topologies with the benefit of a simple control algorithm. These characteristics makes it attractive for 80 Plus Titanium certified AC/DC converters, where the overall power supply efficiency limit (including isolated DC/DC converter) is defined at >96% @ 50% load. Note that 80Plus Titanium mark in server/computer applications is requested by upcoming European union regulations. The printed circuit board (Fig.2), schematic and design files created in free PCB design tool KiCad are public and available at GitHub.com (repository name: PCB-GS66516B-IMS-HB).

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