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Design techniques in Carry Select Adder using Parallel prefix adder for improved switching energy

Abstract. *A new architecture of Carry select adder has been proposed with improved switching energy using parallel prefix adder. The conventional Carry select adder is the use of two Ripple Carry Adder (RCA) and a multiplexer. The findings in this work are the replacement of one RCA block by Brent Kung adder and the other RCA block by excess-1 converter. Simulation results show that the proposed Carry select adder is proved to have improved switching energy when compared with the other adders in 45nm CMOS process.*

Streszczenie. *Zaproponowano nową architekturę sumatora Carry Select z ulepszoną energią przełączania przy użyciu równoległego sumatora prefiksów. Konwencjonalny dodatek Carry Select wykorzystuje dwa Ripple Carry Adder (RCA) i multiplekser. Wyniki tej pracy to zastąpienie jednego bloku RCA sumatorem Brenta Kunga, a drugiego bloku RCA konwerterem nadmiaru-1. Wyniki symulacji pokazują, że proponowany sumator Carry Select ma lepszą energię przełączania w porównaniu z innymi układami w procesie 45 nm CMOS. (**Techniki projektowania sumatora Carry Select wykorzystujące równoległy prefiksowy dodatek w celu poprawy energii przełączania**)*

Keywords: Brent Kung Adder, Carry generation, Carry Select Adder, Generation stage, Parallel prefix adders, Pre processing stage
Słowa kluczowe: sumator Carry Select, RCA – Rip[ple Carry Adder

Introduction

The digital design depends on the three aspects. They are area, power and delay. In a conventional or standardized adder, the sum bit relies upon the sum generated out of the preceding bit and carry generated is circulated to the upcoming bit position[1-2]. Due to the presence of generation of the carry, there occurs a limitation in speed causing a major effect in this field. Ripple carry adder comprises of full adder blocks. Therefore, addition operation is performed with the usage of full adders in order to generate sum and carry. As the carry ripples throughout all the stages, it is termed as Ripple Carry Adder (RCA).

A conventional or regular CSLA is designed with a couple of multiplexer and ripple carry adders[2-3]. The ripple carry adder is designed to provide sum and carry outputs.The multiplexer determines the final sum and carryout bits when C_{in} is known. Addition can be performed in RCA by considering C_{in}=0 or C_{in}=1. However, in the conventional CSLA the area occupied was large, as it required two ripple carry adders to generate sum and carry. To improve the switching energy,conventional CSLA is replaced with the proposed CSLA structure by using parallel prefix adders to achieve less area, power and delay.

Hence there is a need to modify high speed adder by replacing RCA with parallel adder configuration. As reported in the literature survey, it is noticed that the performance of Brent Kung adder was better and utilizes less area. The Brent Kung adder can be used in multiplier and other data path elements.

Conventional Technique

The Carry Select Adder usually comprised of two n-bit parallel adders (ripple carry adders) and a multiplexer. Addition is organized with two n-bit parallel adders to calculate the sum and carry. The carry input is given as logic'0' and logic '1' to the RCA. The Multiplexer determines the sum and carry output based on the known carry input.Among all the adders, RCA has smaller area with more propagation delay. The Carry Skip Adder (CSA) is designed with a scheme to reduce the propagation delay.The Carry Look Ahead Adder (CLA) eliminates the ripple effect. Hence, CLA speed is more when compared with RCA. The carry bit ripples throughout the adder block in the RCA.Therefore, CSLA provides a solution for this linear dependency by using two carry-in inputs i.e., Cin=0 and Cin=1 and generate the result in a more advanced method. The final result can be received by multiplexer when the correct Cin value is known. The circuit diagram of conventional CSLA is shown in Fig.1. The CSLA is used in numerous digital applications to avoid the propagation delay.

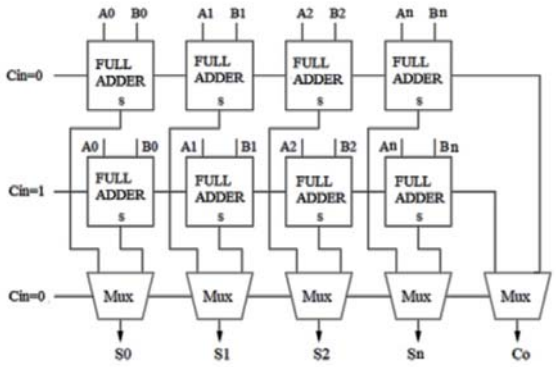

Fig. 1. Circuit diagram of Conventional CSLA [2] Carry Select Adder

CSA generally comprises of 2, n-bit parallel adders and a multiplexer.The multiplexer determines the ouput (sum and carry) when the Cin value is known.

Full Adder

Full Adder is an adder which comprises of A, B and C_{in} as input and two outputs (sum,Cout). Fig.2 shows the basic block of full adder.

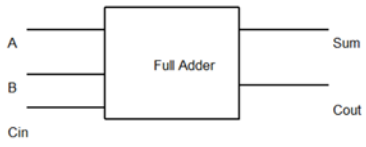

Fig. 2 Basic block of Full Adder

The full adder diagram is shown in Fig.3.

(1) Sum = A Xor B Xor C_{in}

(2) Carry = A.B + B.C_{in} + A.C_{in}

When the condition C_{in}=0,

(3) Sum = A Xor B

(4) Carry = AB

When the condition C_{in}=1,

(5) Sum = NOT (A Xor B)

(6) Carry = A Or B

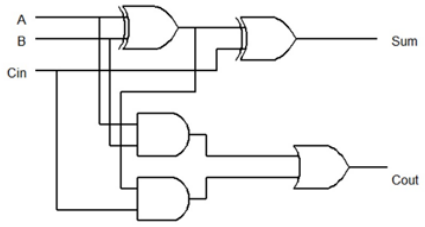

Fig.3 Logic Circuit of Full Adder

Ripple Carry Adder(RCA)

RCA consists of fulladders for adding n-bit numbers.Fig. 4 shows basic block of Ripple carry adder. The truth table of RCA is shown in Table 2.

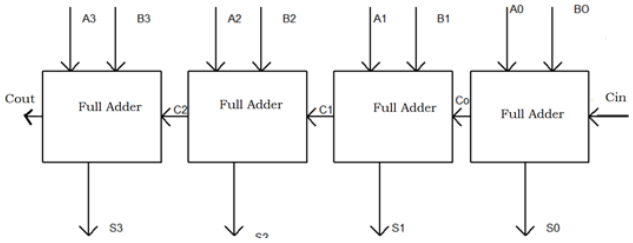

Fig. 4 Logic Circuit of Ripple Carry Adder

Table 2 Truth Table for Ripple Carry Adder

A3	A2	A1	A0	B3	B2	B1	Bo	S3	S2	S1	S0	Cin	Cout
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	1	0	1	1	0	0	0
1	0	1	0	0	1	1	1	0	0	0	1	0	1
0	0	1	1	1	1	0	0	1	1	1	1	0	1
0	1	0	1	1	0	1	1	0	0	0	0	0	1
0	1	1	0	1	0	1	1	0	0	0	1	0	1
0	1	1	1	1	1	1	1	0	1	1	0	0	1

Modified Csla Using Bk Adder

As discussed earlier, in the conventional or in the standardized CSLA the performance is not good as it has a pair of n-bit parallel adders to generate sum and carry bits [4-7]. To overcome this difficulty, conventional CSLA is replaced to modified CSLA structure by using parallel prefix adders to achieve less area, power and delay.

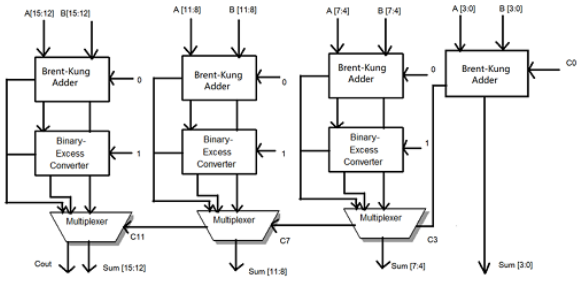

Fig.5 Block Diagram of CSLA with Brent-Kung Adder Brent Kung Adder

Parallel Prefix Adder

Parallel prefix adder is a fast adder which is used for increasing the speed in processor to perform addition operation[8-9]. Parallel prefix adder is similar to Carry Look Ahead Adder. Parallel prefix adders are designed for achieving high efficiency in many applications. The 3-main stages in parallel prefix adder include Pre-processing stage, Carry generation stage and Post processing stage [10-13]. The block diagram of CSLA with Brent-Kung Adder is shown in Fig. 5

Among the various architectures of parallel prefix adder, Brent Kung adder is better in its performance. It also comprises of n number of input and output stages. The area occupied in Brent Kung Adder is very less when compared with other parallel prefix adders. The propagating as well as generating cells is less in Brent Kung adder. Hence, BK adder can be designed for high speed computing applications. Fig.6 shows the post processing circuit. The primary stage is the pre-processing unit in which comprises of generate as well as propagate pointers that are received from the inputs. In the secondary stage the outputs of primary stage are fed as input and carry signals are generated. The ultimate stage is the post processing unit where the final result is attained from the secondary stage using carry signal and propagate a signal from primary stage.

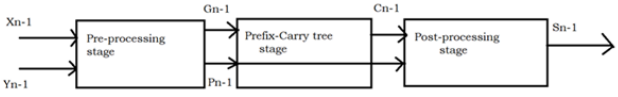

Fig.6 Block Diagram of Brent Kung Adder

Pre Processing Stage

The primary stage inputs are Ax and Bx and the outputs are Gx and Px.

(7) Gx=Ax . Bx
(8) Px= Ax Xor Bx

Carry Generation Stage

In carry generation stage, all the carry signals are obtained. This stage has 3 logic cells. They are Black-Cell, Gray-Cell, and Buffer Cell. The circuit may vary according to the number of inputs.

(9) Gx:y= Gx:z+ Px:zGz-1:y

(10) Px:y = Px:zPz-1:y

Post Processing Stage

This is the ultimate unit in which the XOR function is employed between the propagate pointer and the output of carry pointer received from the secondary stage. The architecture of Brent-Kung adder is shown in Fig.7

(11) Sx = Px XOR Cx-1

(12) Cx = Gx + Px Cx-1 or Cx= Gx

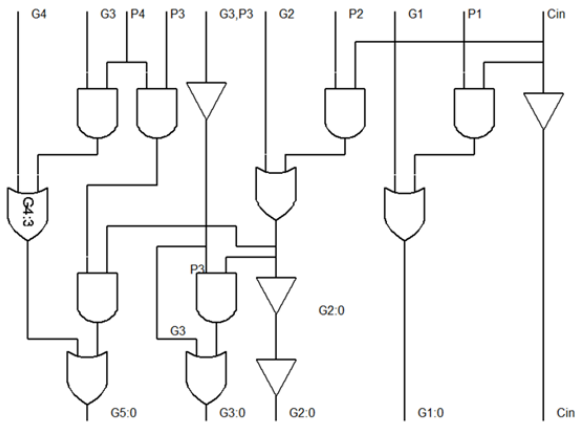

Fig. 7 Architecture of Brent Kung Adder

Binary to Excess-1 Converter

The modified CSLA is attained by changing the RCA with excess-1 converter and BK Adder. Binary to Excess-1 converter is very simple because it uses less logic and also provides area reduction when compared to RCA [14]. Table 4 shows the truth table for BEC.Fig.8 shows the BEC Circuit Diagram.

The equations for BEC conversion are given below:

(13) E0 = Not (B0)

(14) E1 = B0 Xor B1

(15) E2 = B2 Xor (B0 . B1)

(16) E3 = B3 Xor (B0 . B1 . B2)

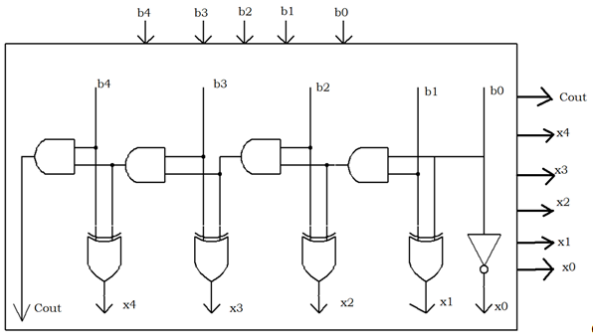

Fig.8 BEC Circuit Diagram

Table 4 Binary to Excess -1 Converter Truth –Table

Decimal Numerals	Binary Numerals	Excess-1 Output		
		Without carry	With carry	
0	00000	00001	0	00001
1	00001	00010	0	00010
2	00010	00011	0	00011
3	00011	00100	0	00100
4	00100	00101	0	00101
5	00101	00110	0	00110
6	00110	00111	0	00111
7	00111	01000	0	01000
8	01000	01001	0	01001
9	01001	01010	0	01010
10	01010	01011	0	01011
11	01011	01100	0	01100
12	01100	01101	0	01101
13	01101	01110	0	01110
14	01110	01111	0	01111
15	01111	10000	0	10000
16	10000	10001	0	10001
17	10001	10010	0	10010
18	10010	10011	0	10011
19	10011	10100	0	10100
20	10100	10101	0	10101
21	10101	10110	0	10110
22	10110	10111	0	10111
23	10111	11000	0	11000
24	11000	11001	0	11001
25	11001	11010	0	11010
26	11010	11011	0	11010
27	11011	11100	0	11100
28	11100	11101	0	11101
29	11101	11110	0	11110
30	11110	11111	0	11111
31	11111	00000	0	00000

Results and Discussion

The conventional CSLA and the modified CSLA using BK Adder are designed using Verilog. Simulation and synthesis of adders are done using Geneus Tool in Cadence . The output waveforms of conventional CSLA, RCA, BEC, BK adder and modified BK adder were obtained. Fig.9 shows the schematic of modified CSLA. Fig. 10 shows the output waveform of CSLA. Fig. 11,12,13 shows the power,delay and area obtained for CSLA

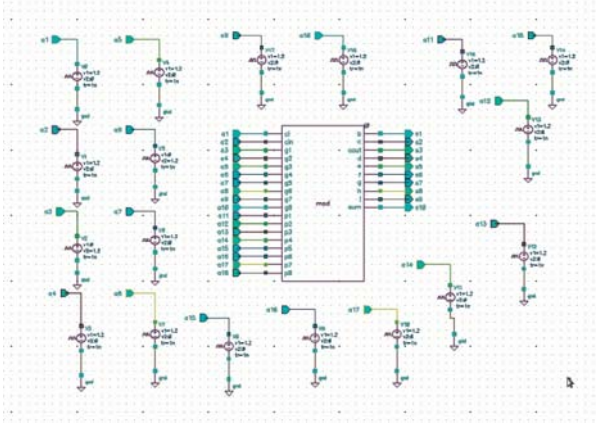

Fig. 9 Schematic of Modified CSLA

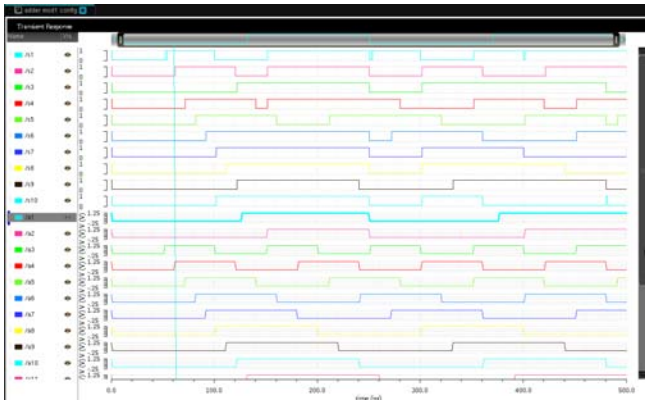

Fig. 10 Output waveform of modified CSLA

csla_timing1.rep | csla_power.rep | csla_gates.rep | csla_cell.rep

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution GENUS15.22 - 15.20-s024_1
  Generated on:           Mar 13 2020  03:15:30 pm
  Module:                 csl
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

                 Leakage   Dynamic    Total
Instance Cells Power(nW) Power(nW) Power(nW)
------------------------------------------
csl         14  926.491  5925.992  6852.483
  x1         1   86.962   241.510   328.472
  x2         1   84.476   452.468   536.944
  x3         1   84.476   524.822   609.298
  x4         1   84.476   567.989   652.465
  x6         1   84.476   673.455   757.931
  x7         1   84.476   563.292   647.768
  x8         1   84.476   664.907   749.384
  x5         2   61.760   359.322   421.082
  d1         1   54.182   133.136   187.318
  d2         1   54.182   274.994   329.176
  d3         1   54.182   269.367   323.549
  d4         1   54.182   188.896   243.078
  d5         1   54.182   161.336   215.518
```

Fig. 11 Output Power

```
Lint summary
 Generated clocks without clock waveform                    0
 Generated clocks with incompatible options                 0
 Generated clocks with multi-master clock                   0
 Paths constrained with different clocks                    0
 Loop-breaking cells for combinational feedback             0
 Nets with multiple drivers                                 0
 Timing exceptions with no effect                           0
 Suspicious multi_cycle exceptions                          0
 Pins/ports with conflicting case constants                 0
 Inputs without clocked external delays                     9
 Outputs without clocked external delays                    5
 Inputs without external driver/transition                  9
 Outputs without external load                              5
 Exceptions with invalid timing start-/endpoints            0

                                                  Total:   28
```

Fig. 12 Output Delay

Table 5 shows the Performance comparison of th modified CSLA. The BK adder is used to compute the carry for each stages.The carry bit and the propagate bit of the next stage is used to compute the sum of the current stage.

The power consumption of the proposed CSLA is very less when compared with the other types of adders. Simulation and Synthesis report shows that the designed CSLA reported improved power delay product in comparison with the other conventional adders.

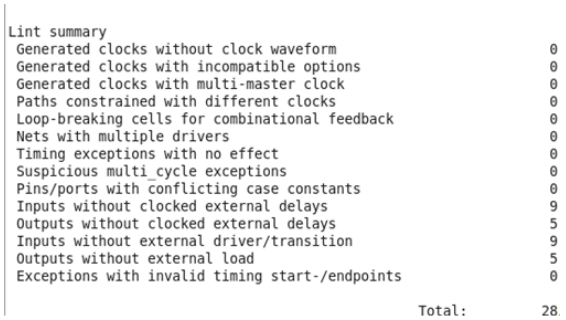

Fig. 13 Output Delay

Table 5 Performace comparision of the Conventional adders with the proposed CSLA adder.

CSLA STRUCTURE	Area (μm²)	Total Power (μW)	Delay (ns)	Power Delay Product (PDP) fJ
CONVENTIONAL CSLA	669	33.56	1.36	45.64
	978	54.29	1.76	95.50
	941	32	1.61	51.52
	634	61	2.45	149.40
MODIFIED CSLA	931	49.28	1.62	79.80
	842	29	1.45	42.05
	474	57	2.21	125.97
This Work	331	985.537nW	28	27.59

Conclusion

In this work, it is concluded that the modified CSLA structure has more advantage in terms of area reduction, power and rapid speed is attained through the parallel prefix structure.Therefore it can be determined that modified CSLA using BK adder is much better in terms of power and power delay product (switching energy) when related to other adder circuits.

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