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Relay Drive Circuits for a Safe Operation Order with a Digital Logic ICs Sequential Switching Function

Abstract. *This paper presented the fail-safe relay drive circuits with digital logic ICs sequential switching that the serial sequence was according to the ISO 13849-2 standard. The boost circuits increased voltage from five volts to 24 volts, in which the high voltage gain boost DC-DC converter circuit was derived from cascading a flyback converter and a boost converter with fail-safe capacitors. The reliability of the circuit was tested by failure mode and effects analysis (FMEA) for the adjustable speed electrical power drive systems (IEC 61800-5-2). This ensured that the designed circuit was fail-safe and without any dangerous failures. The circuit was tested with a computer simulation program and experimental circuit.*

Streszczenie. *W tym artykule przedstawiono bezawaryjne obwody napędów przekaźnikowych z sekwencyjnym przełączaniem cyfrowych układów scalonych, których sekwencja szeregowa była zgodna z normą ISO 13849-2. Obwody zwiększające napięcie zwiększyły napięcie z pięciu woltów do 24 woltów, w którym obwód przetwornicy DC-DC zwiększający wzmocnienie wysokiego napięcia został wyprowadzony z kaskadowania przetwornicy flyback i przetwornicy podwyższającej z bezpiecznymi kondensatorami. Niezawodność obwodu sprawdzono za pomocą analizy przyczyn i skutków awarii (FMEA) dla elektrycznych układów napędowych o regulowanej prędkości (IEC 61800-5-2). Zapewniło to, że zaprojektowany obwód był odporny na awarie i bez żadnych niebezpiecznych awarii. Układ został przetestowany za pomocą programu do symulacji komputerowej i układu eksperymentalnego. (**Obwody sterowania przekaźnikami zapewniające bezpieczną kolejność działania z funkcją sekwencyjnego przełączania cyfrowych układów scalonych**)*

Keywords: Fail-safe, 4-pin capacitor, open-fault, FMEA
Słowa kluczowe: przekaźniki, sterowanie, FMEA.

Introduction

The ISO 13849-2 series sequential safety relay drive design is one of the basic safety principles for driving a variable-speed electric motor. This safety basis requires a switching sequence of two series connected contact relays with a non-simultaneous switching sequence to avoid the normal failure of the relay contact fuse. The two serial relays circuit is connected at 1oo2(one-out-of-two), which the non-synchronous switching occurs when the fuse fails. As such, only one relay would be connected, while the other relay could also cut off the circuit by switching on-off at the same time. The fail-safe characteristics comprise: 1) The relay drive circuit must not provide an excitation signal to the relay in the event of a failure. 2) The relay's opening or closing delay must be greater than 0s [1]. A relay drive circuit consists of an oscillator circuit with a Schmitt trigger inverter, delay time with a linear regulator, and DC voltage boost with a transformer [1-5]. In the past article, the reliability was confirmed by a number of methods; such as, the sum of the failures [6], the mean time to failure [7], the failure of semiconductor devices [8], and failure mode and effects analysis (FMEA) [9].

This paper presented the design of safety relay drive circuits using logic diagrams replacing circuits with logic ICs to reduce the number of functions and devices used. The reliability was tested by FMEA for the adjustable speed electrical power drive systems. The designed circuit was fail-safe and without any dangerous failures. The circuit was also tested and verified with a computer simulation program and experimental circuit.

Design Concept

Principle of an electrical machine drive system in a safe operation order

A motor control circuit would cut off the power to the motor in the event of any fault in safety-related applications. In general, the requirements would be set by international safety standards; such as, IEC 61800-5-2 [1], and would be controlled by series relay contacts and inserted into the electric motor drive system [1-3].

The serial relay contact control would be in accordance with the ISO-13849 instructions. One of the basic safety principles is "Sequential switching for redundant serial contact circuits" to avoid normal connection failure [2,4]. Consequently, both on and off switching would not occur at the same time. Thus, only one of the switches could not operate allowing the current to flow from the supply to the motor, which a function would be 1oo2 (one-out-of-two).

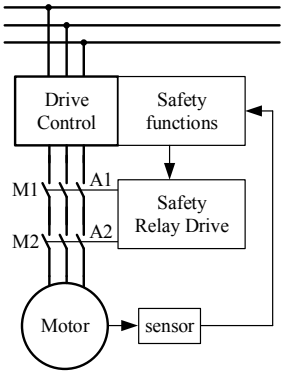


Fig. 1. Safety function of the electrical machine drive system in an emergency stop.

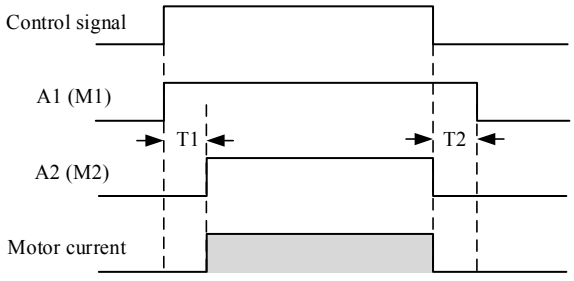


Fig. 2. Welding contact protection with series switching contacts.

In Figure 2, it could be seen that the AC power supply was not directly connected to the load. This would be connected through relay $A_1(M_1)$ that would be connected in a series with relay $A_2(M_2)$. When the control signal was active, relay A_1 would be running at the same time but relay

$A_2(M_2)$ would have a T_1 delay, and when the control signal ended, relay $A_2(M_2)$ would immediately stop working but reel $A_1(M_1)$ would delay T_2 first and then stop. Thus, the results would show that the two relays could not operate at the same time. If a relay contact failed in one relay, the other could continue to operate without a contact.

Relay drive circuits in a safe operation order

For the series switching contacts from Figure 2, the detailed condition and order of the signals of the series switching contacts could be written as Equations 1 and 2 [6].

(1) $$A_1 = s \cdot s\Delta T_2$$

(2) $$A_2 = s \cdot s\Delta T_1$$

From Equations 1 and 2, the principle of the sequential switching to design the circuit delay model and 4-pin capacitor can be shown in Figure 3.

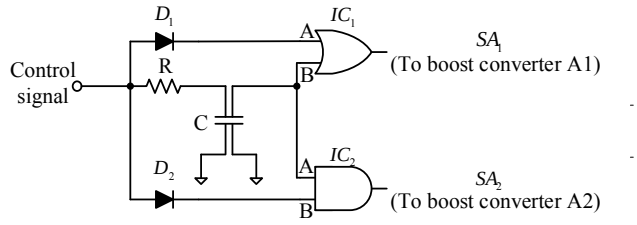


Fig. 3. Fail-safe sequential switching circuit with logic ICs.

In this case, the delay could only be used one delay time to reduce the number of devices in the circuit. A_1 would use a capacitor discharge interval (T_2), and A_2 would utilize a capacitor discharge interval (T_1). The capacitor would use a 4-pin capacitor, or a 2-pin capacitor with a cut-off printed circuit board [10] to solve the capacitor open failure problem. The signal from the digital five volts ICs could not directly drive the 24 Volts relay. A flyback boost converter circuit or boost circuit with transformer would be used to drive a relay in the event that its gain would be more than four. The circuits comprising a combination of flyback converter circuits and boost converter circuits would be proposed to increase the boost ratio [11-13].

Therefore, the circuit would need to be safe when it failed, so the 4-pin capacitors would be used where safety in the event of an open failure occurred. The high boost ratio DC–DC converter circuit derived from cascading a flyback converter and a boost converter with a fail-safe capacitor is shown in Figure 4.

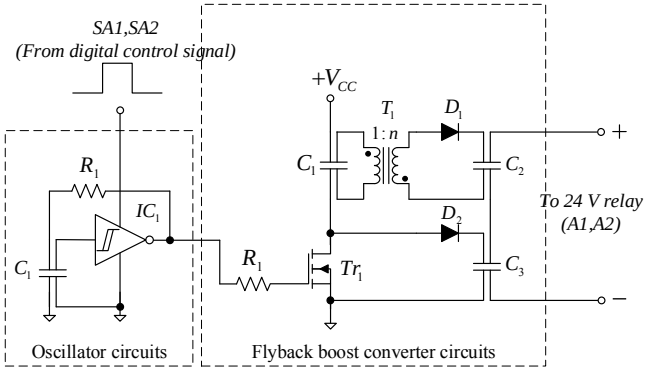


Fig. 4. Flyback converter and a boost converter with a fail-safe capacitor.

The output voltage would be the sum of a flyback converter with an output voltage gain, which would be the ratio of the transformer with a duty cycle (Equation 3) and a boost converter with the output voltage gain would be the duty cycle ratio (Equation 4). The total output voltage is shown in Equation 5.

(3) $$V_o = \frac{nD}{1-D} V_{in}$$

(4) $$V_o = \frac{1}{1-D} V_{in}$$

(5) $$V_o = \frac{1+nD}{1-D} V_{in}$$

Result and Discussion

The results of a relay drive circuit for a safe operation order with digital logic ICs sequential switching are shown in Figures 5 - 7.

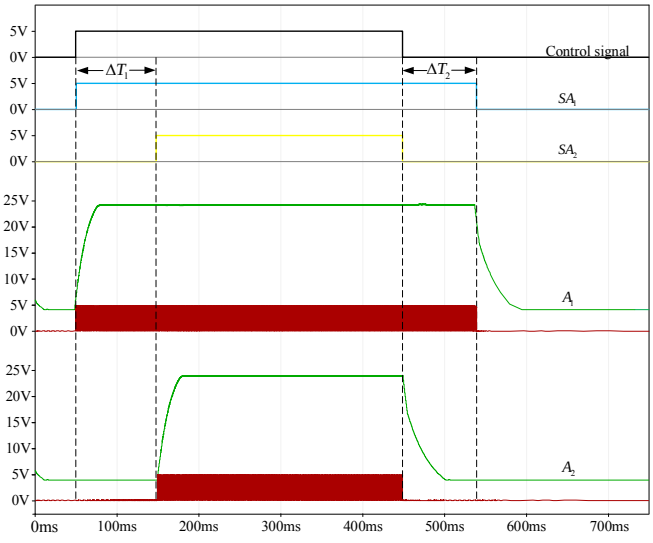


Fig. 5. Simulation results of relay drive circuits for a safe operation order with a digital logic ICs sequential switching function.

Figure 5 shows the simulation results and Figure 7 displays the experimental results of the relay drive circuits for a safe operation order with digital logic ICs sequential switching that could operate as designed. The signal sequence had an on and off delay between relays A_1 and A_2 of approximately 100 ms, which were sufficient to protect the relay welding [2]. The flyback and boost converter circuits increased the voltage from five volts to 24 volts that was conducted by a pulsed signal obtained from a capacitor open-circuit self-oscillation in a CMOS Schmitt trigger invertor oscillator circuit [10].

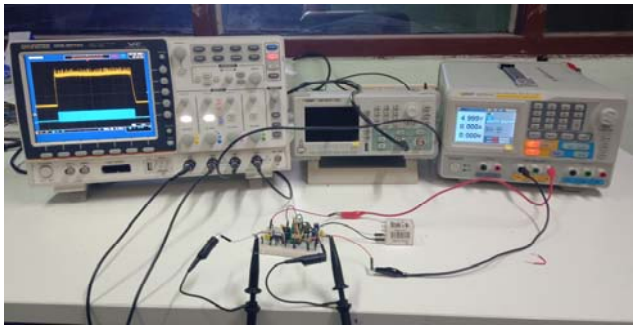
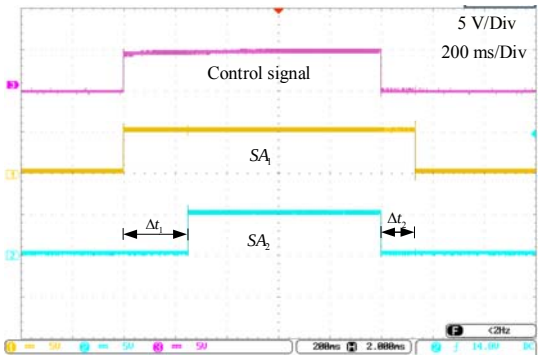
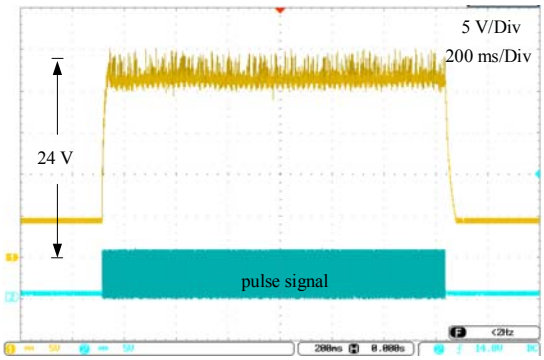


Fig. 6. Experimental circuits



a) The signal voltage of sequential switching circuit with logic ICs



b) The signal voltage of flyback converter and a boost converter

Fig. 7. Experimental results of relay drive circuits for a safe operation order with a digital logic ICs sequential switching function

Table 1 FMEA of the single failure of a sequential switching circuit with a logic ICs circuit

Device		Failure Mode	Effect of the Failure	Remark
R_1		R*0.5	Change of the circuit's characteristic.	Δ
		R*2	Change of the circuit's characteristic.	Δ
		Short circuit	SA_1 signal same as the input; SA_2 signal same as the input.	▲
		Open circuit	SA_1 signal same as the input; SA_2 no signal.	Δ
C_1		C*0.5	Change of the circuit's characteristic.	Δ
		C*2	Change of the circuit's characteristic.	Δ
		Short circuit	SA_1 signal same as the input; SA_2 no signal.	Δ
		Open circuit	SA_1 signal same as the input; SA_2 no signal.	Δ
IC_1	Pin A	Struck at 1	SA_1 5 V, and SA_2 normal signal.	Δ
		Struck at 0	SA_1 signal same as the SA_2; SA_2 normal signal.	▲
	Pin B	Struck at 1	SA_1 5 V, and SA_2 signal same as the input.	Δ
		Struck at 0	SA_1 signal same as the input; SA_2 no signal.	Δ
IC_2	Pin A	Struck at 1	SA_1 5 V, and SA_2 signal same as the input.	Δ
		Struck at 0	SA_1 signal same as the input; SA_2 no signal.	Δ
	Pin B	Struck at 1	SA_1 normal signal; SA_2 off delay time.	Δ
		Struck at 0	SA_1 signal same as the input; SA_2 no signal.	Δ
D_1		Short circuit	SA_1 normal signal; SA_2 normal signal	Δ
		Open circuit	A_1 on delay time, SA_2 normal signal.	Δ
D_2		Short circuit	SA_1 normal signal; SA_2 normal signal	Δ
		Open circuit	SA_1 normal signal; SA_2 no signal.	Δ

Remark : Δ: No significant consequences. ▲: Abnormal condition

Table 2 FMEA of the single failure of flyback and boost converters with a fail-safe capacitor

Device	Failure Mode	Effect of the Failure	Remark
R_1	R*0.5	Change of the circuit's characteristic.	Δ
	R*2	Change of the circuit's characteristic.	Δ
	Short circuit	Normal output.	Δ
	Open circuit	Output 3.8 V DC.	Δ
C_1	C*0.5	Change of the circuit's characteristic.	Δ
	C*2	Change of the circuit's characteristic.	Δ
	Short circuit	Output 3.5 V DC.	Δ
	Open circuit	Normal output.	Δ
C_2	C*0.5	Change of the circuit's characteristic.	Δ
	C*2	Change of the circuit's characteristic.	Δ
	Short circuit	Output 4.3 V DC.	Δ
	Open circuit	Output 0 V DC.	Δ
C_3	C*0.5	Change of the circuit's characteristic.	Δ
	C*2	Change of the circuit's characteristic.	Δ
	Short circuit	Output reduces to 0 V DC.	Δ
	Open circuit	Output 0 V DC.	Δ
D_1	Short circuit	Output 4.5 V DC with 1 V ripple.	Δ

	Open circuit	Output reduces to 0 V DC.	Δ
D_2	Short circuit	Output 4.5 V DC with 1 V ripple.	Δ
	Open circuit	Output reduces to 0 V DC.	Δ
T_1	Short circuit pri	Output 3.6 V DC.	Δ
	Short circuit sec	Output 3.6 V DC.	Δ
	Open circuit pri	Output 0 V DC.	Δ
	Open circuit sec	Output reduces to 0 V DC.	Δ
T_r	Short circuit D-S	Output 4.5 V DC with 1 V ripple.	Δ
	Open circuit G	Output 3.8 V DC.	Δ
	Open circuit D	Output 3.8 V DC.	Δ
	Open circuit S	Output 3.8 V DC.	Δ

Remark : Δ: No significant consequences. ▲: Abnormal condition.

The circuit consisted of individual components that were characterized by the failure from the nature of the components and the structure of the system. Modeling, calculations and validation were also required, and the model was based on the review of the systems and assumptions about the system behavior. The performance analysis of the IEC 61800-5-2 variable speed electric drive systems with the FMEA and the experiments are shown in Tables 1 and 2.

Table 1 shows the FMEA of the single failure of a sequential switching circuit with a logic ICs circuit, which the most common failures were harmless and without any consequences. However, there could be the failure of 1) the short circuit on resistor R_1 that would cause no delay signal, output SA_1 and SA_2 signal would be similar to the input signal, and relays A_1 and A_2 would operate at the same time. 2) The logic would strike at “0” of pin A of the OR logic gate, the SA_2 signal would operate normally, but the SA_1 signal would function simultaneously with SA_2, which in both cases, the relay would be on and off simultaneously, potentially causing a dangerous failure. Nevertheless, such failures could be solved by adding a set of separate open and closed delay circuits. This would enable both the open and closing delays to not fail simultaneously in the event of a single failure. For Table 2, the FMEA of the single failure of the flyback and boost converters with a fail-safe capacitor test in a circuit did not produce any dangerous failures. This was because the flyback and boost converter circuits needed to work together in combination with the two circuits to achieve a voltage gain greater than four times, as a potential single failure could not produce a high voltage gain boost. As a consequence, the circuit would be safe in the event of any failure.

Conclusion

This paper proposed a simulation and experiment of a relay drive circuit for a safe operation order with a digital logic sequence switching according to ISO 13849-2 for the safe design. The boost circuits increased the voltage from five volts to 24 volts, that the high voltage gain boost DC-DC converter circuit was derived from cascading a flyback converter and a boost converter with fail-safe capacitors. Safety development analysis was determined by the FMEA of IEC 61800-5-2 for adjustable speed electrical power drive systems. The results showed that the proposed system worked as a conditional motor drive failure, in which the designed circuit was fail-safe and without any dangerous failures.

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