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A new Modeling of IGBT and Freewheeling Diode based on Electrical Behavioral with Independently of Time Condition

Abstract. *Several IGBT model proposed and constructed over the past years have exposed different essential qualities. However, in this paper, a new model of IGBT and Freewheeling diode based on electrical behavior is presented. The proposed parameters extraction process adopts the least squares regression and bilinear interpolation and, a two-level capacitance technique. and the model's structure solely consists of fundamental components. In addition, the proposed model validates its simplicity for parameters extraction process, and its user-friendly application for a circuit topology of fundamental components. Some key factors of our proposed model are; independent time constraint, implementation flexibility, easily application by different topologies. These enumerated factors reinforce the reliability and suitability of our proposed model for a circuit simulation and optimization. The verification of our proposed model was steered with the use of an experimental circuit that consists of commercial components. Lastly, our simulation results showed a pattern of consistency with the experimental results.*

Streszczenie. *W artykule opisano nowy model IGBT wykorzystujący diodę ruchu swobodnego (freewheeling diode).Model opiera się na niezależnym, ograniczeniu czasu, elastyczności zastosowania I łatwym zastosowaniu w różnych topologiach. Przeprowadzono symulację i optymalizację modelu. Wyniki zweryfikowano eksperymentalnie.* .***Nowy model IGBT bazujący na diodzie typu Freewheeling z niezależnym ograniczeniem czasu***

Keywords: IGBT; Freewheeling diode; Behavioral modeling; Least squares regression; Bilinear interpolation.
Słowa kluczowe: IGBT, Freewheele diode – dioda ruchu swobodnego,.

Introduction

The development of IGBT over the last 20 years has led to different and continuous interests in its application capabilities. It is used in many areas of circuit application such as; flyback inverter, half-bridge inverter and full-bridge inverter [29-31], and also in general applications such as: cooktop appliance, induction forging, induction hardening and electric vehicle [32-35]. The widely use of IGBT device for various high power applications could be associated with its high power density properties. Many researchers have developed different mathematical models for the evaluation of its electric behavior in application circuits for the mitigation of unwarranted occurrences that may arise during hardware implementation.

An analytical IGBT model derived from the physical property of an IGBT device that initializes from an am-bipolar diffusion equation and a fundamental equation of a semiconductor device were proposed [1-11]. Authors of literatures [12-15] presented models derived from the fundamental equations of MOSFET and BJT combination. The electrical and thermal effects that comprise of silicon chip surface temperature package, header temperature package, case temperature, and ambient temperature were demonstrated by the models in [16, 17].

Researchers in [18], designed and proved the implementation of Saber Circuit Simulator with static and dynamic condition, and their results were similar to the expected experimental results. An equivalent circuit suitable for SPICE simulation was proposed [19-21]. As stated above, an analytical IGBT model has been widely implemented in numerous applications, however, parameters extraction process for an analytical model from physical phenomenon requires a professional technique, in order to complete the model construction. There are many parameters that are difficult to specify, and are unstated in the manufacturer's specifications sheet, which makes the implementation of the analytical model difficult. Nonetheless, the behavioral model is less complex than the analytical model.

Different mathematical modeling techniques using an electrical behavior were proposed in [22, 23]. Authors of these literatures proposed a behavioral model which initializes from the fundamental equations of MOSFET and BJT, but its implementation still remains problematic. A simplified behavioral model based on data measurement, corresponding circuit, mathematical model, construction method was proposed in [24]. Though, the disadvantage of this model might not be overseen by ambiguous and complex shape of its gate signal, because its conductance function is separated into a state of time, and it is also independent on voltage drop between the gate and the emitter. A model that governs this ambiguous and complex shape of gate was proposed [25]. This technique was structured on neuron-fuzzy functions, which could be considered as a complex method in the construction process, when compare with the method proposed in [26]. The author's approach embraces the Hammersten Model, which consists of nonlinear static block and a linear dynamic block, this model is governed by IGBT phenomena. Nevertheless, our proposed model that embraces a simplified circuit simulation and optimization technique is technically different from the model proposed in [26]. The proposed model is presented as schematic' diagram, and consists of inactive components.

Finally, we present a technique for modeling an IGBT and Freewheeling diode, the model was constructed with the use of manufacturer's specifications sheet, and experimental setup. This technique is based on the least squared regression method with electrical characteristics, in terms of collector-emitter current against collector-emitter voltage at each point of gate-emitter voltage. A bilinear interpolation method for conductance function modeling, was also adopted.

IGBT and Freewheeling diode conductance modeling

An equivalent circuit of our proposed IGBT and Freewheeling diode model is presented in this section. It is made up of fundamental components as displayed in Fig. 1. The conductance modeling process is divided into two parts. The first part is the G_{CE} IGBT conductance modeling process, which is also sub-divided into two parts; the modeling of electrical characteristics in terms of the collector-emitter voltage against collector-emitter current at each point of gate-emitter voltage, and the use of bilinear interpolation method that depends on both the collector-

emitter voltage and gate-emitter voltage for the governing of conductance function.

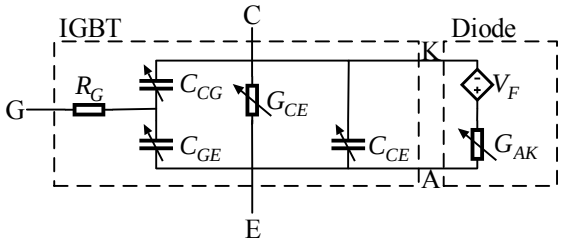

Fig. 1. Schematic diagram of IGBT and a Freewheeling diode model.

The first part of IGBT conductance modeling involves the formulation of the proposed least squares regression with polynomials. Eq. (1) represents the fundamentals of least squares regression by polynomials as a general form of collector-emitter current a variation against collector-emitter voltage [28].

(1) $I_{CE}\left(V_{CE},V_{GE}\right)=a_0+a_1V_{CE}+a_2V_{CE}^2+\ldots+a_mV_{CE}^m$.

The collector-emitter current (I_{CE}), collector-emitter voltage (V_{CE}), gate-emitter voltage (V_{GE}), and the coefficients $a_0,a_1,a_2,\ldots,a_m$ transform Eq. (1) into data curve. m is less than the total number of data minus one $\left(m<n-1\right)$, which means that one set of data includes n data point in the form of $\left(V_{CE}^i,I_{CE}^i\right)$, while $i=1,2,3,\ldots,n$. To model a collector-emitter current against collector-emitter voltage at each gate-emitter voltage curve, we used data from manufacturer's specifications sheet of IGBT-2MBI100VA-120-50 [38]. Solving Eq. (1) leads to the mathematical Eq. (2), and from the curve in manufacturer's specifications sheet, the gate-emitter voltage at 8V:

(2)
$$I_{CE}\left(V_{CE},8\right)=\begin{cases}0, & V_{CE}<0.703855\\ -0.037838+21.6397\mathrm{V_{CE}}-369.496\left(\mathrm{V_{CE}}\right)^2+2235.37\left(\mathrm{V_{CE}}\right)^3-6428.56\left(\mathrm{V_{CE}}\right)^4 & \\ +9750.11\left(\mathrm{V_{CE}}\right)^5-7975.32\left(\mathrm{V_{CE}}\right)^6+3333.3\left(\mathrm{V_{CE}}\right)^7-559.518\left(\mathrm{V_{CE}}\right)^8, & 0.703855\le V_{CE}<1.32232\\ 12.136, & V_{CE}\ge 1.32232\end{cases}$$

at 10V:

(3)
$$I_{CE}\left(V_{CE},10\right)=\begin{cases}0, & V_{CE}<0.682059\\ -0.8137+29.8023\mathrm{V_{CE}}-146.241\left(\mathrm{V_{CE}}\right)^2+222.085\left(\mathrm{V_{CE}}\right)^3-119.032\left(\mathrm{V_{CE}}\right)^4 & \\ +27.4129\left(\mathrm{V_{CE}}\right)^5-2.32489\left(\mathrm{V_{CE}}\right)^6, & 0.682059\le V_{CE}<3.43329\\ 95.873, & V_{CE}\ge 3.43329\end{cases},$$

at 12V:

(4)
$$I_{CE}\left(V_{CE},12\right)=\begin{cases}0, & V_{CE}<0.684558\\ 6.46642-59.1606\mathrm{V_{CE}}+82.3672\left(\mathrm{V_{CE}}\right)^2-14.2348\left(\mathrm{V_{CE}}\right)^3, & 0.684558\le V_{CE}<3.22808\\ 107.78+27.0083\mathrm{V_{CE}}, & V_{CE}\ge 3.22808\end{cases}$$

at 15V:

(5)
$$I_{CE}\left(V_{CE},15\right)=\begin{cases}0, & V_{CE}<0.605108\\ 1.59022-30.6318\mathrm{V_{CE}}+46.2789\left(\mathrm{V_{CE}}\right)^2, & V_{CE}\ge 0.605108\end{cases}$$

at 20V:

(6)
$$I_{CE}\left(V_{CE},20\right)=\begin{cases}0, & V_{CE}<0.633139\\ 4.12014-44.2401\mathrm{V_{CE}}+59.5962\left(\mathrm{V_{CE}}\right)^2, & V_{CE}\ge 0.633139\end{cases}$$

. and at 7V, the gate-emitter threshold voltage is given as $I_{CE}\left(V_{CE},7\right)=0$.

The governing conductance function that depends on both the collector-emitter voltage, and gate-emitter voltage. The characteristics curve from the manufacturer's specifications sheet could be considered as rectangular grids, with the proposed bilinear interpolation method. The graphical representation of bilinear interpolation for a two-dimensional interpolation is shown in Fig. 2.

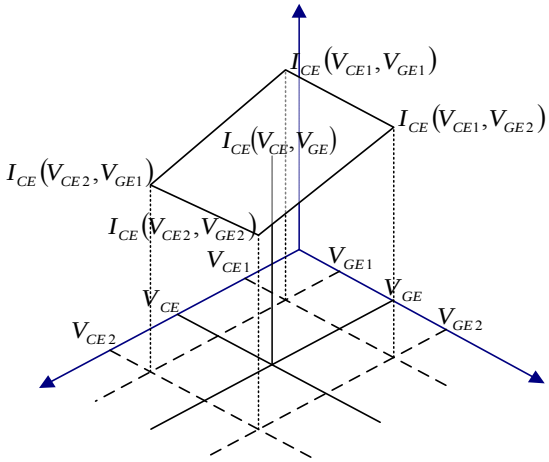

Fig. 2. Graphical depiction of two-dimensional bilinear interpolation.

The general form of bilinear interpolation that relates the collector-emitter current, collector-emitter voltage with the gate-emitter voltage is given as the surface equation in Eq. (7) [36].

(7) $I_{CE}\left(V_{CE},V_{GE}\right)=b_1+b_2V_{CE}+b_3V_{GE}+b_4V_{CE}V_{GE}$.

and from Eq. (7) the values of coefficient b_1,b_2,b_3 and b_4 are into four parts as follows.

b_1:

(8)
$$b_1=\frac{V_{CE2}V_{GE2}I_{CE}\left(V_{CE1},V_{GE1}\right)-V_{CE2}V_{GE1}I_{CE}\left(V_{CE1},V_{GE2}\right)-V_{CE1}V_{GE2}I_{CE}\left(V_{CE2},V_{GE1}\right)+V_{CE1}V_{GE1}I_{CE}\left(V_{CE2},V_{GE2}\right)}{\left(V_{CE2}-V_{CE1}\right)\left(V_{GE2}-V_{GE1}\right)}$$

b_2:

(9)
$$b_2=\frac{-V_{GE2}I_{CE}\left(V_{CE1},V_{GE1}\right)+V_{GE1}I_{CE}\left(V_{CE1},V_{GE2}\right)+V_{GE2}I_{CE}\left(V_{CE2},V_{GE1}\right)-V_{GE1}I_{CE}\left(V_{CE2},V_{GE2}\right)}{\left(V_{CE2}-V_{CE1}\right)\left(V_{GE2}-V_{GE1}\right)}$$

b_3:

(10)
$$b_3=\frac{-V_{CE2}I_{CE}\left(V_{CE1},V_{GE1}\right)+V_{CE2}I_{CE}\left(V_{CE1},V_{GE2}\right)+V_{CE1}I_{CE}\left(V_{CE2},V_{GE1}\right)-V_{CE1}I_{CE}\left(V_{CE2},V_{GE2}\right)}{\left(V_{CE2}-V_{CE1}\right)\left(V_{GE2}-V_{GE1}\right)}$$

and b_4 **as:**

(11)
$$b_4=\frac{I_{CE}\left(V_{CE1},V_{GE1}\right)-I_{CE}\left(V_{CE1},V_{GE2}\right)-I_{CE}\left(V_{CE2},V_{GE1}\right)+I_{CE}\left(V_{CE2},V_{GE2}\right)}{\left(V_{CE2}-V_{CE1}\right)\left(V_{GE2}-V_{GE1}\right)}$$

.

V_{CE1} and V_{CE2} are given as:

(12) $V_{CE1}=V_{CE}-\Delta V_{CE}$,

(13) $V_{CE2}=V_{CE}+\Delta V_{CE}$.

and an acceptable value of $\Delta V_{CE}=0.1$. Finally, V_{GE1} and V_{GE2} are given as:

(14)
$$V_{GE1}=\begin{cases}0, & 0\le V_{GE}<8\\ 8, & 8\le V_{GE}<10\\ 10, & 10\le V_{GE}<12\\ 12, & 12\le V_{GE}<15\\ 15, & 15\le V_{GE}<20\\ 15, & V_{GE}\ge 20\end{cases},$$

(15)
$$V_{GE2}=\begin{cases}8, & 0\le V_{GE}<8\\ 10, & 8\le V_{GE}<10\\ 12, & 10\le V_{GE}<12\\ 15, & 12\le V_{GE}<15\\ 20, & 15\le V_{GE}<20\\ 20, & V_{GE}\ge 20\end{cases}.$$

The derivation of a complete conductance function (G_{CE}) is given as:
(16)
$$G_{CE}\left(V_{CE},V_{GE}\right)=\begin{cases}0, & V_{GE}\le V_T\\ \dfrac{I_{CE}\left(V_{CE},V_{GE}\right)-I_{CE}\left(V_{CE}-\Delta V_{CE},V_{GE}\right)}{\Delta V_{CE}}, & V_{GE}>V_T\end{cases}$$

.
while $V_T=7V$.

The second part involves the modeling the conductance function of a Freewheeling diode, which is based on the electrical behavior of the diode adopted from the Manufacturer's specifications sheet. The anode-cathode current and the anode-cathode voltage with least square regression method. the cathode current function is stated in Eq. (1) as:
(17)
$$I_{AK}\left(V_{AK}\right)=\begin{cases}0, & V_{AK}<0.685511\\ 2.91465-19.4867V_{AK}+7.35414\left(V_{AK}\right)^2+21.6919\left(V_{AK}\right)^3, & V_{AK}\ge 0.685511\end{cases}$$

, from Eq. (17) the diode conductance is derived as:
(18)
$$G_{AK}\left(V_{AK}\right)=\begin{cases}0, & V_{AK}<V_F\\ \dfrac{I_{AK}\left(V_{AK}\right)-I_{AK}\left(V_{AK}-\Delta V_{AK}\right)}{\Delta V_{AK}}, & V_{AK}\ge V_F\end{cases}$$

, while the forward on voltage of diode is given as:
(19)
$$V_F=\begin{cases}0, & V_{AK}<0\\ 0.7, & V_{AK}\ge 0\end{cases}.$$

Internal capacitance estimation

In this section, a two-level capacitance estimation process is presented. It is divided into 2 parts; capacitance estimation (1), and capacitance estimation (2), both parts are used in the experimental set up as shown in Fig 3. The diode section was excluded because the experiment was solely conducted on the positive side of IGBT device. Other necessary assigned parameters before estimation are; V_{dc} , V_{in} , R_1 , and R_2 , it must be noted that appropriate parameters are required for a precise and definite estimation process. The parameters chosen for a clear and concise signal measurement are; $V_{dc}=48\text{V}$, $R_1=53.4\Omega$, $R_2=30\Omega$, and V_{in} was assigned with a one-period rounded shape rectangular pulse that has a rise and fall time of 46 ns, width of 41.7 us, and amplitude of 12V. $R_G=7.5\Omega$ value was adopted from the Manufacturer's specifications sheet. The results from the measurement points of V_{CE} and V_{GE} could be separated into signal wave forms of 9 states, t_1 to t_9 , as shown in Fig 4. While the dash line of V_{CE} , and the solid line of V_{GE} represent the signal wave forms.

First, is the capacitance estimation process level 1, which consists of C_{CE} , C_{CG} and C_{GE} . These capacitances function when internal collector-gate voltage level greater than zero ($V_{CG}>0$). The variables at level 1 are given as: C_{CE1} , C_{CG1} and C_{GE1} respectively. The derivation process for solving these variables are presented as follows [27, 37]:

(20)
$$V_T^+=12e^{-\frac{t_1}{C_{CGGE1}R_2}}\left(-1+e^{\frac{t_1}{C_{CGGE1}R_2}}\right),$$

C_{CGGE1}:

(21)
$$C_{CGGE1}=C_{CG1}+C_{GE1},$$

and

(22)
$$C_{GE1}=r_1C_{CG1}.$$

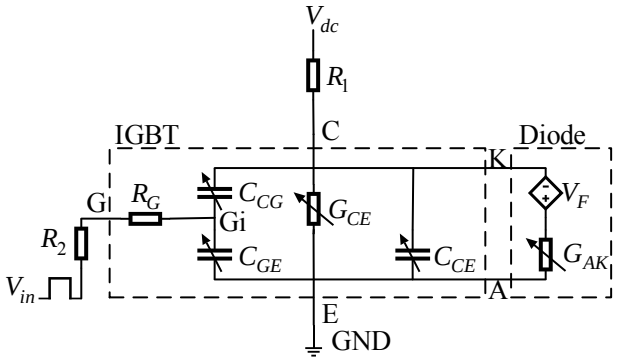

Fig. 3. Schematic diagram for internal capacitance estimation.

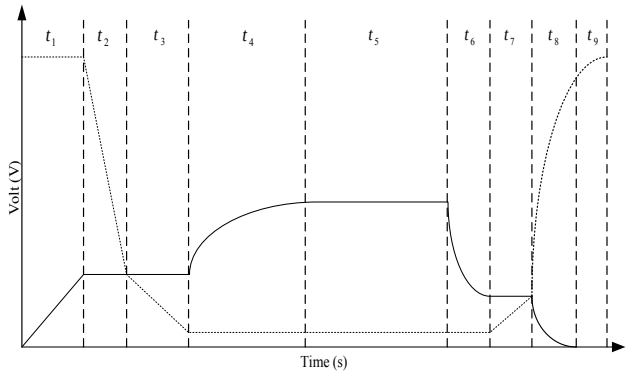

Fig. 4. Transition state of IGBT.

The final derivation of level 1 capacitance completed by solving Eq. (23)
(23)
$$V_T^+=\frac{48e^{-\left(\frac{G_{CE}\left(V_S,V_T^+\right)t_2}{C_{CGCE1}}\right)-\left(\frac{t_2}{C_{CGCE1}R_1}\right)}\left(G_{CE}\left(V_S,V_T^+\right)R_1+e^{\frac{\left(1+G_{CE}\left(V_S,V_T^+\right)R_1\right)t_2}{C_{CGCE1}R_1}}\right)}{1+G_{CE}\left(V_S,V_T^+\right)R_1}$$

,
while C_{CGCE1} is given as:

(24)
$$C_{CGCE1}=C_{CG1}+C_{CE1}.$$

from Eq. (20) and Eq. (23), t_1 and t_2 are time durations as depicted in Fig. 4, which obtainable from the measurement data. V_T^+ is voltage value that is slightly greater than the gate-emitter threshold voltage. V_S is collector-emitter saturation voltage which can be obtained from manufacturer's specifications sheet. In order to achieve desirable values for C_{CG1} and C_{GE1} from Eq. (22), coefficient ratio r_1 could be adopted from the (Tunable

parameter). By using the assigned values of (0.216×10^{-6} and 0.275×10^{-6}) from the experimental data, for t_1 and t_2, and solving Eq. (20) and Eq. (23) with Newton method [28], values of $C_{CGGE1}=6.564\times10^{-9}$ and $C_{CGCE1}=29.412\times10^{-9}$ were obtained. $r_1=11$, and solving Eq. (21) and Eq. (24) the solution values of $C_{CG1}=0.547\times10^{-9}\text{F}$, $C_{GE1}=6.017\times10^{-9}\text{F}$, and $C_{CE1}=28.865\times10^{-9}\text{F}$ were obtained.

Second, is the capacitance estimation process level 2. These capacitances function, when internal collector-gate voltage level less than or equal to zero ($V_{CG}\le0$). The variables at level 2 are given as: C_{CE2}, C_{CG2} and C_{GE2}. The derivation process for solving these variables are presented as follows:

(25) $$V_{inA}=12e^{-\frac{5t_4}{C_{CGGE2}R_2}}\left(-0.415+e^{\frac{5t_4}{C_{CGGE2}R_2}}\right),$$

C_{CGGE1}:

(26) $$C_{CGGE2}=C_{CG2}+C_{GE2},$$

and

(27) $$C_{GE2}=r_2C_{CG2}.$$

The final derivation of level 2 capacitance completed by solving Eq. (28)

(28)

$$V_S=\frac{48e^{-\left(\frac{G_{CE}\left(V_S,V_T^+\right)t_3}{2C_{CGCE2}}\right)-\left(\frac{t_3}{2C_{CGGE2}R_1}\right)}\left(-0.854+0.146G_{CE}\left(V_S,V_T^+\right)R_1+e^{\frac{\left(1+G_{CE}\left(V_S,V_T^+\right)R_1\right)t_4}{2C_{CGGE2}R_1}}\right)}{1+G_{CE}\left(V_S,V_T^+\right)R_1},$$

while C_{CGCE2} is given as:

(29) $$C_{CGCE2}=C_{CG2}+C_{CE2}.$$

from Eq. (25) and Eq. (28) V_{inA} an amplitude of V_{in}. By using the assigned values of (1.992×10^{-6} and 7.853×10^{-6}) the experimental data, for t_3 and t_4, solving Eq. (25) and Eq. (28), the values of $C_{CGGE2}=43.021\times10^{-9}$ and $C_{CGCE2}=146.158\times10^{-9}$ were obtained. $r_2=0.111$, and solving Eq. (26) and Eq. (29) the solution values of $C_{CG2}=38.723\times10^{-9}\text{F}$, $C_{GE2}=4.298\times10^{-9}\text{F}$, and $C_{CE2}=107.435\times10^{-9}\text{F}$ were obtained.

To complete the internal capacitance estimation process the final representation of C_{CG}, C_{GE} and C_{CE} can be written as

(30) $$C_{CG}=\begin{cases}C_{CG2}, & V_{CGi}\le0\\ C_{CG1}, & V_{CGi}>0\end{cases},$$

(31) $$C_{GE}=\begin{cases}C_{GE2}, & V_{CGi}\le0\\ C_{GE1}, & V_{CGi}>0\end{cases},$$

(32) $$C_{CE}=\begin{cases}C_{CE2}, & V_{CGi}\le0\\ C_{CE1}, & V_{CGi}>0\end{cases}.$$

Simulation Results and Discussion

The simulation and experimental outcomes of our proposed model's verification process are theoretically explained in this section. It involves two procedural measures; the simulation of the resistive load, and the inductive load respectively.

The schematic diagram in Fig. 3 is a representation of a simulated resistive load, and the technical procedures observed are as follows; assigning of components' values such as; $R_1=53.4\Omega$, $R_2=50\Omega$, however, V_{in} was assigned by one-period rounded shape rectangular pulse that has a rise and fall time of 46 ns, width of 41.7 us, and an amplitude of 12 V. The next step is solving a time domain differential equation, using coded Python Language platform, and a Numpy as reference library [39-41]. The simulation results from this process are displayed in Fig. 5. However, these results are chronologically grouped into three parts: input voltage, gate-emitter voltage, and the collector-emitter voltage. While the last component voltage supply V_{dc} is assigned the value of 48 V.

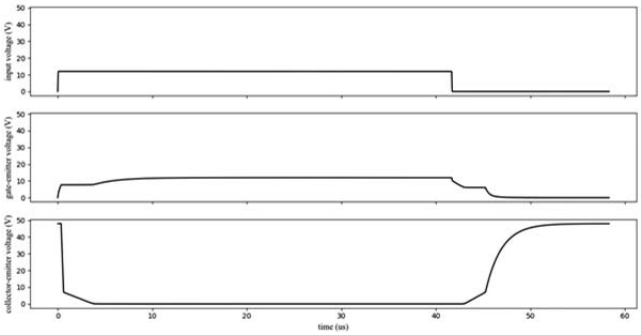

Fig. 5. Resistive load simulation result.

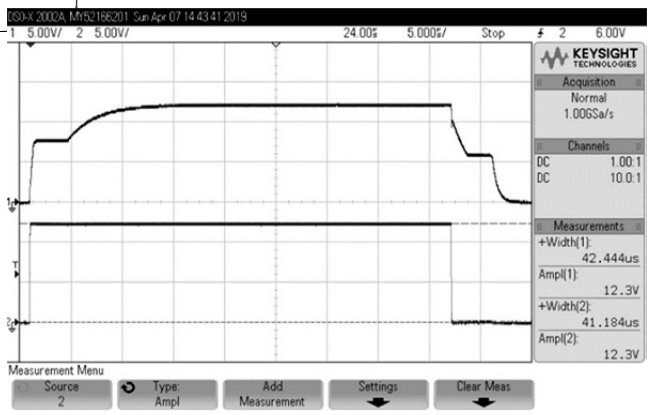

Fig. 6. Resistive load experimental result, input voltage against gate-emitter voltage.

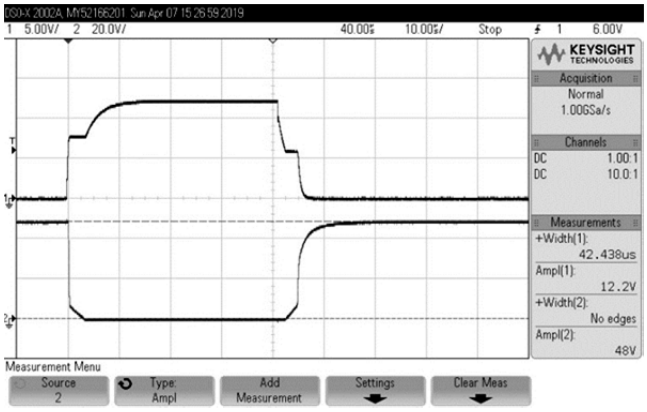

Fig. 7. Resistive load experimental result, gate-emitter voltage against collector-emitter voltage.

The experimental process of the resistive load simulation was carried out with a circuit of same parameters, and results are shown in Fig. 6 and Fig. 7 respectively. Fig. 6 shows the input voltage graph below and the gate-emitter voltage graph above, while Fig. 7 illustrates the gate-emitter signal and the collector-emitter signal below. The measurement of data for Fig. 6 was carried out using an oscilloscope adjusted to Time/Div of 5 us, Volts/Div of 5V, Probe of 1:1 for channel 1, and 10:1 for channel 2. While for Fig. 7, the oscilloscope was readjusted to the values of 10 us for Time/Div, 5V and 20V for Volt/Div, and probe ratio of both channels remained unchanged. Lastly, signals from channel 1 and channel 2 are displayed as the upper and lower graphs in Fig. 7.

From the simulation results, the transition states are separated into 9 states is shown in Fig. 4 the internal capacitance estimation section, which is also illustrated in Fig. 5 for the middle and bottom gate-emitter voltage and collector-emitter voltage. The time duration in each state is presented in Table 1, Column 2, while Column 3 is for the time duration of each state of the experimental results.

The transition states for both simulation and experimental results are the same, the time duration in each state of the simulation is also constant, and closely related to that of the experimental results. This feature reflects the strength and effectiveness of our model for the simulation of any resistive circuit connected with a resistive load.

Table 1. Comparison between the simulation and experimental results

Transition state	Simulation result (us)	Experimental result (us)
t_1	0.350	0.330
t_2	0.262	0.296
t_3	3.138	3.106
t_4	10.25	10.10
$t_4+t_5+t_6$	38.01	39.06
t_6	1.50	1.44
t_7	2.10	2.23
t_8	2.20	1.93
t_8+t_9	7.20	7.47

In the second part of an inductive load simulation, the schematic diagram of Fig. 8 was adopted with parameter s' values of; $L_1=100\times10^{-6}\text{H}$, $C_1=0.8179\times10^{-6}\text{F}$, and $R_1=7.5\Omega$. These components' values remained constant in the resistive load simulation process.

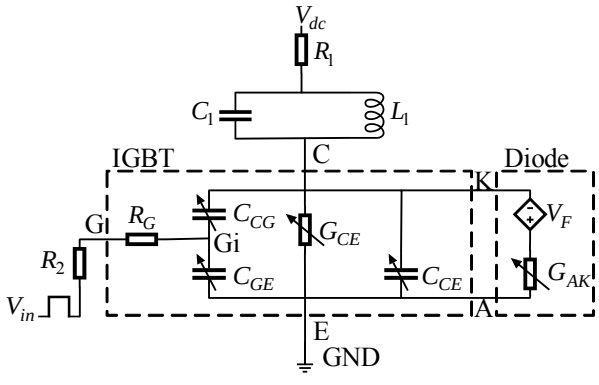

Fig. 8. Schematic diagram for an inductive load simulation.

Both IGBT and Freewheeling diode were considered in the verification process of the model's capability for an inductive load simulation. The simulation and experimental results are depicted in Fig. 9 and Fig. 10 respectively. The simulation curve resulted from the conducted experiment, and it reveals that IGBT and Freewheeling diode are always in complete synchronization for an inductive load simulation.

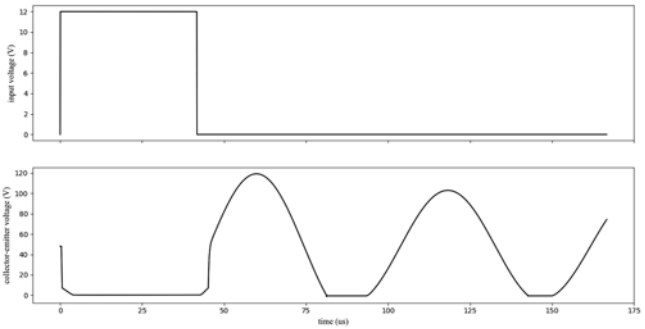

Fig. 9. Inductive load simulation result.

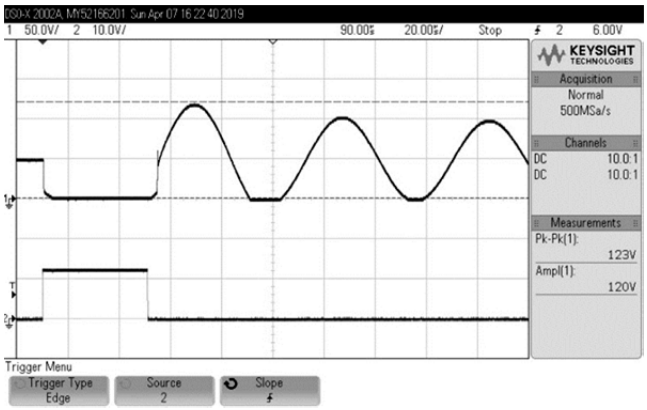

Fig. 10. Inductive load experimental result.

Simulation results from the resistive and inductive load have shown that our proposed IGBT and Freewheeling diode model is suitable for both resistive and inductive load simulation circuits. However, the practical benefits of this model are sub-divided into three parts. First, the transition state results from t_1 to t_9 of this model are closely related in term of physical behavior to that of the experimental results, in accordance with t_2, t_3, t_7 and t_8+t_9 on the high power side are duly considered. Second, the model is without time-constraint, which portrays its implementation flexibility for different circuits' topologies. Lastly, fundamental components such as; G, L, and C, are incorporated in our model for simplicity use in circuit topology.

Conclusions

Though there have been different proposed models of IGBT, however, our proposed model, which is based on electrical behavior of IGBT and Freewheeling diode opens up an interesting area of research that could be further explored in the future. The experimental results of the proposed model proved without doubt, its simulative capability for resistive and inductive loads. Furthermore, it showed the simplicity of the model's parameters extraction nuance. Lastly, the consistency of our simulation results with the experimental results reveals the reliability and technical accuracy of model's framework.

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