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# Cooling of minimized surface-mount packages in power electronics applications

***Abstract***. *With rise of GaN and SiC semiconductors in last few years, amount of available power semiconductors in minimized surface mount packages significantly increased. Together with rising pressure to increase power density of power conversion systems became effective design of cooling crucial. The aim of this article is to propose innovative methods of cooling of minimized surface mount packages, especially in application of power electronics. Article presents FEM thermal simulation of several possible variants of problem solution and provides results of measurement on physical prototypes with intention to compare. Results shows that the future of cooling in power electronics belongs to printed circuit boards with metal substrate.*

***Streszczenie.*** *Badano chłodzenie układów elektronicznych bazujących na GaN i SiC przy minimalizacji wymiarów I zwiększaniu gęstości mocy. Przedstawiono analizę rozkładu temperatury wybranych układów Najlepsze rezultaty osiągnięto dla obwodów drukowanych z metalowym podłożem. (**Chłodzenie elementów elektronicznych przy minimalizacji ich wymiarów**)*

**Keywords:** power electronics, thermal vias, thermal management, surface mount package cooling, cooling of GaN.
**Słowa kluczowe:** układy elektroniczne, chłodzenie, rozkład temperatury.

## Introduction

In the last few years amount of available fast switching, wide bandgap devices (especially Gallium Nitride semiconductors) for power electronics application significantly increased. For proper operation of those novel switching devices is critical to eliminate parasitic inductances in circuit, which leads into a brand-new trend of minimized, surface mount packages in power electronics. On the one hand, improved switching performance by low inductive packages helps to reduce power loss of the device during switching, on the other hand, makes cooling of the device much more challenging. Comparing to industrial standard lead packages (TO-220, TO-247), which were in most of the cases directly attached to heatsink with a screw over insulating thermal interface, is now necessary to design more sophisticated heatsink structure. Design cooling of the device as a part of the printed circuit board (PCB) itself.

If we take a look at the nowadays portfolio of GaN devices available on the market, we can split it onto two groups based on the position of the cooling pad versus the printed circuit board - top and bottom cooled surface mount packages. Most of the devices are available in both options, some of the manufacturers are designing semiconductors packages in a mirrorable way - only shape of electrical connections is defining cooling requirements (for example Infineon's PDSO). As the "top side" cooling is relatively straight forward and directly dependent on insulating material performance, bottom side cooling – transfer of a heat over printed circuit board to the heatsink will be the aim of following chapters.

## Theory of heat transfer over PCB

Considering the device manufactured with a cooling pad on a same side as electrical connection is the heat transferred over the PCB (single side SMT) to the heatsink attached over insulating interface, which is at same time providing electrical insulation. Major benefit of this solution is simple manufacturing process, which is important to maintain quality in mass production. Disadvantage is the additional temperature increase on thermal resistance of the assembly, which is limiting the maximal power loss of the device, therefore limiting its performance by maximum temperature.

Analysis of overall temperature resistance of PCB in bottom side cooling system can be divided into two main contributors – insulating material and copper layers.

Performance of insulating material is defined by production technology of PCB and operating voltage level – material and thickness of core/pre-preg layers.

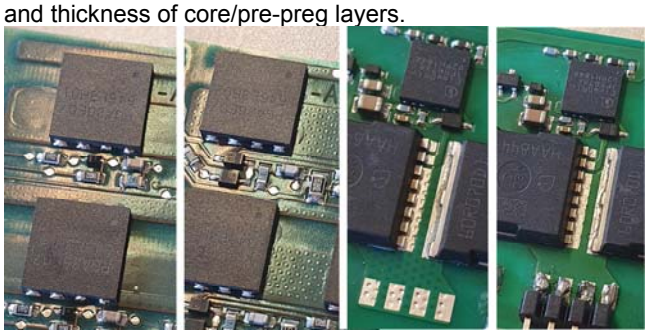

Fig.1. Photo of four evaluated prototypes in this article

In case of FR4 base material is the contribution to cooling very low (0,35$Wm^{-1}K^{-1}$) which is in opposite to expensive ceramic material based solutions (Aluminium Nitride ceramic 140$Wm^{-1}K^{-1}$). Goal in all cases is to choose material which can provide sufficient electrical insulation to the heatsink. In case of low thermal conductivity of material is right strategy to bridge PCB by conductive material and add additional insulating layer, which can provide also mechanical fixing (e.g. Sticky foil Arlon Secure 1500KT2).

Contribution of copper layer to cooling is mainly in distributing heat in planar (X, Y) direction, which increases area of heat transfer over thermally lower conductive material. In high frequency switching applications needs to be kept in mind capacity of cooling pad to ground (typ. Heatsink), which is affecting device performance and adding switching losses. Therefore, is increase of cooling pad area possible only in limited extend.

All of those assumptions can be considered as a start point for a successful cooling design and are based on well-known formula:

(1) $$R_\vartheta = \frac{1}{\lambda} \cdot \frac{l}{S}$$

where: $R_\vartheta$ – thermal resistance [$KW^{-1}$], $\lambda$ – thermal conductivity [$Wm^{-1}K^{-1}$], $l$ – length [m], S – area of heat transfer [$m^2$]

With intention to determine solution with minimum possible thermal resistance of printed circuit board, several examples are presented in following chapters. All examples are complete half-bridge with insulated driver.

**PCB with copper inlays**

In case of printed circuit boards with low thermal conductivity of base material (FR4), is the right approach to thermally "bridge" it by using material with higher thermal conductivity (ideally copper, 400Wm$^{-1}$K$^{-1}$).

This idea is fulfilled by Copper inlay technology - which is a pre-milled copper shape protruded over milled opening in standard, several layer PCB. This design style is ideal for carrying high currents over PCB, seen in automotive applications. In experiment case, is the cooled surface mount device directly soldered to the copper inlay and the heat is transferred through the high performance thermal conductive paste to the heatsink.

Performance of this solution evaluated on a porotype is displayed in figure 4. Power losses assigned to the four devices are 20W, two transistors in parallel in a half bridge application (5W for every transistor chip). Heatsink temperature is 30.8°C, PCB surface temperature is 39.3 °C, resulting in thermal resistance from PCB surface to the heatsink side $R_{\vartheta PCB}$ = 0.85 KW$^{-1}$. Thanks to the very nonstandard manufacturing process, copper inlays are from a cost point of view not an attractive solution.

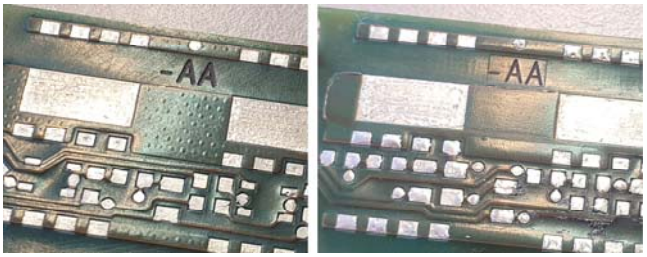


Fig.2. Surface view on six-layer PCB with filled and caped thermal vias (left) and copper inlay (right)

**PCB with thermal vias**

Alternate solution to copper inlays is the PCB using standard manufacturing process - high amount of vias with an intention to transfer heat efficiently. Design and effectivity of this solution is hardly dependent on PCB manufacturer capabilities – especially maximum hole/via plating thickness (Fig.3 - c), distance between drilled holes (Fig.3 - k) and the hole diameter itself (Fig.3 - D).

Considering dimensions displayed on drawing (Fig.3) and a fact, that for a lowest thermal resistance of PCB the highest area of copper should be achieved (equation 1) - triangular organization of vias is using manufacturing capabilities in most effective way. Comparing to frequently seen square pattern [1][9], brings triangular pattern 15.5% more copper vs. area ratio which is directly reflected in performance.

By comparing area of the "useful" copper transferring heat in Z direction to the total PCB area, following formula can be constructed **Błąd! Nie można odnaleźć źródła odwołania.**. Derivation (=0) of this equation shows the optimum for a defined via plating thickness and drilled hole distance, points A and B highlighted in figure 5 are manufacturable.

$$k_{vias} = \frac{A_{Cu}}{A_{PCB}} = \frac{2.\pi.(D.c - c^2)}{\sqrt{3}.(D+k)^2} \tag{2}$$

where: $A_{Cu}$ – total area of copper active in Z direction [m$^2$], $A_{PCB}$ – total area [m$^2$], $D, c, k$ – dimensions displayed on picture below [m]

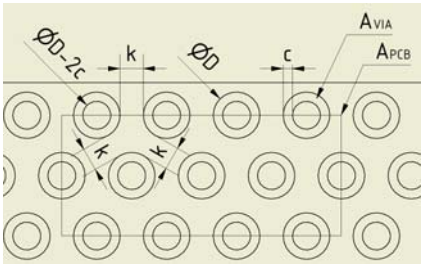


Fig.3. Parameters of printed circuit board thermal vias (top view)

As centralized power losses are expected (transistor assembled on PCB), thickness of top layer is not negligible, as it is distributing heat in X/Y axis and making vias on a side (more away from device) effectively contributing to heat transfer. FEM simulation (point A and B, figure no. 5) has proven that higher copper fill factor is leading to a lower thermal resistance of PCB – model B was chosen as a reference for a physical realisation. Limiting factor for a top layer thickness is a pitch of components used, in case of any QFN package used, is thickness limited to 1oz (40µm - experiment case). Figure no. 4 shows thermal camera snapshot of optimized version, power losses assigned to the four devices exactly the same as in copper inlay case (5W for every transistor chip). Thermal resistance from PCB surface to the heatsink side is $R_{\vartheta PCB}$ = 0.87 KW$^{-1}$.

Both presented solutions, copper inlay and thermal vias, are only passing the heat over the FR4 PCB without electrical insulation. In case where potential of cooled device needs to be insulated from heatsink, is necessary to include insulating interface resistance into total $R_{\vartheta}$ calculation, resulting in significantly lower performance. As the surface of the PCB might contain deviations, is attaching of thermal conductive foil to the surface not a trivial task – any defects in application (bubbles) lead into reduced performance.

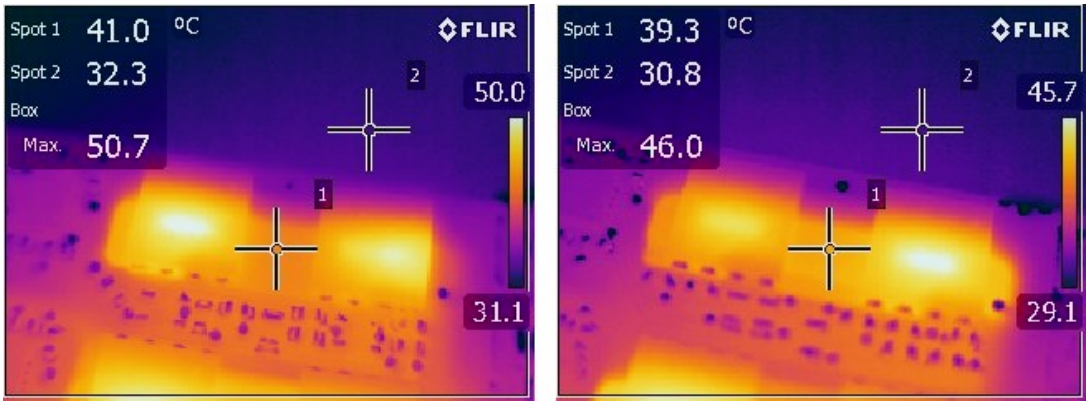


Fig.4. Thermal camera picture of FR4 based PCB – copper inlay (right), optimized thermal vias (left). Spot no.2 represents the heatsink temperature

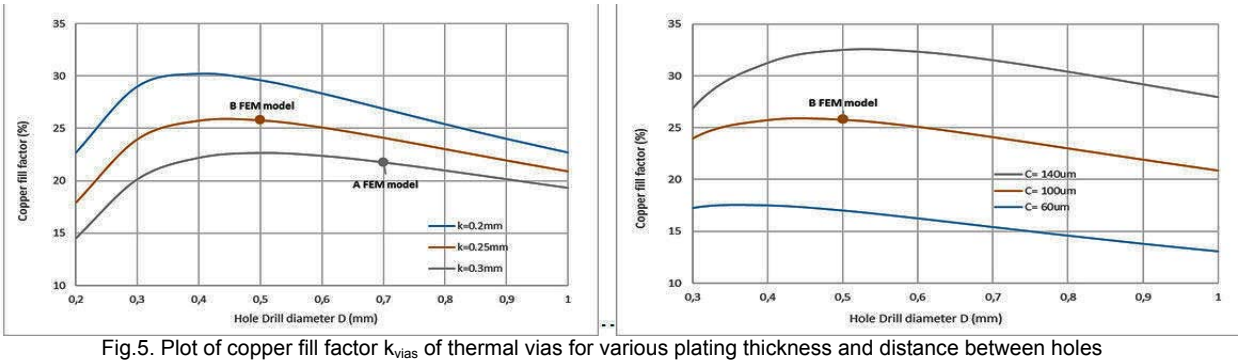


Fig.5. Plot of copper fill factor $k_{vias}$ of thermal vias for various plating thickness and distance between holes

**PCB on Insulated Metal Substrate**

To achieve better performance in terms of thermal resistance and at same time providing electrical insulation, temperature increase over electrically insulating interface between PCB and Heatsink needs to be reduced - step into more advanced technology is needed – insulated metal substrate PCB (IMS). This technology is well adopted in automotive lighting application for the same purpose – cooling of surface mount LEDs. For use of IMS PCB in power electronics is necessary to use material between layers and substrate with proper voltage insulation, dielectric parameters and keep distances of components/traces from edges to meet sufficient creepage/clearance according to IPC9592. Thermal performance of nowadays available insulating materials suitable for high voltage application (e.g. Arlon 92ml, x-y axis 3.5 $Wm^{-1}K^{-1}$, z-axis 2 $Wm^{-1}K^{-1}$) is comparable to insulating capton based materials mentioned in previous chapter. Manufacturing process of IMS PCB allows to reduce thickness of insulating layer significantly (typ. from 70-150µm), which is reflected in overall performance.

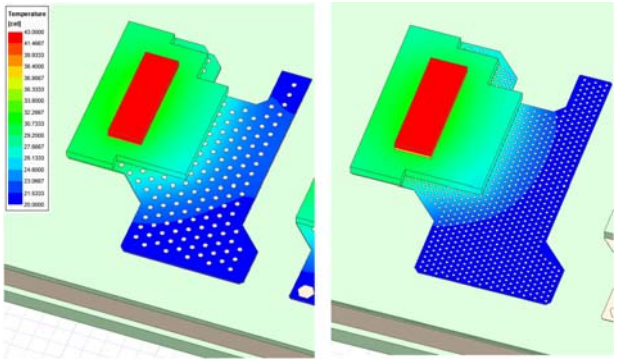

Fig.6. Thermal simulation of Insulated Metal Substrate PCB

From cooling point of view, is ideal to design IMS board as a single layer board. Based on conducted FEM simulations, is the cooling pad copper thickness and size significantly affecting final performance. Major design constrain is the placement and routing of a MOSFET driver, which is not possible on a single copper layer. Possible solution is installing another FR4 PCB on top of IMS [5], and bring the driver signals over the connector, which is from low inductive layout and reliability not optimum. Right approach in this case seems to be a dual layer IMS.

**Multilayer PCB on Insulated Metal Substrate**

With dual layer IMS is thickness of insulating interface nearly doubled (depends on voltages between layers) and performance is therefore reduced.

By using thermal vias described in previous chapter is possible to “gain back” part of the performance of single layer solution, by bridging the intermediate insulating layer (Fig. 7.). Same equations as in previous chapter can be applied, therefore higher copper fill factor of vias pattern should lead to a better thermal performance. Based on results of FEM simulation were selected two optimized variants of thermal vias pattern, manufactured with different production processes.

**Variant A** – drilled vias with diameter D = 0.5mm with industrial standard plating c = 40um, distance between holes k = 0.25mm. Thickness of layers 150µm/150 µm (fill factor $k_{vias}$ = 11.87%)

**Variant B** – high dense laser drilled D = 0.15mm copper filled micro-vias, distance between holes k = 0.2mm ($k_{vias}$ = 16.66%). As the laser drill technology was used, the middle layer thickness needs to be reduced to avoid any defects in micro-vias plating. Therefore, is the layer thickness 100µm/150µm.

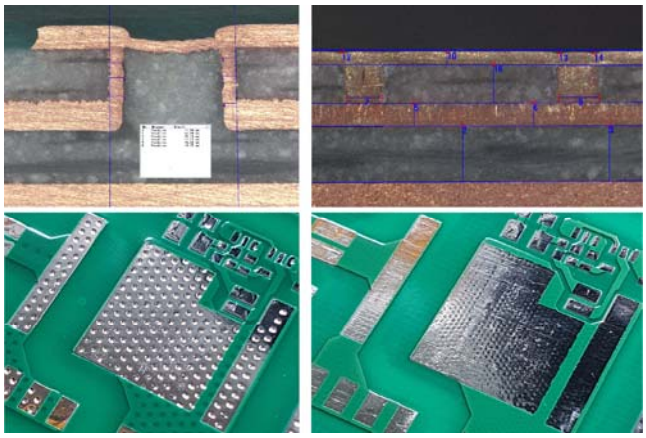

Fig. 7: Micro-section analysis and surface photos of tested prototypes - variant A (left), variant B (right)

Thermal camera pictures of variant A and B are shown in figure no. 8. With small difference caused mainly by production tolerances of prototypes, results are matching the simulation. As expected, higher copper fill factor shows lower thermal resistance. Graph displayed in figure no. 6 shows simulation result of IMS board without vias, therefore impact of thermal vias is visible. Differences between tested variants A and B are not significant, as the vias are affecting the heat transfer only over part of the total thickness. In order to make all presented solutions comparable, power loss assigned to devices in both cases the same as for FR4 based PCBs – 10 Watts per switch. All simulation models were created in Ansys ICEPAK 2020 R1

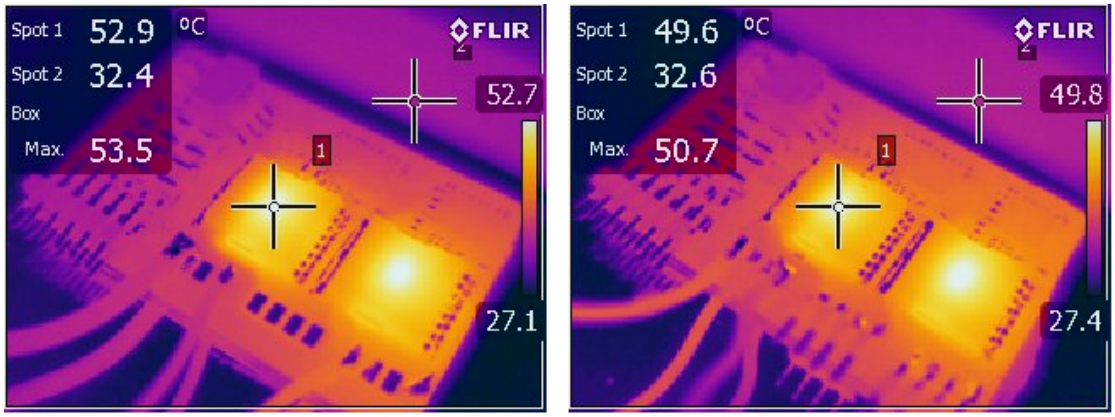


Fig.8. Thermal camera picture of IMS PCB - variant A (left), variant B (right). Spot no.2 represents the heatsink temperature.

## Conclusion

Several configurations of printed circuit board for cooling of minimized surface mount packages in power electronics application were presented. From simulation results and measurement on physical prototype is clear, that best results in terms of thermal resistance from package to heatsink can be achieved by using insulated copper metal substrate PCB technology. In addition, performance might be improved by using optimized thermal vias matrix down to outstanding 0,81KW$^{-1}$. Presented examples contain insulated GaN gate driver, routed on two layers without any design constrains.

Solutions based on multilayer FR4 PCB are suitable mainly for applications, where cost saving is the main decision factor. Achieved thermal resistance (fig. 4.) over PCB itself is comparable to IMS and sufficient for applications, where high voltage insulation is not required. By adding additional thermal insulating interface is overall performance of FR4 variants significantly reduced.

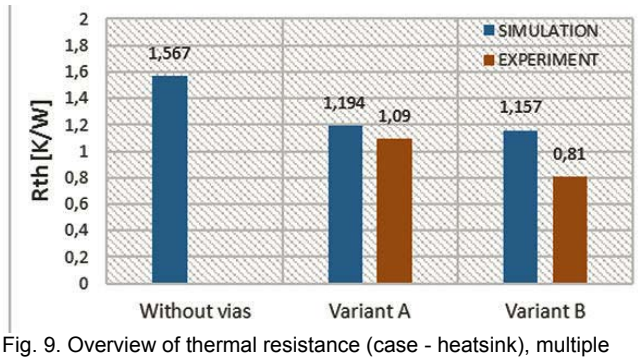


Fig. 9. Overview of thermal resistance (case - heatsink), multiple versions of IMS PCB

Based on the presented result is well understandable capability in terms of cooling performance, which helps to select right approach for use of novel widebandgap devices (GaN, SiC) in a specific application.

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## REFERENCES

[1] D. S. Gautam, F. Musavi, D. Wager, and M. Edington, "A comparison of thermal vias patterns used for thermal management in power converter", *2013 IEEE Energy Conversion Congress and Exposition*, pp. 2214-2218, 2013.

[2] A. Fodor, R. Jano, G. Chindris, and D. Pitica, "Thermal via placement for high-power applications", *2017 IEEE 23rd International Symposium for Design and Technology in Electronic Packaging (SIITME)*, pp. 223-226, 2017.

[3] C. Negrea, P. Svasta, G. Chindris, and D. Pitica, "Modeling of thermal via heat transfer performance for power electronics cooling", *2011 IEEE 17th International Symposium for Design and Technology in Electronic Packaging (SIITME)*, pp. 107-110, 2011.

[4] P. Skarolek, J. Lettl, G. Chindris, and D. Pitica, "GaN Transistors Cooling Options Comparison", *2011 IEEE 17th International Symposium for Design and Technology in Electronic Packaging (SIITME)*, pp. 323-326, 2019.

[5] J. L. Lu, R. Hou, D. Chen, and D. Pitica, "Opportunities and design considerations of GaN HEMTs in ZVS applications", *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 880-885, 2018.

[6] A. P. Catalano, R. Trani, A. Castellazzi, and V. d'Alessandro, "Analytical Modeling of Through-PCB Thermal Vias and Heat-Sinks for Integrated Power Electronics", in *2019 25th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2019, pp. 1-6.

[7] X. Jorda, X. Perpina, M. Vellvehi, J. Millan, and A. Ferriz, "Thermal characterization of Insulated Metal Substrates with a power test chip", in *2019 25th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)*, 2009, pp. 172-175.

[8] T. A. Asghari, X. Perpina, M. Vellvehi, J. Millan, and A. Ferriz, "PCB Thermal Via Optimization using Design of Experiments", in *Thermal and Thermomechanical Proceedings 10th Intersociety Conference on Phenomena in Electronics Systems, 2006. ITHERM 2006*, 2006, pp. 224-228.

[9] J. Nicolics, M. Mundlein, M. Fasching, J. Millan, and A. Ferriz, "Minimization of the Thermal Interface Resistance of Power SMD Assemblies for High-Temperature Applications", in *2006 29th International Spring Seminar on Electronics Technology*, 2006, pp. 49-54.