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Novel Modified Non-Isolated DC-DC Boost Converter Based on Voltage Lift Technique

***Abstract**. In this paper, a novel DC-DC boost converter based on the voltage lift technique is manifested. It is firmly reasoned that, with a lesser number of elements, the proposed converter can yield analogously high voltage gain than that of the recently published DC-DC boost converters. The proposed converter is anticipated to provide higher efficiency due to its substantial voltage gain at a comparatively low duty cycle. Finally, to validate the acquired simulation results, a small-scale laboratory prototype is implemented and compared with the theoretical interpretation.*

Streszczenie.** Przedstawiono nowy przekształtnik DC-DC typu boost bazujący na technice voltage lift. Przy mniejszej liczbie elementów yen przekształtnik ma on lepsze parametry niż przekształtniki opisywane w literaturze. Skonstruowano I zbadano prototyp przekształtnika. **Nowy typ przekształtnika DC-DC typu boost bazujący na technice voltage lift.

Keywords: DC-DC boost converter; Voltage Lift technique; Renewable Energy.
Słowa kluczowe: przekształtnik DC-DC, przekształtnik typu boost.

1.Introduction

Advances in technology and sharp elevation in human living standards have caused significant augmentation in world energy demand over the last decade. To meet this growing energy demand employing the conventional power generation methods (using fossil fuels) induces adverse environmental effects, such as greenhouse effect, air pollution due to emission of SO2 and Nitrogen oxides, etc. [1]. For years, researchers have demonstrated a substantial inclination towards the boundless other alternate energy sources such as fuel cells, wind energy, photovoltaic (PV) systems, and batteries that feature cleanliness and sustainability. However, energy resources such as principally photovoltaic cells and fuel cells yield significantly lower voltage levels (up to 50V). Therefore, high step-up DC-DC converters are greatly encouraged to boost up this low voltage for various applications [2-3]. Conventional non-isolated step-up PWM converters such as boost, buck-boost, and SEPIC, etc., possess noticeable features in regards to its simplicity and cost-effectivity. Unfortunately, the gain of these converters is limited due to circuit parameters and operation at high duty cycles to attain high voltage gains, which in results reduces the converter efficiency to a paramount extent. Various voltage-boosting techniques have been elucidated in the literature to achieve augmented gain while operating at low duty cycles and improved efficiency [4-6].

Major voltage-boosting techniques that can be found in the literature are segregated into five categories, namely, Switched Capacitor (SC), voltage multiplier, switched inductor, and voltage lift (VL), magnetic coupling, and converters with multistage/-level structures. New power converter topologies with the inclusion of the above voltage-boosting techniques are continuously being proposed and developed to meet the rising demand for power conversion applications [7]. Switched-capacitor can achieve high-voltage conversion gain [8-9]. However, these converters require several switches, which increases the complexity of the control strategies and associated driving circuitry. This converter topology also suffers from poor regulation, which results in pulsating input current. A number of voltage multiplier circuits are presented in the literature for high boost applications as they are easy to implement in any circuit [10-11]. However, a number of cells required for high gains also multiplies, which results in enhanced power loss, cost, and circuit size. The magnetic coupling-based boosting technique for isolated and non-isolated converters is consistently proposed [12-13]. Even though, these converters have dominant boost ability; however, they suffer from obvious drawbacks. For instance, leakage inductance must be recycled to avoid significant voltage spikes. Furthermore, with the increment of turns ratio converter size also tends to increase. Multilevel DC-DC converters are suitable for high-power high-voltage applications [14-15]. Despite various noticeable advantages such as high-power density, modularity structure, and reliability, these converters also require a large number of components, high-priced and deteriorated efficiency, due to a higher number of stages.

Eventually, among the aforementioned voltage-boosting techniques, voltage lift (VL) technique is a prestigious, relatively simple and amenable in many converters. This technique has been widely employed in the literature introduced by Luo (VL Luo converters) [16-17]. VL technique utilizes fundamental energy storage elements (inductors and capacitors) in conjunction with power semiconductor switches and diodes to boost the input voltage level to higher voltage levels. The energy storage elements transfer the low input energy (in steps) to the output capacitor with a much higher level because of its storage capabilities. High power density, greater efficiency, plain structure and cost-effectiveness, and small output voltage ripple as compared to the other techniques are the crucial features of this technique. Furthermore, the lack of additional switches that lead to the complexity of the control system of a DC-DC converter is a prominent outcome of this technique.

In this paper, a modified non-isolated structure of a conventional boost converter using a single switch is proposed to achieve a high voltage gain. The proposed converter possesses the capability of achieving high voltage gain at reasonably low duty cycle, which makes it more suitable for medium and high voltage applications, for instance, in DC microgrids. The converter can be used to interface various low power voltage sources like batteries, photovoltaic (PV) panels, and fuel cells into a common DC bus (380V) voltage. The extensive operation of the proposed converter is also analyzed both in CCM and DCM. The efficiency of the proposed converter is evaluated at different duty cycles and is illustrated graphically.

2.Structure of the proposed Converter

The proposed structure is elucidated in Fig 1 which is encompassed of three inductors, a single switch, four capacitors, and four diodes. The operation of the switch is controlled by a PWM technique with a switching frequency of 25 kHz. To simplify the analysis of the proposed

converter, few assumptions are made. i) To eradicate the inconsistent behavior of the converter, the steady-state operation of the converter is considered. ii) The voltage ripple for each capacitor is neglected due to a sufficiently large capacitor value; therefore, the capacitor's voltage in each switching period is identical. iii) The switch and diodes are considered ideal.

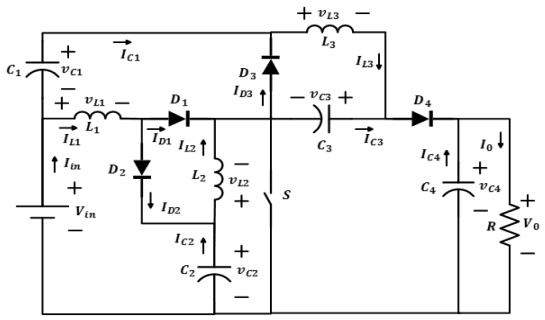

Fig 1. Structure Proposed converter.

2.1.Operation of the Proposed Converter in CCM

The key focus of this section is to elaborate the CCM operation of the proposed circuit performed in PSIM software extensively. Various waveforms are presented for capacitors, diodes, switch, and inductors, which incorporates both on-switching and off-switching states. Moreover, theoretically current and voltage relationships that signify the operation of the converter are also established. Fig 2(a) and (b) dictates equivalent circuits of the proposed converter during time T_{on} and T_{off} (grey color indicates off state of diodes).

During the on switching period, diodes , D_2 and D_3 are reverse biased and diode D_1 is forward biased. In this state, supply voltage V_1 is providing energy to the inductor L_1 and hence its current value is linearly increased from its minimum value I_{LV1} to its peak value I_{LP1} as illustrated in Fig 3(a). In the meanwhile, Capacitor C_2 is discharged through the inductor L_2 by releasing its stored energy. The voltage of the Capacitor C_2 is dropped to the lowest value V_{CV2} Fig 3(b). and inductor L_2 current is raised from the lowest value I_{LV2} to its highest value I_{LP2}. Also, the capacitor C_1 is discharged through the inductor L_3 and capacitor C_3 As a result, capacitor C_1 voltage is dropped to the lowest value v_{CV1} and current in the inductor L_3 is augmented from its minimum value I_{LV3} to its maximum value I_{LP3} Fig 3(c), while the voltage of the capacitor C_3 is raised from its minimum value V_{CV3} to its maximum value V_{CP3} as shown in Fig 3(d). During on-period, the load is isolated from rest of the circuit as D_4 is reverse biased, capacitor C_4 is providing energy to the load and its voltage is dropped from its maximum value V_{CP4} to the lowest value V_{CV4}.

During the off-switching period, diodes $\boldsymbol{D_2,D_3}$ and $\boldsymbol{D_4}$ are forward biased and diode $\boldsymbol{D_1}$ is reverse biased.Inductor $\boldsymbol{L_1}$ is providing energy to Capacitor $\boldsymbol{C_2}$ by losing its stored energy and capacitor's $\boldsymbol{C_2}$ voltage is raised from the lowest value $\boldsymbol{V_{CV2}}$ to maximum value $\boldsymbol{V_{CP2}}$, while current in the inductor is dropped to a minimum value $\boldsymbol{I_{LV1}}$. Also inductor $\boldsymbol{L_2}$ is supplying energy to a capacitor $\boldsymbol{C_1}$ by liberating its stored energy and voltage of $\boldsymbol{C_2}$ is raised to a peak value of $\boldsymbol{V_{CP1}}$ thereby the current in the inductor $\boldsymbol{L_2}$ is dropped to $\boldsymbol{I_{LV2}}$. Inductor $\boldsymbol{L_3}$ and capacitor $\boldsymbol{C_3}$ both are supplying energy to the capacitor $\boldsymbol{C_4}$ and load. Current in inductor $\boldsymbol{L_3}$ is reduced to $\boldsymbol{I_{LV3}}$ while the voltage of the capacitor $\boldsymbol{C_3}$ is dropped to V_{CV3} and voltage of the capacitor C_4 is raised to a peak value of V_{CP4}.The voltage and current waveforms of the diodes in CCM are shown in Fig 4.

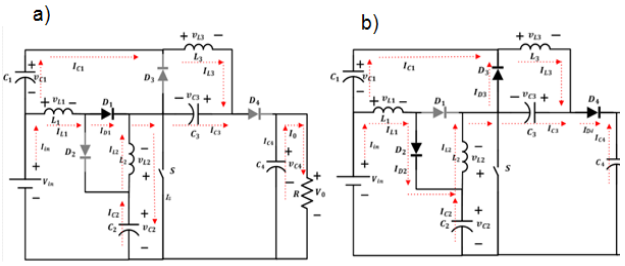

Fig 2. Proposed converter (a) during the on-switching period; (b) during the off- switching period.

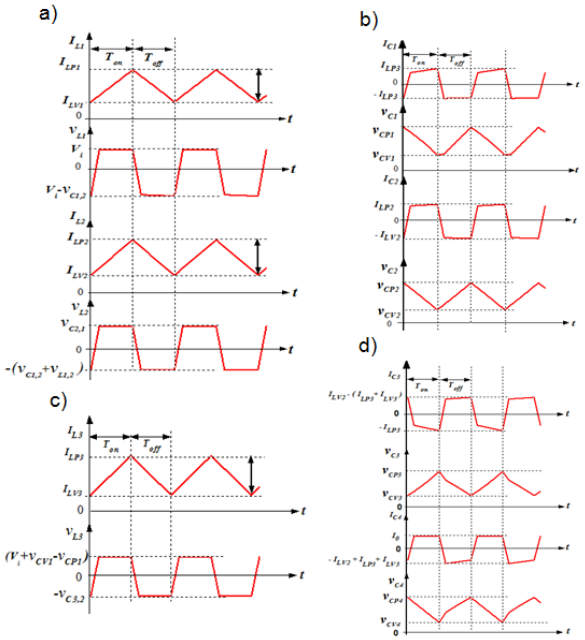

Fig 3. The current and voltage waveforms in CCM for; (a) inductors L_1, L_2; (b) Capacitors C_1, C_2; (c) inductor L_3; (d) Capacitors C_3, C_4.

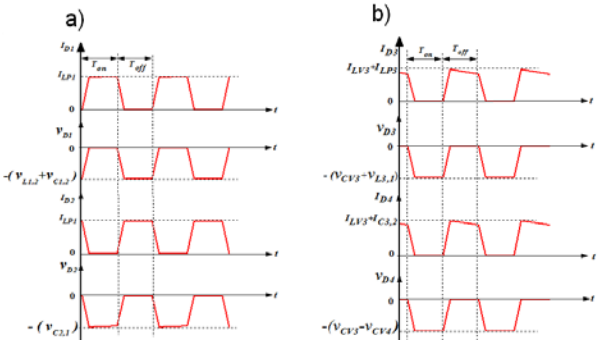

Fig 4. The current and voltage waveforms in CCM for; (a) Diodes D_1, D_2; (b) Diodes D_3, D_4.

Voltage and current equations of inductors in CCM:

When the switch is on, inductors L_1, L_2 and L_3 voltages, and currents are obtained as:

(1)

$$\begin{cases} v_{L1,1} = V_i = L_1 \dfrac{di_{L1,1}}{dt} = \dfrac{\Delta i_{L1,1}}{T_{on}}, i_{L1,1} = \dfrac{V_i}{L_1} t + I_{LV1} \\ v_{L2,1} = L_2 \dfrac{di_{L2,1}}{dt} = v_{C2,1} = \dfrac{V_i}{(1-D)}, i_{L2,1} = \dfrac{v_{C2,1}}{L_2} t + I_{LV2} \\ v_{L3,1} = L_3 \dfrac{di_{L3,1}}{dt} = v_{L1,1} + v_{C1,1} - v_{C3,1}, i_{L3,1} = \dfrac{\left(v_{L1,1} + v_{C1,1} - v_{C3,1}\right)}{L_3} t + I_{LV3} \end{cases}$$

In the time interval of T_{off}, inductors L_1, L_2 and L_3 voltages and currents are as follow:

(2)

$$\begin{cases} v_{L1,2} = V_i - v_{C2,2} = L_1 \dfrac{di_{L1,2}}{dt} = -\dfrac{\Delta i_{L1}}{T_{off}}; i_{L1,2} = -\dfrac{\left(V_i - v_{C2,2}\right)}{L_1} t + I_{LP1} \\ v_{L2,2} = v_{C3,2} + v_{C2,2} - V_0 = L_2 \dfrac{di_{L2,2}}{dt}; i_{L2,2} = -\dfrac{\left(v_{C3,2} + v_{C2,2} - V_0\right)}{L_2} t + I_{LP2} \\ v_{L3,2} = L_3 \dfrac{di_{L3,2}}{dt} = -v_{C3,2}; i_{L3,2} = \dfrac{v_{C3,2}}{L_3} t + I_{LP3} \end{cases}$$

Voltage and current equations of capacitors in CCM:
By using inductor volt-sec balance rule forinductors L_1, L_2 and L_3 and applying KCL (Fig 2(a) and (b)), Capacitors C_1, C_2, C_3, and C_4 voltages and currents can be earned as:

(3)

$$\begin{cases} v_{C1,1} = v_{C1,2} = v_{C1} = \dfrac{V_i\left(2D - D^2\right)}{\left(1-D\right)^2}; I_{C1,1} = I_{L3,1}, I_{C1,2} = I_{L3,2} + I_{C3,2} - I_{L2,2} \\ v_{C2,1} = v_{C2,2} = v_{C2} = \dfrac{V_i}{\left(1-D\right)}; I_{C2,1} = I_{L2,1}, I_{C2,2} = I_{L3,2} - I_{L1,2} \\ v_{C3,1} = v_{C3,2} = v_{C3} = V_0 - \dfrac{V_i}{\left(1-D\right)^2}; I_{C3,1} = -I_{L3,1}, I_{C3,2} = I_{L2,2} + I_{C1,2} - I_{L3,2} \\ v_{C4,1} = v_{C4,2} = v_{C4} = V_0 = \dfrac{(1+D)}{\left(1-D\right)^2} V_i; I_{C4,1} = -I_0, I_{C4,2} = I_{L3,2} + I_{C3,2} - I_0 \end{cases}$$

Voltage and current equations of Diodes in CCM:
During T_{on} and T_{off}, Diodes voltages and currents can be written as:

(4)

$$\begin{cases} V_{D1} = -(V_{C1} + V_{L1,1}), I_{D1} = i_{L1,1} \\ V_{D2} = V_{in} - V_{L1,2} - V_{C2}, I_{D2} = i_{L1,2} \\ V_{D3} = -(V_{L3,2} + V_{C3}), I_{D3} = i_{L3,2} - i_{C1,2} \\ V_{D4} = V_{C3} - V_{C4}, I_{D4} = i_{C3,2} + i_{L3,2} \end{cases}$$

Voltage gain and current ratio of the proposed converter in CCM:
With an assumption of a lossless converter, voltage gain and current ratio are deducted as:

(5)

$$\begin{cases} \dfrac{V_0}{V_i} = \dfrac{(1+D)}{\left(1-D\right)^2} \end{cases}$$

(6)

$$\begin{cases} \dfrac{I_0}{I_i} = \dfrac{\left(1-D\right)^2}{(1+D)} \end{cases}$$

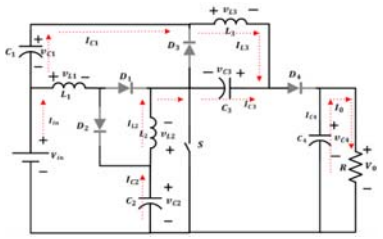

Fig 5. Proposed Converter during discontinuous inductor current (t_2-t_3).

2.2.Operation of the proposed high step-up converter in DCM:

In this section operation of the proposed converter in DCM is extensively analyzed. Various modes of operation are enlightened, and key waveforms are illustrated in DCM operation. The proposed converter has three modes of operation during DCM. The equivalent circuits during DCM operation are shown in Figs.2 and 5. The characteristic waveforms during DCM are also demonstrated in Figs (6-8).

Mode I:

When the switch is on, i.e., at the time (t_0 - t_1), diodes D_2 ,D_3 and D_4 are reverse biased and diode D_1 is forward biased as shown in Fig 2(a). Input voltage V_i provides energy to the inductor L_1 and its current is increased to a maximum value I_{LP1} (Fig 6(a)). Also, capacitor C_2 is discharged through the inductor L_2 and its voltage is dropped to the lowest value V_{CV2} (Fig 7(a)). This energy is stored by the inductor L_2 and its current is raised from the lowest value I_{LV2} to its highest value I_{LP2}. In the meanwhile, capacitor C_1 is supplying energy to the inductor L_3 and capacitor C_3 and current of the inductor L_3 is raised to its maximum value I_{LP3} (Fig 6(b)) while the voltage of the capacitor C_3 reaches to the highest value V_{CP3} (Fig 7(b)). During this time interval, the voltage of the capacitor C_1 is dropped to its minimum value V_{CV1}. Since diode D_3 is reverse biased, capacitor C_4 is providing energy to the load and its voltage is dropped to its lowest value V_{CV4}.

Mode II:

During the off-switching period at a time (t_1- t_2), diode D_1 is reverse biased and diodes D_2,D_3 and D_4 are forward biased as illustrated in Fig 2(b). Inductor L_1 is supplying energy to the capacitor C_2 and its current falls to zero at the end of time interval (t_1- t_2) as shown in Fig 7(a), while the voltage of the capacitor C_2 is increased to its maximum value V_{CP2} . Also, inductor L_2 current falls to zero at the end of time interval (t_1-t_2) Fig 6(a), providing energy to the capacitor C_1 thus its voltage is increased to the highest value V_{CP1}.During this time, inductor L_3 and capacitor C_3 both are supplying energy to the capacitor C_4 and load and thus the voltage of the capacitor C_4 is reached to a peak value V_{CP4} (Fig7(b)) Current in inductor L_3 is reduced to zero while the voltage of the capacitor C_3 is dropped to the lowest value V_{CV3} at the end of the time interval (t_1- t_2).

Mode III:

At the time (t_2- t_3), all the four diodes are reverse biased (Fig 5), and current in the three inductors reaches zero as illustrated in Fig 6. Voltage of capacitors C_1 and C_2 is maintained at peak values V_{CP1} and V_{CP2} respectively as capacitor's C_1 and C_2 current is zero during this time interval. Also the voltage of the capacitor C_3 remains at the lowest value V_{CV3} during the time (t_2- t_3) as a capacitor C_3 current is zero. Capacitor C_4 continues to supply energy to the load by releasing its stored energy. Voltage of capacitor C_4 is reduced to the minimum value V_{CV4} at the end of the time interval (t_2- t_3).The currents and voltages of all the four diodes during DCM is demonstrated in Fig 8.

Voltage equations of inductors and Capacitors in DCM (at t = DT and t = $D'T$):

(7)

$$\begin{cases} v'_{L1,1} = V_i, v'_{L1,2} = V_i - v'_{C2,2}, v'_{C1,1} = v'_{C1,2} = v'_{C1} = \dfrac{V_i\left(D+D'\right)D + DD'}{\left(D'\right)^2} \\ v'_{L2,1} = v'_{C2,1}, v'_{L2,2} = \left(v'_{C3,2} + v'_{C2,2} - V'_0\right), v'_{C2,1} = v'_{C2,2} = v'_{C2} = \dfrac{V_i\left(D+D'\right)}{D'} \\ v'_{L3,1} = v'_{L1,1} + v'_{C1,1} - v'_{C3,1}, v'_{L3,2} = -v'_{C3,2}, v'_{C3,1} = v'_{C3,2} = v'_{C3} = V_0 - \dfrac{V_i\left(D+D'\right)^2}{\left(D'\right)^2} \end{cases}$$

And the gain in DCM is calculated as,

(8)

$$\frac{V_0}{V_i} = \frac{\left(D+D'\right)^2 + D^2 + DD'}{D'^2}$$

where the time intervals DT and $D'T$ are $\frac{t_0 - t_1}{T}$ and $\frac{t_1 - t_3}{T}$.

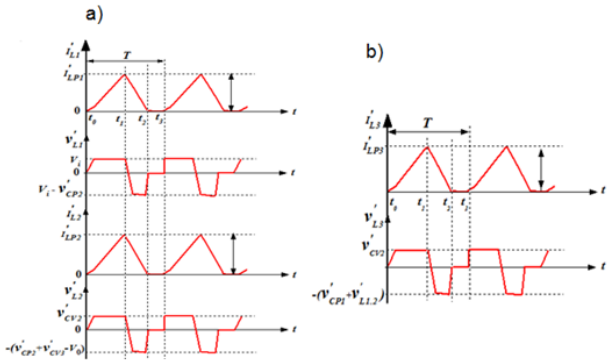

Fig 6. The current and voltage waveforms in DCM for; (a) inductors L_1, L_2; (b) inductor L_3.

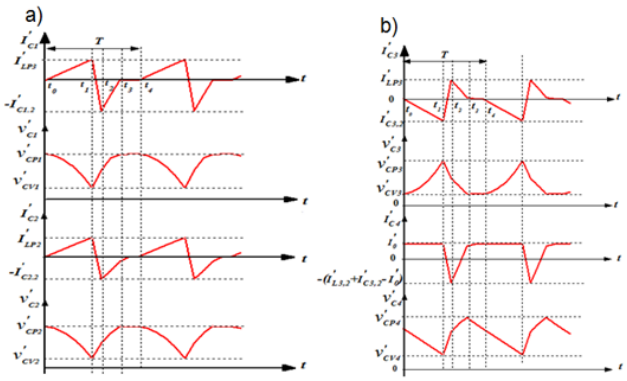

Fig 7. The current and voltage waveforms in DCM for; (a) Capacitors C_1, C_2; (b) Capacitors C_3, C_4.

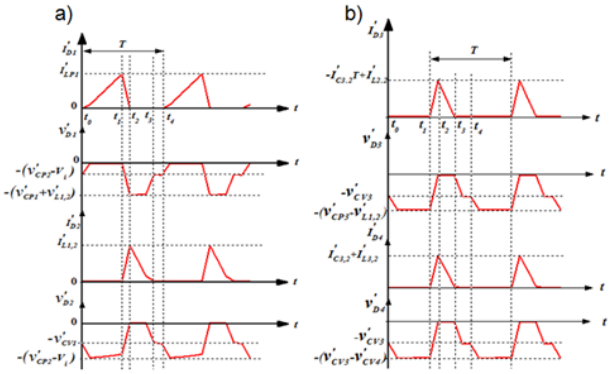

Fig 8. The current and voltage waveforms in DCM for ;(a) Diodes D_1 and D_2 ; (b) DiodesD_3, D_4.

2.3.Calculation of critical Inductance:

The critical inductance dictates the boundary between the modes of converter operation. At boundary conditions, the inductor current reaches zero, and this occurs at a critical value of inductor(s). In the proposed structure, three inductors are used; therefore, three critical values for L_1 (L_{C1}), L_2 (L_{C2}), and L_3 (L_{C3}) need to be calculated. In finding the critical values, the following equation has to be satisfied.

(9) $$I_{LV1} + I_{LV2} + I_{LV3} = 0$$

where I_{LV1}, I_{LV2}, and I_{LV3} are the minimum values of the three *inductors and must be zero*.

By using charge balance rule for capacitors and applying boundary conditions, critical values of inductors can be extracted as:

(10)

$$\begin{cases} L_{C1} = L_2(1-D)^2 \\ L_{C2} = \dfrac{1}{\left[\dfrac{D}{V_i L_3}\left\{\dfrac{2V_i - V_0(1-D)^2}{(1-D)^2 D^2}\right\} + \dfrac{2I_0 f}{DV_i}\right]} \\ L_{C3} = \dfrac{1}{2I_0 f}\left[\dfrac{V_i\left(D^2+2D-1\right) - V_0(1-D)^2 D^2 + V_0(1-D)^4}{(1-D)^2}\right] \end{cases}$$

Therefore, the converter operates in CCM when $L_1 > L_{C1}, L_2 > L_{C2}$, and $L_3 > L_{C3}$ *while operates in DCM when* $L_1 < L_{C1}$, $L_2 < L_{C2}$ *and* $L_3 < L_{C3}$. *At boundary conditions, i.e., when* $L_1 = L_{C1}$, $L_2 = L_{C2}$ *and* $L_3 = L_{C3}$ *the converter operates in critical mode.*

2.4.RMS calculation and efficiency analysis:

The RMS values of all the passive elements and semiconductor devices are determined, and the efficiency of the converter is calculated based on these values.
For the calculation of RMS values, the ripple in inductor currents and capacitor voltages are ignored. RMS values of Diodes, Capacitors, and Switch current are given as:

(11)

$$\begin{cases} I_{D1,rms} = \dfrac{I_0(1+D)}{(1-D)^2}\sqrt{D}, I_{C1,rms} = I_0\sqrt{\dfrac{D}{(1-D)}} \\ I_{D2,rms} = \dfrac{I_0(1+D)}{(1-D)^2}\sqrt{(1-D)}, I_{C2,rms} = \dfrac{I_0(1+D)}{(1-D)^2}\sqrt{D(1-D)} \\ I_{D3,rms} = I_{D4,rms} = \dfrac{I_0}{\sqrt{(1-D)}}, I_{C3,rms} = I_{C3,rms} = I_0\sqrt{\dfrac{D}{(1-D)}} \\ I_{s,rms} = \dfrac{I_0(1+D)(2-D)}{(1-D)^2}\sqrt{D} \end{cases}$$

For efficiency analysis, parasitic resistances of inductors, capacitors, diodes, and switches are taken into consideration. The parasitic on-state resistance of MOSFET is represented by r_S. Parasitic resistances of inductors and capacitors are represented by $(r_{L1}, r_{L2}, r_{L3})$and (r_{C1}, r_{C2}, r_{C3}), respectively. Forward voltage and parasitic resistances of diodes is represented by V_F and $(r_{D1}, r_{D2}, r_{D3}, r_{D4})$, respectively. Losses due to inductors, capacitors, diodes, and switch are calculated as:

(12)

$$\begin{cases} P_{L,loss} = I_{L1}{}^2 r_{L1} + I_{L2}{}^2 r_{L2} + I_{L3}{}^2 r_{L3} \\ P_{C,loss} = I_{C1,rms}{}^2 r_{C1} + I_{C2,rms}{}^2 r_{C3} + I_{C3,rms}{}^2 r_{C3} + I_{C4,rms}{}^2 r_{C4} \\ P_{D1,loss} = I_{D1,rms}{}^2 r_{D1} + V_F I_{D1,avg}, P_{D2,loss} = I_{D2,rms}{}^2 r_{D2} + V_F I_{D2,avg}, \\ P_{D3,loss} = I_{D3,rms}{}^2 r_{D3} + V_F I_{D3,avg}, P_{D4,loss} = I_{D4,rms}{}^2 r_{D4} + V_F I_{D4,avg} \\ P_{S,loss} = I_{S,rms}{}^2 r_S, P_{Switch} = \dfrac{1}{2}\dfrac{(t_r + t_f)}{T} I_{S,avg} V_S + \dfrac{1}{2}\dfrac{C_{oss}}{T} V_S{}^2 \end{cases}$$

3.The comparison analysis between the proposed converter and other high gain converters:

In this section, The performance of the proposed converter is compared with the converters mentioned in **Table 1** in terms of voltage gain, the number of elements, and current stress on the power semiconductor switch(s).

The proposed converter has a prominent performance, particularly when the high gain is required. To achieve high voltage gain, the above-mentioned converters have to operate at extremely high duty cycle, which results in degradation of the system efficiency and increases stress on circuit elements. The comprehensive comparative analysis is inspected in **Table1** to avow the noteworthy significance of the converter proposed in the study. The voltage gain of the proposed converter at D ≥ 0.6 is higher in comparison with the converters mentioned above. The curve of voltage gain variation of the proposed converter and other converters with D at CCM operation is shown in **Fig 9(b)**. Converters presented in [18] and [19] have a higher number of elements (13 and 14) with additional switch than the proposed converter (12). Moreover, the voltage gain calculated in [20] possesses negative value, which coerces to implement additional circuitry to avail positive voltage. Even though the proposed converter and previously proposed converters in [21], [22], [23], [24] have the same number of elements but the author in [21] have adopted two switches which in results increase the complexity of the system and reduce the cost-effectivity. The converter presented in [22] can achieve high voltage gain by increasing the turns ratio of the coupled inductor. However, the enhancement in turn ratio provides an increment in size and cost. Converters presented in [23] and [24] are less competent in achieving high voltage gain at low duty cycles. The gain of these converters is limited due to the operation at extreme duty ratios when high voltage gain is required.

Table 1. Comparison summary between the proposed converter and other high gain converters.

	Propo-sed con-verter	Con-verter in [18]	Con-verter in [19]	Con-verter in [20]	Con-verter in[21]	Con-verter in[22]	Con-verter in [23]	con-verter in[24]
Swi-tches	01	02	02	02	01	01	01	01
Indu-ctors	03	03	05	03	05	04	06	03
Ca-paci-tors	04	03	02	03	01	02	04	03
Dio-des	04	05	05	04	05	05	03	05
Total count	12	13	14	12	12	12	14	12
Volta ge Gain	$\frac{(1+D)}{(1-D)^2}$	$\frac{n}{D(1-D)^{n=2}}$	$\frac{-5}{(1-D)}$	$\frac{2}{D(1-D)}$	$\frac{2+n(2-D)}{(1-D)}$	$\frac{4}{(1-D)}$	$\frac{3D}{(1-D)}$	$\frac{(1+D)^2}{(1-D)}$

Table 2. Switch current comparison between the proposed converter and other high gain converters

	Switch(s) RMS Current(A)	Duty	Outp ut (V)	Inp ut (V)	Load resistor (Ω)
Propo sed	$I_{s,rms}=I_0[\frac{(1+D)}{(1-D)^2}-1+\frac{(1+D)}{(1-D)}]\sqrt{D}$	0.7	294	12	200
[18]	$I_{s1,rms}=\frac{2\sqrt{D}I_0}{(1-D)}$	0.91	294	12	200
[19]	$I_{s1,rms}=2I_0[\frac{1}{D(1-D)}+1]\sqrt{D}$	0.91	294	12	200
[21]	$I_{s,rms}=\frac{3I_0\sqrt{D}}{(1-D)}$	0.83	294	12	200
[23]	$I_{s,rms}=\sqrt{D}[\frac{2+2D(2-D)}{D(1-D)}]I_0$	0.89	294	12	200

Table 2 indicates that the current stress on the active switch of the proposed converter is less compared with other converters to achieve the same output voltage (294V) for the same input (12V). **Fig 9(a)** demonstrates the comparison of current stress on the main switch between the proposed and other converters. From the above discussion, it is concluded that the proposed converter has comparatively lesser current stress while operating at a reasonably low duty cycle. Also, the proposed converter uses a single switch and either equal or less the number of elements compared with other converters and avoid transformer or coupled inductor to achieve high voltage transfer gain.

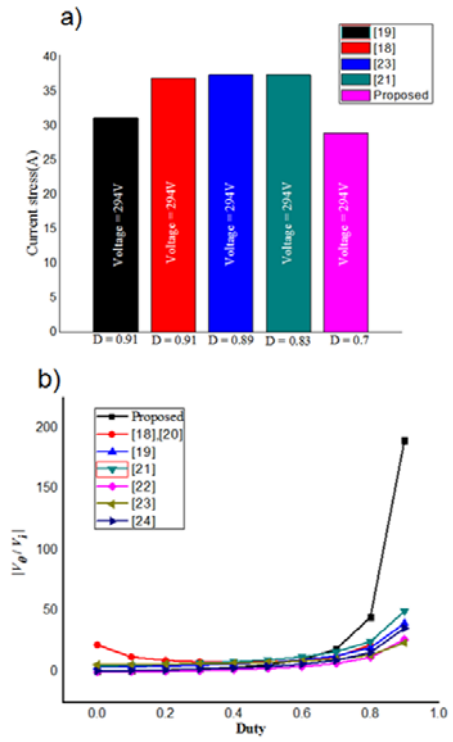

Fig 9. Comparison between the proposed converter and other converters; (a) Current stress; (b) Voltage gain.

*4.*Results and Discussion:

In this section, the results obtained from laboratory prototype and simulations are provided to acquire their validations acutely. Power loss in each converter element is computed, and the converter's efficiency is analyzed at various duty cycles. Parameters used in simulation and experimental prototype are provided in **Table 5**. The experimental prototype of the proposed converter is illustrated in **Fig 10**.

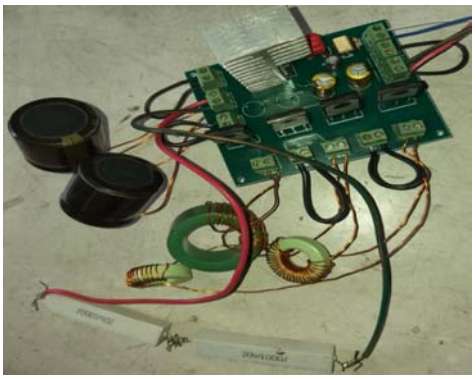

Fig 10. Experimental Prototype of the proposed converter.

Critical inductance:

For the parameter values provided in **Table 5**, Critical inductor values L_{C1}, L_{C2}, and L_{C3} are calculated as 666μH, 111μH, and 27.4μH, respectively. After incorporating these

values, the converter operates in critical mode and current in the inductors L_1, L_2, and L_3 reaches zero.

Simulation and Experimental Results for CCM:

Considering L_1= 8mH, L_2 = 5mHand L_3 = 8mH, as given in Table 5, the converter operates in CCM and the simulation results are illustrated in Figs. 3 and 4. During time T_{on}, inductor L_1 voltage reaches to 9.8 V, which is desirably consistent with the theoretical analysis presented in equation (1). While at T_{off}, inductor L_1 voltage drops to -11.9 V, which is also in accordance with the theoretical expression provided in equation (2). Similarly, at the end of the on-switching period, inductor L_2 and inductor L_3 acquired respective voltages 13 V and 13.3 V demonstrate significant consistency with theoretical results shown in equation (1). At the end of the off-switching period, the acquired voltages (-20 V and -20 V) depict prominent consistency with the results obtained from equation (2). Similarly, capacitors C_1, C_2 and C_3 the respective attained voltages such as 21.2V, 20V, and 13.3V provide the necessary validation against equation (3). Moreover, the obtained voltages (-13.3V, -20V, -33.1V, and -33.4V) of all the four diodes dictate the required confirmation for equation (4). Switch current at $t=t_{on}$ reaches 1.7 A, which follows equation(10). Furthermore, it is quite obvious from Figs. 6(a)and (b) that the variation of inductors currents having peak values 0.92 A, 0.58 A, and 0.26 A, respectively are also following theoretical expression given in equation (1) and finally all the capacitor and diode currents shown in Figs. 3 and 4 provide the validity for equation (4).

The experimental results are provided at 25 kHz switching frequency with a 40% duty cycle to demonstrate the operation of the proposed converter in CCM. Experimental waveforms of inductors, diodes, capacitors, and switch voltage are provided in Figs.11 and 12. Summary of comparison results of simulation and experiment is presented in Table 4. It can be seen that the experimental results reaffirm the simulation results at the expense of trivial differences due to the influence of parasitic elements and components available in the laboratory. The converter specification with the inclusion of parasitic elements is also shown in Table 5. The losses in each component at D = 30%, 40%, and 50% are listed in Table 3, which elucidates the significant losses occur in the diodes and inductors. The losses can be minimized by the selection of proper diode with low forward voltage drop and fine quality inductor core.

Table 3. Power loss in converter components and efficiency

	Switch	Diodes	Inductors	Capacitors	Efficiency (%)	Duty (%)
Loss (W)	0.9	1.25	1.14	0.15	83	50
	0.11	0.57	0.27	0.03	90	40
	0.03	0.41	0.09	0.014	92	30

Table 4. Comparison of simulation and experimental results of the proposed converter in CCM.

Parameters	Simulation (D=40% ,Vi=12 V)	Experiment (D=40%, Vi=12 V)
V_0	46 V	42.1V
V_{L1} , V_{L2}, V_{L3}	9.8V, 16V, 16V	11.5V, 17.3V, 17.5V
V_{C1} , V_{C2}, V_{C3}	21V, 20V, 13V	18.5V, 18.2V, 11.4V
V_{D1} , V_{D2}, V_{D3}, V_{D4}	10V, 12V, 21V, 21V	9.1V, 11.4V, 21V, 21.5V
V_S	25V	25V
I_{L1}, I_{L2}, I_{L3}	0.97A, 0.57A, 0.25A	0.89A, 0.48A, 0.2A
I_{D1}, I_{D2}, I_{D3}, I_{D4}	0.61A, 0.74A, 0.39A, 0.37A	0.5A, 0.44A, 0.21A, 0.2A
I_S	1.1A	0.92A

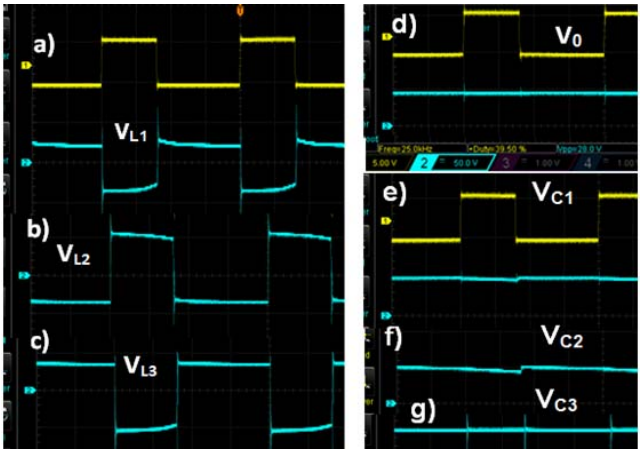

Fig 11. Experimental waveforms in CCM for; (a) inductor L_1; (b) inductor L_2; (c) inductor L_3; (d) Output;(e) Capacitor C_1;(f) Capacitor C_2; (g) Capacitor C_3.

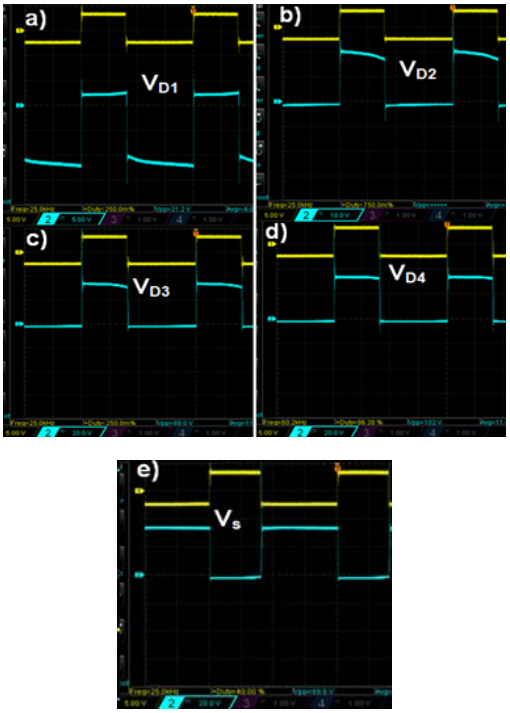

Fig 12. Experimental waveforms in CCM for; (a) Diode D_1; (b) Diode D_2; (c) Diode D_3; (d) Diode D_4;(e) Switch voltage.

Table 5. Proposed Converter specification

Parameters	CCM	DCM
R	200Ω	200Ω
L_1, L_2, L_3	8mH, 5mH, 4.5mH; r_{L1} =0.3 Ω, r_{L2} = r_{L3} = 0.2 Ω	500µH, 30µH, 15µH
C_1,C_2	8uF, 8uF; r_{C1} = r_{C2} = 0.2 Ω	8uF, 8uF
C_3,C_4	220uf, 220uF; r_{C3} = r_{C4} =0.3Ω	220uf, 220uF
Diodes	MUR3060PT; V_F= 0.8V; r_D = 0.1Ω	MUR3060PT; V_F= 0.8V; r_D = 0.1Ω
Switch	IRF460Z; r_s = 0.22Ω; t_r = 21ns; t_f = 21ns; C_{oss} = 21pF; Q_{rr} = 5µC	IRF460Z; r_s = 0.22Ω; t_r = 21ns; t_f = 21ns; C_{oss} = 21pF; Q_{rr} = 5µC
Duty cycle	D = 40%	D = 50%
V_i, f	12V, 25kHz	12V, 25kHz

Simulation and Experimental Results in DCM:

The proposed converter operates in DCM by substituting inductance values shown in Table 3. The simulation results in DCM are shown in Figs. (6-8). The voltage of the three inductors achieved to 11V, 30V, and 27V, respectively, which is following (6). The voltage of the four capacitors (C_1, C_2, C_3, C_4) shown in Fig 8 is approximately 48V, 21V, 38V, and 98V, respectively, which is confirmed by (6). Diode voltages shown in Fig 8 are 26V, 15V, 41V, and 42V, respectively, which is reaffirmed by the theoretical analysis in (6). The experimental results for DCM are provided in Fig 13. The output voltage at 50% duty cycle is 66.4 Volts, as illustrated in Fig 13(k). It can be noted that the experimental results confirm the simulation results with some small differences due to the presence of parasitic elements.

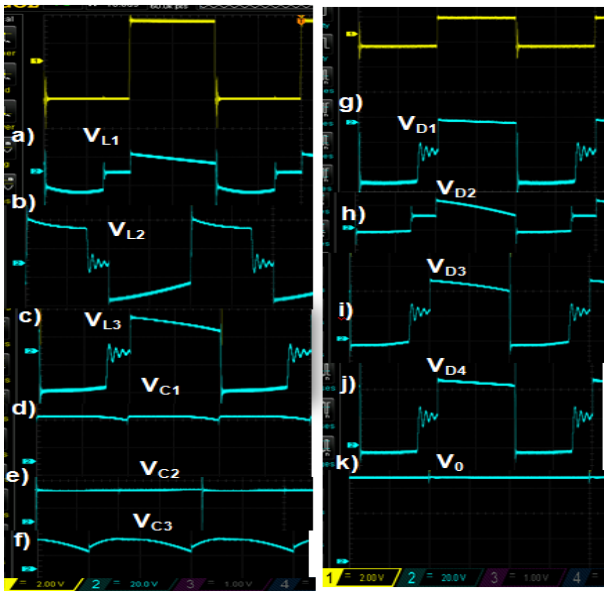

Fig 13. Experimental waveforms (Voltage) in DCM for; (a) inductor L_1; (b) inductor L_2; (c) inductor L_3; (d) Capacitor C_1;(e) Capacitor C_2; (f) Capacitor C_3;(g)Diode D_1; (h) Diode D_2; (i) Diode D_3; (j) Diode D_4; (k) Output.

The efficiency analysis of the converter is shown in Fig. 14, which demonstrates the reduction of efficiency with the enhancement of the duty cycle. This phenomenon can be explained by the fact that current value is augmented as *D* is enhanced, which yields the minute power loss in the circuit elements.

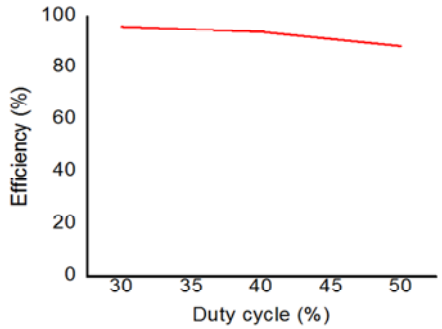

Fig 14. Efficiency vs. Duty Cycle obtained from the experimental setup.

Conclusion

In this paper, a new topology for the DC-DC boost converter was designed and analyzed. The voltage lift technique was employed using a single switch to boost the output voltage. The gain equation indicated that the proposed converter could achieve high voltage gain as compared to other conventional converters, which makes it suitable for high step-up applications such as in photovoltaic systems. The proposed converter can impart a unique role in augmenting the low voltage of solar panels to the required DC bus voltage and the voltage in DC nano-grids. Moreover, current stress on the switch was comparatively low than that of the conventional converters, which justifies the enhancement of the converter's efficiency. The performance of the proposed converter is validated by comparing simulation and experimental results. The efficiency of the proposed converter is high compared to the conventional converters in simulation, and the maximum efficiency of 92.3% was achieved experimentally at a 30% duty cycle. Further intensification in the voltage gain can be achieved by consolidating the interleaved topology into the existing topology.

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