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DSVPWM with Open-Leg Switching state for Two-Level Three-Phase Voltage Source Inverters

Abstract. *A new discontinuous space vector pulse width modulation (DSVPWM) method was proposed by utilizing the open-leg switching state in the space vector method. The proposed method was investigated by MATLAB simulation, and experimental methods. Results were compared with the space vector pulse width modulation (SVPWM) method and the 60° discontinuous space vector (60DSVPWM) method. Total harmonic distortion (THD) value of the proposed method was close to the THD value of SVPWM in the high modulation index. In addition, magnitude of the fundamental output current of the proposed method was higher than for the two existing methods.*

Streszczenie. *Zaproponowano nową metodę modulacji szerokości impulsów w płaszczyźnie wektorowej. Zaproponowana metoda była sprawdzona jako symulacja z wykorzystaniem Matlab oraz eksperymentalnie. Otrzymane wyniki były porównane z innymi dotychczas stosowanymi metodami jak na przykład SVP{WM .* ***Nowa metoda modulacji szerokości impulsów w dwupoziomowym, trójfazowym przekształtniku.***

Keywords: Discontinuous Space Vector Pulse Width Modulation, Open-leg Switching State, Delay Time, Dead Time.
Słowa kluczowe: modulacja szerokości impulsów DSVOWM, SVPWM, przekształtnik.

Introduction

Several years ago, many pulse width modulation (PWM) methods for two-level three-phase inverters were proposed such as space vector PWM (SVPWM), discontinuous PWM (DPWM), discontinuous space vector PWM (DSVPWM) and hybrid PWM [1, 2, 3, 4, 5]. All these methods were studied and developed to reduce the harmonic distortion of output current and switching losses in inverters. The two-level three-phase inverter as shown in Fig.1 can generate eight switching states comprising six active states {(100), (110), (010), (011), (001) and (101)} and two zero states {(000) and (111)}. The inverter leg states are bi-state: the first state is '1' and the second state is '0'. The state '1' means that only the upper switch in the leg is turned on, and the state '0' means that only the lower switch is turned on. Some studies demonstrated using a third state where both switches in the leg were turned off. This was called the open-leg switching state (OLSS) in [6] and the state 'X' in [7]. In [6], the inverter switches were operated under the six existing active states and six new partial-active states where each new state included the OLSS. Consequently, the inverter was operated in a 150° conduction mode providing low total harmonic distortion (THD) of output current and a blank period to avoid a short circuit in the inverter leg. However, one drawback of conduction modes is that it is difficult to control the output voltage. In [7], turning off both switches in the leg, the state 'X', was employed in the PWM method and defined as the unipolar pulse width modulation (UPWM) method.

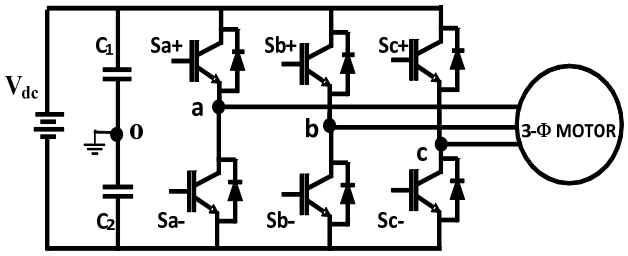


Fig.1. Two-level three-phase inverter

In UPWM, the delay time of switching pulse to protect the DC source shortage at the leg can be neglected and the dead time effect can be avoided without compensation. UPWM is based on a carrier-based method which lacks the independence of the switching state selection. On the other hand, the space vector method implemented on microcontrollers or digital signal processors (DSP) is easy to select and sequence the switching state, which affects switching losses in the inverter and output current quality. A new modulation based on the space vector method can be generated by changing the switching sequence or choosing one of two of zero switching states in one sampling period [2, 3, 4, 5].

Here, a new DSVPWM was proposed using the DSVPWM method with the OLSS under UPWM conditions. This was called DSVPWM with open-leg switching state (DSVPWMOLSS). Moreover, validation of DSVPWMOLSS was verified by simulation and experiment.

Unipolar pulse width modulation

The pulse width modulation with open-leg switching state method defined as the unipolar pulse width modulation (UPWM) method was presented and realized using the DPWM method with LOSS [7]. In [7], the OLSS is called the state 'X' which means that both switches in a leg are turned off. In addition, the output current direction of the inverter affects the polarity of the output voltage. If the output current flows out of the leg to loads, as shown in Fig. 2 a), the output voltage is $-V_{dc}/2$ and the state is defined as the state 'X_+'. By contrast, if the output current flows into the DC source, as shown in Fig. 2 b), the output voltage is $+V_{dc}/2$ and the state is defined as the state 'X_-'.

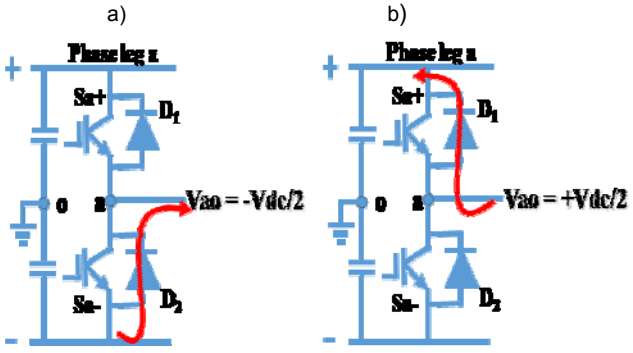


Fig.2. Output voltage at the a-leg; a) the state X_+ and b) the state X_-

The UPWM method is a carrier-based PWM implementation in which a modulating waveform is

compared with a carrier waveform to generate PWM pulses. The modulating function of the DPWM0 method was adopted as the UPWM modulating function (modulating waveform) and can be expressed in (1) [7].

$$(1)\quad V_{avg}=\begin{cases} m\sin(\omega t+\pi/3), & 0\le \omega t<\pi/3 \\ 1+m\sin(\omega t+2\pi/3), & \pi/3\le \omega t<2\pi/3 \\ -1, & 2\pi/3\le \omega t<\pi \\ m\sin(\omega t+\pi/3), & \pi\le \omega t<4\pi/3 \\ -1+m\sin(\omega t+2\pi/3), & 4\pi/3\le \omega t<5\pi/3 \\ 1, & 5\pi/3\le \omega t<2\pi \end{cases}$$

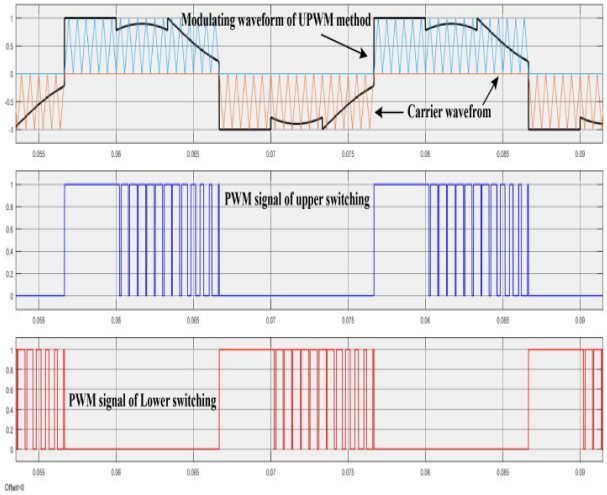


Fig.3. Carrier-based PWM of the UPWM method

UPWM gate signals of the upper and lower switches are generated by comparing the modulation waveform of the UPWM method with the carrier waveform as shown in Fig. 3.

The output voltage and the total harmonic distortion (THD) of the UPWM and DPWM0 methods are similar if the UPWM method is under the conditions:

1) The load inverter is a three-phase low-power AC motor,

2) The inverter-leg state must be clamped onto the DC bus voltage while the output current of the inverter crosses a zero value to avoid an unpredictable current direction.

In the SVPWM method, eight voltage vectors as six active vectors (V_1 through V_6) and two zero vectors (V_0 and V_7), are generated by eight switching states which comprise $V_1(100)$, $V_2(110)$, $V_3(010)$, $V_4(011)$, $V_5(001)$, $V_6(101)$, $V_0(000)$, and $V_7(111)$ [1]. In addition, the reference voltage vector, V_{ref}, in the voltage vector space is generated by two adjacent active vectors and two zero vectors. In the UPWM method, the switching pulses of three legs in a sampling period comprise two active states and a zero state but some leg states of two-thirds of switching states were replaced by the state 'X'. The switching states of the UPWM method were defined and explained in the voltage space vector plane as shown in Fig. 4.

One advantage of the UPWM technique is that it can avoid dead time effects without detecting the output current direction of each leg when the reference vector is moving inside the sector. However, the delay time of PWM signals or dead time is still necessary to protect the short circuit in the legs when the reference vector is transferring from one sector to the next sector.

DSVPWM with the open-leg switching state method

A new DSVPWM method called the DSVPWM with open-leg switching state (DSVPWMOLSS) is presented here based on the PWM with OLSS method or the UPWM method. The DSVPWMOLSS method was designed to control the inverter driving the three-phase induction motors where the load current lags the fundamental component of output voltage. To avoid an unpredictable current direction, the inverter legs must be clamped onto the DC bus voltage when the load current is crossing a zero level. The DPWM0 method employs only V_0 in odd sectors and only V_7 in even sectors. The DPWM0 modulating waveform is illustrated in Fig. 5 [8]. The DPWM0 method can also provide the leg-clamp state to avoid unpredictable current direction if the leg current lags the fundamental output voltage by 30° to 90° as shown in Fig. 5. Therefore, the DPWM0 method was chosen and developed with OLSS to establish DSVPWMOLSS.

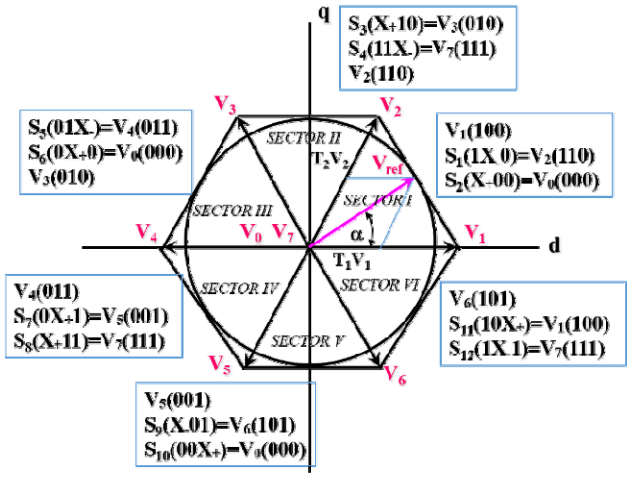


Fig.4. Voltage vectors of UPWM method

The UPWM vector sequence can be illustrated as V_Y, V_X, V_Z in every sampling period where V_Y is the active vector following the reference vector, V_X is the active vector preceding the reference vector and V_Z is the zero vector. The drawback of this sequence is the requirement of delay time of the PWM signals when the reference vector is transferring between one sector and the next. Therefore, the DSVPWMOLSS vector sequence is newly defined to eliminate the delay time of PWM signals but the DC source shortage at the legs is still protected by OLSS.

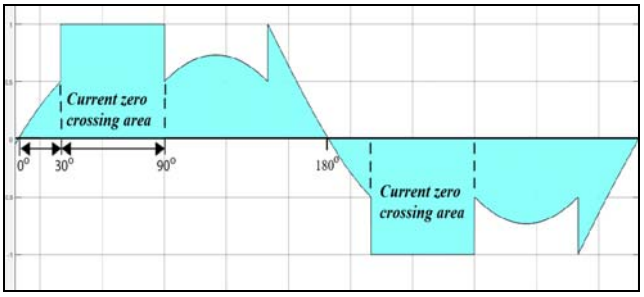


Fig.5. DPWM0 modulating waveform

The DSVPWMOLSS is realized by replacing the OLSS (the state 'X') with some switching state in the DPWM0 method. Moreover, the new vector sequence or new switching state sequence in one sampling period is defined as V_Y, V_X, V_Z, V_X, V_Y. The zero vector V_0 is used in the odd sectors and the zero vector V_7 is used in even sectors. The

leg state in a switching state or a vector is replaced with the state 'X' if there is transition of the leg state during the sampling period.

For example, the vector sequence in sector 1 of the DPWM0 method is rearranged as V_Y,V_X,V_Z,V_X,V_Y and can be expressed as V_2,V_1,V_0,V_1,V_2 sequence. In this study, this is called the 60° discontinuous space vector (60DSVPWM), and all sequences in the six sectors are illustrated in Table 1. Then, the leg states in V_0 and V_2 were replaced with the state 'X'. When the a-leg state is switched from 1 to 0 at V_0, the vector V_0 changes as $S_2(X_+00)$. In addition, when the b-leg state is switched from 0 to 1 at V_2, the vector V_2 changes as $S_1(1X0)$. On the other hand, the c-leg is no longer the transition of the leg state over a sampling period, thus, the vector V_1 remains the same. Therefore, the DSVPWMOLSS vector sequence in sector 1 is S_1,V_1,S_2,V_1,S_1, as shown by the pattern in Fig. 6. DSVPWMOLSS sequences in the six sectors are shown in Table 1. Consequently, the inverter legs are clamped onto the DC bus voltage for 60° in each half cycle of fundamental output voltage waveform. The clamping state starts at 30° and ends at 90° for the first half cycle and starts at 210° and ends at 270° for later half cycles.

The DSVPWMOLSS method provides output voltage similar to output voltage of the 60DSVPWM method if it is under UPWM conditions. Therefore, the power factor ($cos\varphi$) of the load of the inverter must be less than or equal to 0.866 (lagging).

Dwell time of each switching state or voltage vector can be formulated as [1, 4, 9]:

$$T_X = T_S m \sin(\frac{\pi}{3} - \alpha^o) \quad (2)$$

$$T_Y = T_S m \sin(\frac{\pi}{3} - \alpha^o) \quad (3)$$

$$T_Z = T_S - T_X - T_Y \quad (4)$$

Where T_X is the duration time of V_X, T_Y is the duration time of V_Y, T_Z is the duration time of the zero vector (V_0 and V_7), T_S is the sampling time, m is the modulation index, and α^o is the angle of the reference voltage vector in a sector.

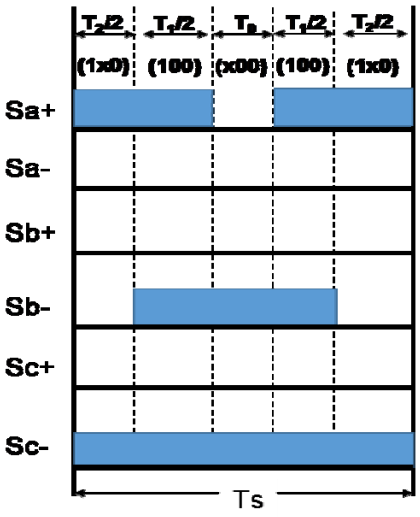


Fig.6. Switching pattern of the DSVPWMOLSS method in sector 1

Table 1. Vector sequences in six sectors

Sector	SVPWM	60DSVPWM	DSVPWMOLSS
1	$V_0,V_1,V_2,V_7,V_2,V_1,V_0$	V_2,V_1,V_0,V_1,V_2	S_1,V_1,S_2,V_1,S_1
2	$V_0,V_3,V_2,V_7,V_2,V_3,V_0$	V_3,V_2,V_7,V_2,V_3	S_3,V_2,S_4,V_2,S_3
3	$V_0,V_3,V_4,V_7,V_4,V_3,V_0$	V_4,V_3,V_0,V_3,V_4	S_5,V_3,S_6,V_3,S_5
4	$V_0,V_5,V_4,V_7,V_4,V_5,V_0$	V_5,V_4,V_7,V_4,V_5	S_7,V_4,S_8,V_4,S_7
5	$V_0,V_5,V_6,V_7,V_6,V_5,V_0$	V_6,V_5,V_0,V_5,V_6	S_9,V_5,S_{10},V_5,S_9
6	$V_0,V_1,V_6,V_7,V_6,V_1,V_0$	V_1,V_6,V_7,V_6,V_1	$S_{11},V_6,S_{12},V_6,S_{11}$

Simulation results

To verify the feasibility of the DSVPWMOLSS method, the inverter and PWM controller were simulated in the MATLAB/SIMULINK model. In Fig. 7, the inverter and PWM controller model proposed by [10] were adapted to operate in the SVPWM, 60DSVPWM and DSVPWMOLSS methods. These methods were simulated and total harmonic distortion (THD) values of their output currents were compared. Simulation parameters are given in Table 2.

In this study, a three-phase inverter model controlled with a PWM control unit model supplied 50 Hz three-phase voltage to a wye-connected RL load model, with resistance and inductance values as 0.524 Ω and 0.00327 H, respectively. Hence, the load power factor (PF) was 0.454 (lagging).

Simulation results of the DSVPWMOLSS model are shown in Figs. 8-10. Fig. 8 shows the PWM signals of the upper switch of the three legs. The three PWM signals are 120° out of phase from each other. Each switch is clamped to the DC bus level for 60° and turned off for 180° The PWM signals of the upper and lower switches are 180° of phase from each other as shown in Fig. 9. Moreover, Fig. 9 shows that if one switch is chopping the DC voltage, the other remains off. The OLSS is established among the switching of both switches in the leg. Therefore, short circuit protection in the leg can be eliminated.

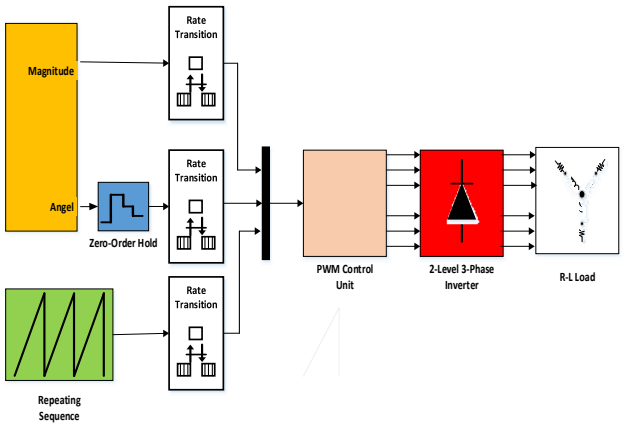


Fig.7. MATLAB/SIMULINK model of inverter and PWM controller

Table 2. Simulation parameters

Parameters	Quantity	Unit
Sampling time	0.002	Second
Output frequency	50	Hz
Resistance	0.524	Ohm
Inductance	0.00327	H

Fig. 10 shows a line voltage, a phase voltage, a load current and PWM signals of $Sa+$ of the DSVPWMOLSS method. These results verify the validation of the DSVPWMOLSS method. The line voltage and phase voltage are 30° out of phase from each other. Moreover, the load current crosses the zero value in the clamping interval of PWM signals.

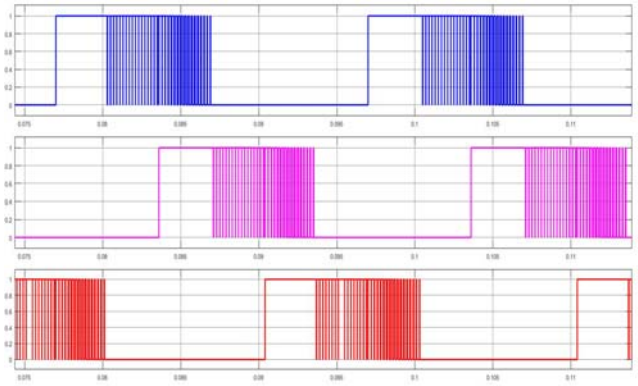


Fig.8. PWM signal of DSVPWMOLSS

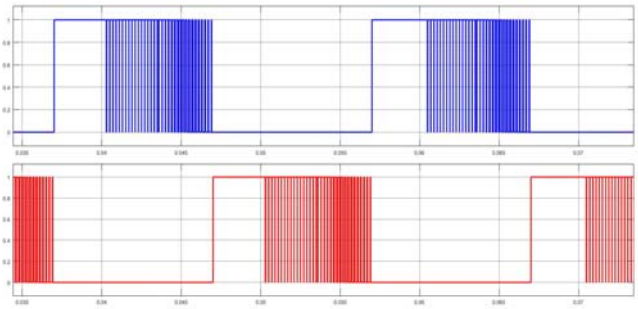


Fig.9. Upper and lower PWM signal of a leg

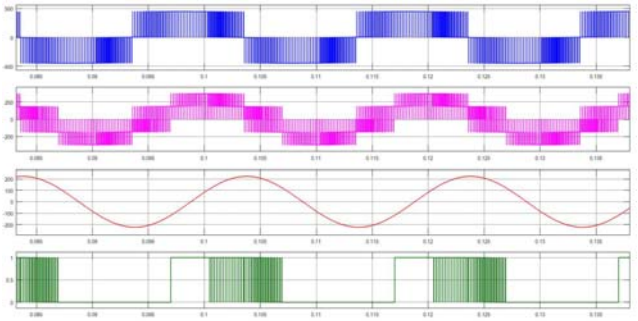


Fig.10. Line voltage (V_{AB}), phase voltage (V_{AN}), load current (I_A) and PWM signal of upper switch ($Sa+$)

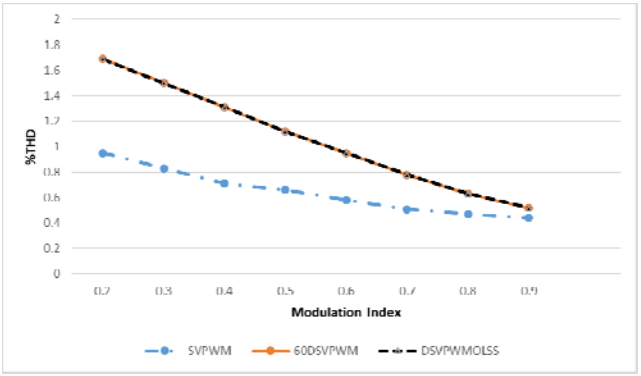


Fig.11. Simulation results (%THD vs. Modulation index) of SVPWM, 60DSVPWM and DSVPWMOLSS at PF = 0.45 (lagging)

For a comparative simulation study, THD values of the output current of the three methods are shown as curved in Fig. 11. The THD curve of the SVPWM method is lower than the other two methods. In addition, THD curve differences between the SVPWM method and the others increased at low modulation index values. When the modulation index value reached 0.9, THD curves of the 60DSVPWM and DSVPWMOLSS methods were close to the SVPWM method.

Experimental results

To verify the effectiveness of the proposed method, an experimental setup was implemented as shown in Fig. 12, with parameters of the two-level three-phase inverter and load shown in Table 3. The inverter was composed of six molded IGBTs and its input DC bus voltage was set at 310V. In addition, the PWM control unit was an Arduino DUE board on which the SVPWM, 60DSVPWM and DSVPWMOLSS algorithms were implemented. All methods in this experiment operated at the same sampling time and number of samples per output frequency. Rising edges of PWM signals of the SVPWM and 60DSVPWM methods, except for the DSVPWMOLSS method, were delayed by a dead time circuit with delay time set at 10 μs to protect short circuits in the legs.

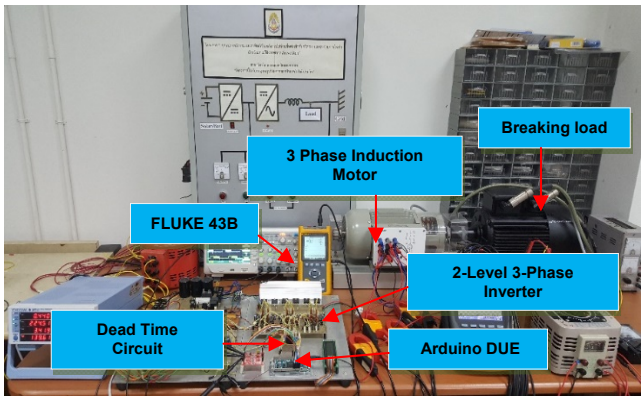


Fig.12. Experimental set-up

Table 3. Parameters of the inverter

Parameters	Quantity	Unit
DC-link voltage	310	volt
3Ø Induction motor	1.0	KW
Sampling time	222	μs
Number of samples per output frequency	15	times
Delay time	10	μs
Molded IGBT : 1MBH20D-060	6	set

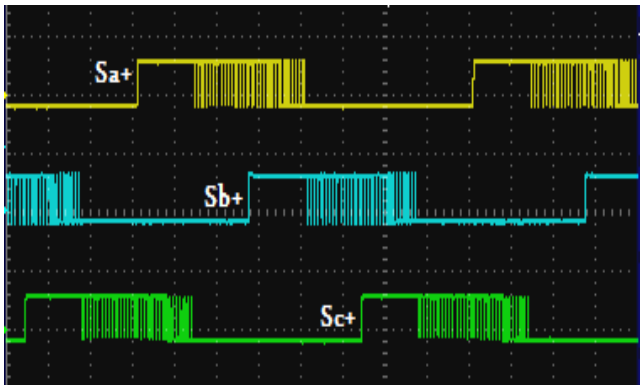
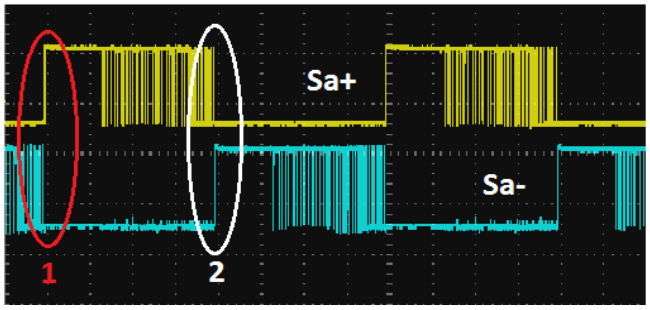


Fig.13. IGBT gate signals of three upper switches for the DSVPWMOLSS method (Horizontal axis: 2.5ms/div; Vertical axis: 20V/div).

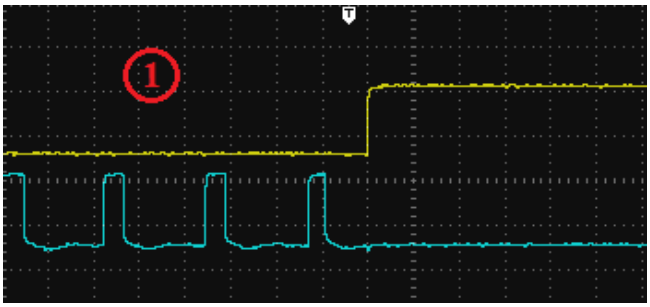
Fig. 13 shows the DSVPWMOLSS gate signals of the three upper IGBTs ($Sa+$, $Sb+$, $Sc+$) which were set at 120° out of phase from each other. Each IGBT was turned on and clamped through 60°. Therefore, the proposed method followed the conditions of UPWM: the current passes the zero value in this duration. In addition, IGBT gate signals, as shown in Fig. 13, corresponded to the PWM signals in the simulation results section as shown in Fig. 8.

PWM signals of the upper and lower switches in the a-leg ($Sa+$ and $Sa-$) and the state 'X' are shown in Fig. 14 a). The lower IGBT was turned off while the upper IGBT was chopping and vice versa. In addition, the state 'X' occurred among switching of the switch state. Fig. 14 b) shows magnified PWM signals of both switches in the a-leg with the state 'X' which occurs while the on-state of IGBT is transferring from the lower IGBT ($Sa-$) to upper IGBT ($Sa+$), or vice versa. The on-state of IGBT transferring from $Sa+$ to $Sa-$ is shown magnified in Fig. 14 c). Thus, the delay time or dead time to protect the short circuit in the leg can be eliminated. Moreover, the gate signals of the IGBT in Fig. 14 a) were similar to PWM signals in the simulation section as shown in Fig. 9.

a)



b)



c)

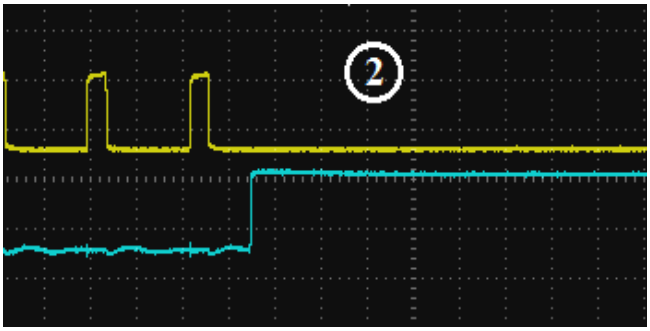


Fig.14. IGBT gate signals of upper and lower switches of the DSVPWMOLSS method (Vertical axis: 10V/div; Horizontal axis: a) 2.5ms/div, b) and c) 100μs/div).

In this study, the inverter operated at the modulation index (m) = 0.9 and at output frequency = 50 Hz. The inverter drove a 1KW three-phase induction motor which was controlled by an open loop control system. In addition, the motor load was set up as a breaking load by feeding the DC voltage into the stator of the 3KW induction machine. Consequently, the power factor ($cos\varphi$) of the induction motor was 0.45 (lagging).

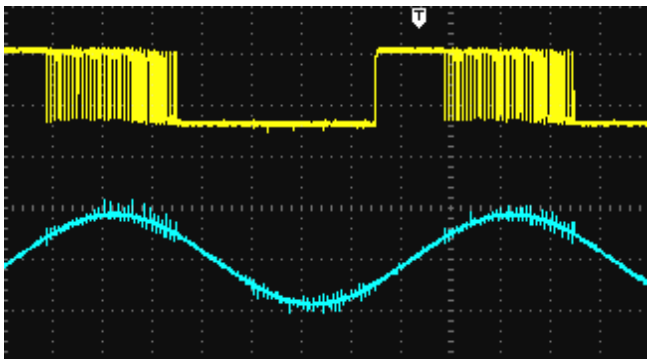


Fig.15. IGBT gate signals of lower switch ($Sa-$) and load current (Horizontal axis: 2.5ms/div; Vertical axis: 10V/div and 4A/div)

Fig.15 shows the IGBT signals of the DSVPWMOLSS method while the load current was crossing the zero value during the clamping duration of IGBT; thus, the DSVPWMOLSS method can avoid uncertainty of current direction. Results, shown in Fig. 15, were similar to simulation results shown in Fig. 10.

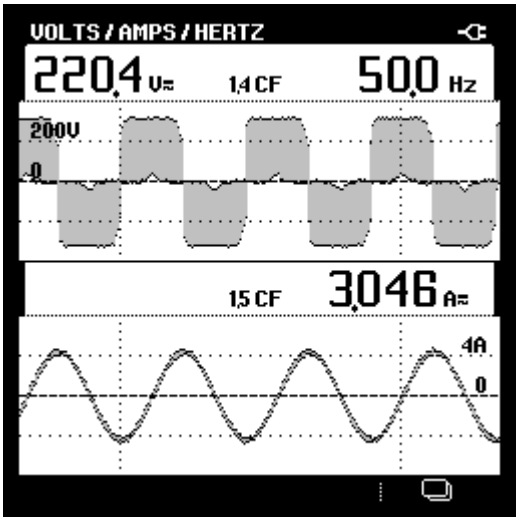


Fig.16. Line voltage and load current of the DSVPWMOLSS method

The output voltage waveform, load current waveform and current THD value of the DSVPWMOLSS method were measured by a power quality analyzer (FLUKE 43B), as shown in Figs. 16-18. Figs. 16 and 17 show the output voltage waveform of the line voltage and phase voltage, respectively and the load current waveform at m = 0.9 with output frequency = 50 Hz. All waveforms were symmetric and similar to simulation results as shown in Fig. 10. Phase difference between the phase voltage and load current was 63.26° (lagging) with $cos\varphi$ as 0.45 (lagging). The harmonic spectrum and THD value of the load current are shown in Fig. 18. A THD value of 0.5 means that the measured current is nearly sinusoidal. Results verify that the inverter

with the DSVPWMOLSS method can supply a symmetric waveform and low harmonic current to the motor without dead time protection.

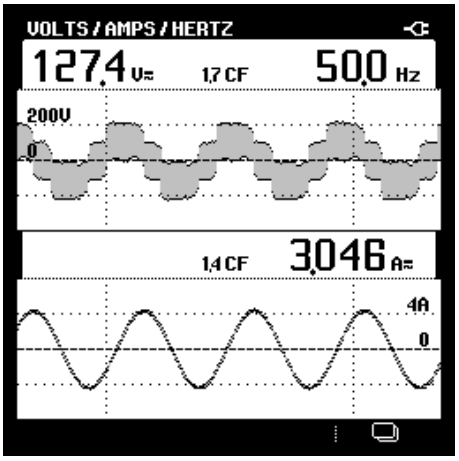


Fig.17. Phase voltage and load current of the DSVPWMOLSS method

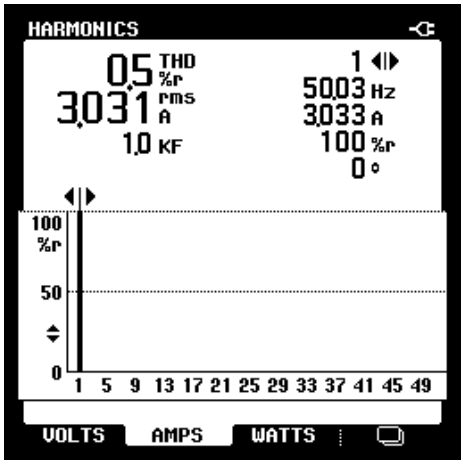


Fig.18. Magnitude spectrum of load current of the DSVPWMOLSS method

In this study, the proposed method was experimented and compared with existing methods (SVPWM and 60DSVPWM). The legs of the inverter controlled using the existing methods protected a short circuit using dead time circuits. Moreover, a delay time of the gate signal was set at 10 μs. A significant effect of the delay time reduced the output magnitude of fundamental components [11, 12, 13]. Fundamental magnitudes of load current of the three methods were normalized by the maximum magnitude value of the DSVPWMOLSS method. The normalized fundamental magnitudes of line current of the three methods were plotted in Fig. 19. The fundamental component magnitude over the modulation index of DSVPWMOLSS method is the higher than the existing two methods due to the elimination of the delay time of switching signals.

THD values over the modulation index of load current of the three methods plotted in Fig. 20 show a steady decrease over the modulation index. Although the output voltage waveforms of 60DSVPWM and DSVPWMOLSS methods were the same because the DSVPWMOLSS method was performed under UPWM conditions, the effect of delay time of the 60DSVPWM method resulted in difference of both THD curves at low modulation index. On the other hand, at high modulation index, the THD curve of the 60DSVPWM method was almost similar to the DSVPWMOLSS curve. From the SVPWM curve, the THD curve of SVPWM was lower than the other two methods but the THD curves of the 60DSVPWM and DSVPWMOLSS methods were closer to the SVPWM method as the modulation index increased to 0.9.

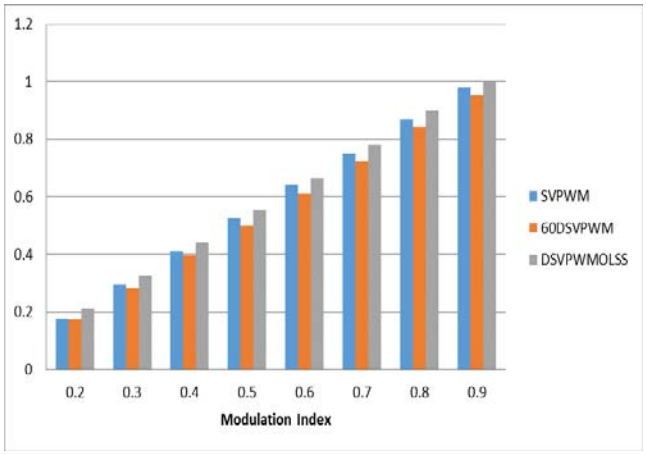


Fig.19. Normalized fundamental magnitude of load current over the modulation Index for SVPWM, 60DSVPWM and DSVPWMOLSS methods

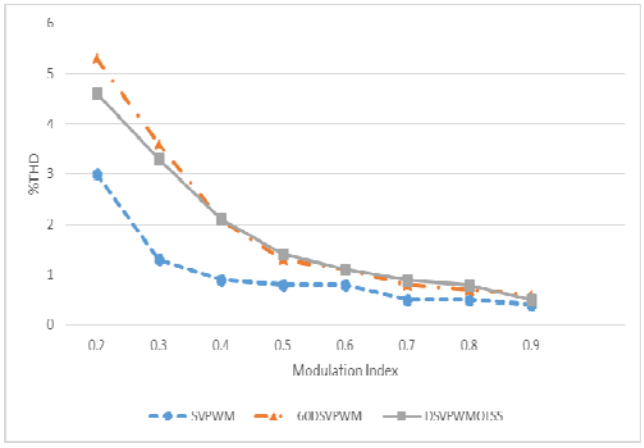


Fig.20. THD over the modulation index of SVPWM, 60DSVPWM and DSVPWMOLSS methods at $cos\varphi$ = 0.45 (lagging)

Conclusions

Here, a novel discontinuous SVPWM technique employing the open-leg switching state was proposed and defined as discontinuous SVPWM with the open-leg switching state (DSVPWMOLSS). The proposed technique was studied and compared with SVPWM and 60DSVPWM methods. In addition, harmonic distortion and magnitude of the fundamental components of current were investigated. Results showed that the proposed method can drive an induction motor without dead time protection. For the proposed method, the THD curve at low modulation index was higher than the SVPWM THD method but lower than the 60DSVPWM method due to the delay time effect. On the other hand, the all THD curves were close to the same value at high modulation index. In addition, the fundamental magnitude of load current was higher than the SVPWM and 60DSVPWM methods because the dead time is was eliminated. Therefore, the proposed method can provide the a higher torque in induction motors than the two existing methods. For application, this new proposed method is suitable as an application to drive small induction motors

with open-loop control systems at high modulation indices to generate low THD current and high magnitude of the fundamental current without the dead time protection.

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