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A Simple and Accurate CMOS Sample-and-Hold Circuit Using Dual Output-OTA

Abstract*. A new CMOS sample-and-hold (S/H) circuit using dual output-operational transconductance amplifier (DO-OTA), one resistor and one capacitor is presented. It is unlike conventional S/H circuit. The proposed circuit has not use a switched-capacitor, switched-current or MOS switches for on-off switch but it uses an on-off DO-OTA by bias current that replace them. The proposed S/H circuit is high speed on-off status of switch and without buffer circuit can be obtained. However, it is a very simple circuit, high accuracy, low-power consumption and suitable for signal processing applications by using on the first part of analog to digital converter. The simulation results are used to confirm the workability of the proposed circuit.*

Streszczenie. *W pracy zaprezentowano nową koncepcję układu sample and Hold bazującą na transkonduktancyjnym wzmacniaczu DO-OYA. Proponowany układ nie wykorzystuje przełączanego kondensatora I zamast tego wykorzystuje przełączany prąd układu DO-OTA.* ***Prosty i dokładny układ Sample-and-Hold wykorzystujący transkondukltancyjny wzmacniacz DO-OTA***

Keywords: Sample-and-hold, operational transconductance amplifier, dual-output.
Słowa kluczowe: układ Sample-and_Hold, wzmacniacz transkonduktancyjny .

Introduction

Generally, the signals can be divided in two categories which are analog and digital signals. Analog signal is nature signals which is seemed in continuous signal. It is smoothly changed such as sinusoidal and cosine signals but the digital signal is quickly changed. It has two status that is high and low levels. However, analog and digital signals can be converted. Analog signal can be converted to digital signal that is analog-to-digital converters (ADC) and the digital signal can be converted to analog signal that is digital-to-analog converter (DAC). ADC and DAC are an important part of the signal processing system in telecommunications, instrumentation, control, measurement and communications. In deep, ADC has been used for data processing purposes in digital signal processing which is generated binary bit (low and high levels or bit "0" and bit "1"). For DAC, it converts digital signal to analog signal by reconstruction analog signal as same as the first signal input. Because the analog signals and digital signals are counterpart, ADC and DAC are couple converters which are in the mixed-signal processing systems.

Besides the first stage of the ADC circuit, it is sample-and-hold circuit (S/H) [1]-[3]. It has been used to eliminate variations in input signal that can corrupt the conversion process that is important building block for modern communication systems and other data converters [4] as the demand on high-speed, high-resolution data acquisition systems increases rapidly and low power [3]-[7]. Basic simple S/H circuit consists of a switch and a capacitor [3]. Later, S/H circuits used close-loop and open-loop structures by switched-capacitor (SC) and switched-current (SI) circuits have been proposed [8]-[17]. SC circuits are amenable for implementation in digital CMOS technologies which rarely have high-density linear capacitors and SI circuits are very attractive due to the fact that they do not need linear capacitors [14]. Compared between SC and SI circuits, SI circuits are seriously limited by the problem of charge injection due to their harmonic distortion which is much worse than SC circuits but SC circuits have the main drawback of used non-overlapping or inverting signals to control the switches.

However, many S/H circuits can be realized to be based on op-amp and capacitor that have been designed by close-loop and open-loop structures. So, they have the obstacle of the limited bandwidth of the amplifiers in the loop, the close-loop has not been used for high-speed applications but the open-loop can be accomplished high-speed performance at the cost of lower accuracy than closed-loop ones. Moreover, the transconductance and output impedance of the op-amp cause the limited of time constant in sampling mode [18]. Then, OTA as active device is also used to increase the accuracy and resolved the main drawback of op-amp [19]-[24]. Another interesting technique is analogue switch that has been proposed in [25] which used the second current conveyor (CCII) as active device. It absent from non-overlapping clock signal requirements for SC and SI circuits to control their switches because they have been replaced by bias current source. For integrated circuit (IC) implementation, the number of CMOS for OTA and CCII will be compared. Normally, CMOS for OTA is less than CCII. Then, this paper proposes a simple and accurate CMOS S/H circuit for the first part of A/D converter which uses OTA as active device, one resistor and one capacitor by non-overlapping clock signal requirements and without buffer circuit but this paper uses external bias current for OTA that replaces for many switches in SC or SI by applying as the same technique as in [25]. The proposed S/H circuit is very simple circuit, high accuracy, low-power and suitable for the first part of analog to digital converter in signal processing applications.

Dual-Output OTA

A simple circuit symbol of OTA consists of two voltage input ports and one output port that is current output [26]. However, OTA can be modified by two outputs that are dual-output OTA (DO-OTA). The circuit symbol and schematic DO-OTA are shown in Fig. 1 and Fig. 2, respectively. The characteristic can be expressed by:

$$I_{o1} = I_{o2} = g_m \left(V_1 - V_2\right) \tag{1}$$

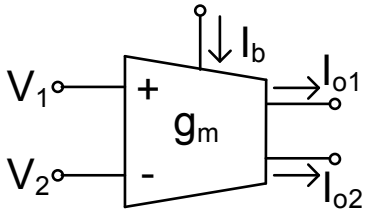

Fig.1. The circuit symbol of dual-output OTA

The ideal terminal characteristic of OTA is high impedance at terminal I_o, V_1 and V_2 (i.e. there is no input current). It has the advantage cascade ability for the

voltage-mode circuits. The transconductance g_m can be electronically tuned and found through the biasing current I_b [26] that is shown as:

$$g_m = \sqrt{\mu_n C_{ox}(W/L) I_b} \tag{2}$$

where: *W* and *L* are the effective channels width and length of MOS, respectively, μ_n is mobility of carrier in the channel, C_{ox} is the gate-oxide capacitance per unit area and I_b is bias current of OTA.

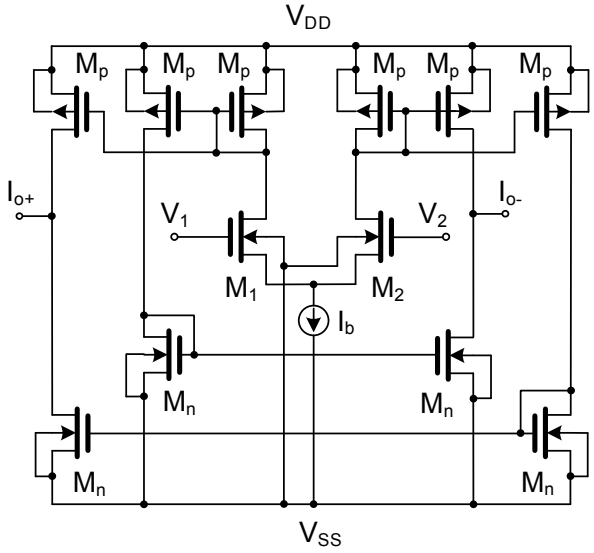

Fig.2. The schematic of dual-output OTA

Proposed Circuit

The proposed S/H circuit is shown in Fig. 3. It consists of DO-OTA, resistor R_{in} and capacitor C_{out}. This paper will design and apply based on an analogue switch operating [25] that used CCII as active device. The operating of the proposed circuit in Fig. 3 can explain, when the input signal V_{in} is applied and the biasing current I_b is controlled by binary bit stream of digital that is bit "1" and bit "0", in the other words, the biasing current I_b is used for sampling frequency in proposed S/H circuit. And then, when the biasing current I_b is bit "1" that DO-OTA is supplied by I_b, therefore this circuit is compared as switch that will be closed. Inversely, when the biasing current I_b is bit "0", DO-OTA is not supplied by I_b, therefore this circuit is compared as switch that will be opened.

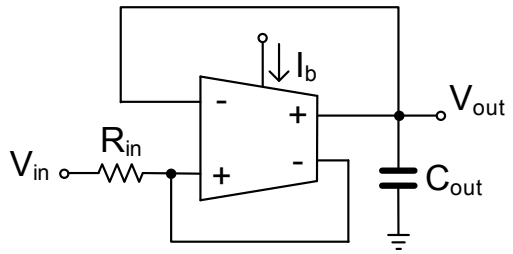

Fig.3. Proposed S/H circuit

During the sampling frequency while the biasing current I_b is bit "1" (switch close), the hold capacitor is stored and charged up that is "sampling mode". While the biasing current, I_b is bit "0" (switch open), the hold capacitor is discharge that is "holding mode". Thus, the input signal V_{in} is unnecessary for S/H circuit that means the last value is held until the input signal V_{in} is sampled again. The relatedness about the input signal V_{in} and the output signal V_{out} in Fig. 3 can be expressed as:

$$V_{out} = V_{in}\left(1 - e^{-t/R_{in}C_{out}}\right) \tag{3}$$

From Eq. (3), t is sampling period that can be found by $1/f_s$, where f_s is sampling frequency by I_b for DO-OTA. Noticed in Eq. (3), the resistor R_{in} and capacitor C_{out} is multiplied that is the time constant τ. By substituting f_s and τ in (3), the voltage V_{out} can be rewritten as:

$$V_{out} = V_{in}\left(1 - e^{-1/\tau f_s}\right) \tag{4}$$

Then, the output V_{out} of the proposed S/H circuit in (4) is depended on the time constant τ (resistor R_{in} and capacitor C_{out}) and sampling frequency f_s (bias current I_b for DO-OTA).

Non-Ideal Effect

The effect of non-idealities of OTA is discussed in this section. Notwithstanding in the previously section, MOS transistors are perfectly matched and OTA is assumed by no tracking errors. But practically, the non-ideality effects arise out of tracking errors and MOS transistors are not perfectly matched. The non-idealities of OTA is analyzed. Then, in Eq. (4) can be added non-ideality parameters and written as:

$$V_{out} = \beta_k V_{in}\left(1 - e^{-1/\tau_i f_s}\right) \tag{5}$$

Where: β_k = 1-ε_{kv} and ε_{kv}($|\varepsilon_{kv}|$<<1) denote the voltage tracking error from V_{in} terminal to V_{out} terminal, $\tau_i = (R_{in})(C_{out}//C_o//R_o)$, it is time constant of non-ideality for proposed circuit. In addition from Eq. (4), C_o and R_o have been appeared at the output of OTA and they parallel with C_{out}. Because of the condition of high impedance at the output terminal of OTA terminal, they can be made negligible by satisfying C_o <<1 and R_o >>1.

Simulation Results

The proposed S/H circuit is verified by the simulation from PSPICE simulators. The 0.18 μm TSMC CMOS parameters [27] will be designed for all MOS transistors of DO-OTA in Fig. 2 which the aspect ratio of all MOS transistors is shown in Table 1. The power supply is ±0.9 V. The interrelated parameters for using in this paper and summarized performance of DO-OTA are shown in Table 2.

Table 1. MOS Transistor Aspect Ratios Used for Fig. 2

MOS Transistor	W/L(μm/μm)
M_n	25/0.8
M_p	8/0.8
M_1, M_2	10/0.8

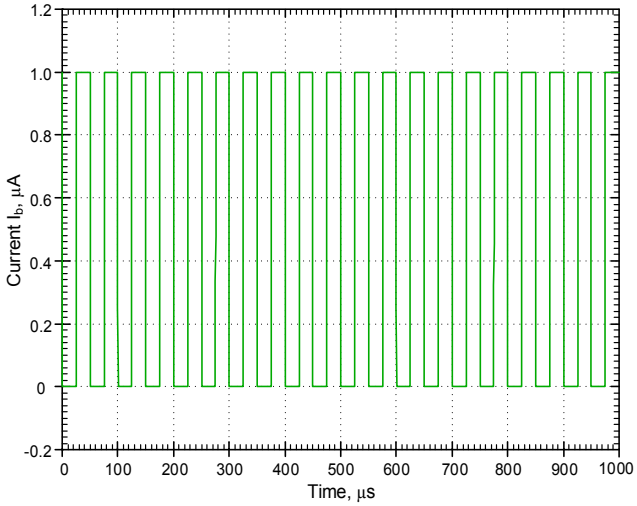

Fig.4. The bias current I_b for the sampling frequency f_s 20 kHz

Table 2. Interrelated Parameters and Summarized Performances of DO-OTA in Fig. 3

Parameters	Values
Technology	0.18 µm
Supply voltage (V)	±0.9 V
Bias current (I_b)	1 µA (for Fig. 5 and Fig. 6) 2 µA (for Fig. 8 and Fig. 9)
Sampling frequency (f_s)	20 kHz (for Fig. 5 and Fig. 6) 200 kHz (for Fig. 8)
Transconductance (g_m) I_b = 1 µA I_b = 2 µA	 37.08 µS 74.16 µS
Time-constant (τ) R_{in} = 500 Ω, C_{out} = 3 pF R_{in} = 1 kΩ, C_{out} = 10 pF	 1.5 ns 10 ns
$R_o//C_o$	260 kΩ//9.44 fF
Power consumption (I_b = 2 µA)	14 µW

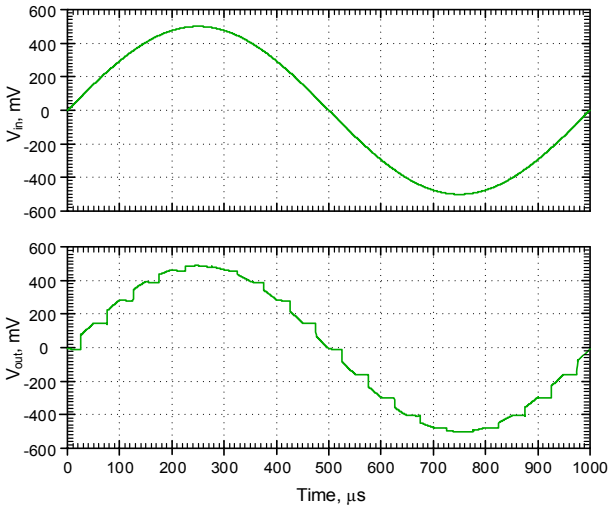

Fig.5. Simulated S/H output signal with sinusoidal input by used sampling frequency in Fig. 4

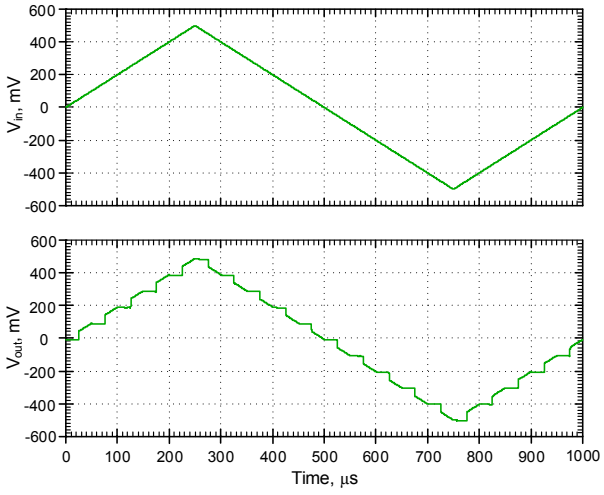

Fig.6. Simulated S/H output signal with triangular input by used sampling frequency in Fig. 4

The amplitude of the bias current I_b bit streams for DO-OTA was 1 µA which the sampling frequency f_s 20 kHz is used for controlling on and off DO-OTA operating. It is shown in Fig. 4 and will be used for the firstly test of proposed circuit that have 1.5 ns for the time-constant τ by R_{in} = 500 Ω and C_{out} = 3 pF. When the sinusoidal and triangular input waveform V_{in} are applied with amplitude and frequency 0.5 V_{p-p} and 1 kHz, respectively. The S/H sinusoidal output waveform is shown in Fig. 5 that sampling and holding mode resemble S/H output waveform in Fig. 6 but it was slightly different by input waveform especially.

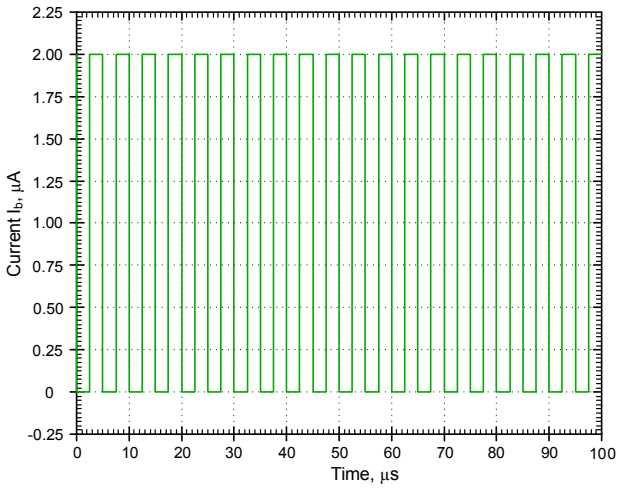

Fig.7. The bias current I_b for the sampling frequency f_s 200 kHz

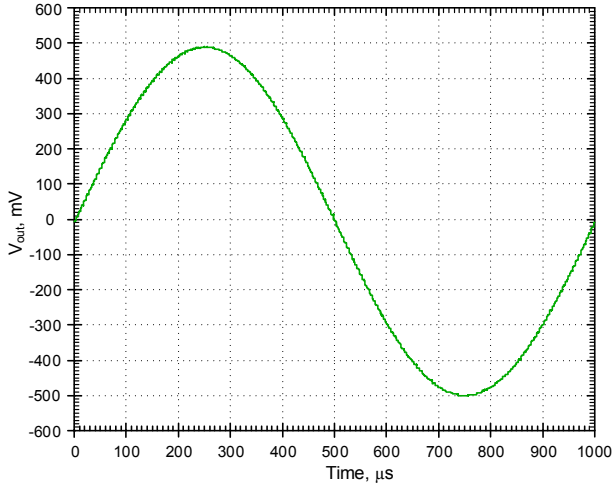

Fig.8. Simulated S/H output signal with sinusoidal input by used sampling frequency in Fig. 7

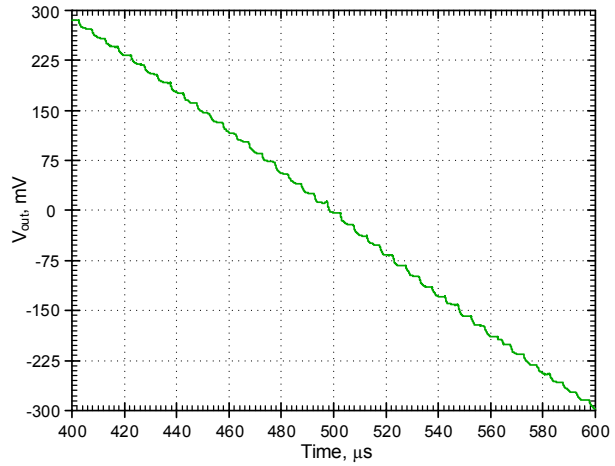

Fig.9. Simulated S/H sinusoidal output signal with zoom in from Fig. 8

Fig. 7 shows the secondly test of proposed circuit which bias current I_b bit streams have been increased to 2 µA. The input V_{in} sinusoidal is used as same as amplitude in

Fig. 5 for 0.5 V_{p-p} and frequency 1 kHz. The sampling frequency f_s with 10 times of Fig. 4 was used by increasing to 200 kHz. The time-constant τ is 10 ns about 7 times more than the first test by R_{in} = 1 kΩ and C_{out} = 10 pF. The S/H sinusoidal output waveform is shown in Fig. 8. Obviously, time-constant τ and sampling frequency f_s are increased by Fig. 9 that shows sinusoidal output waveform with zoom in from Fig. 8 in frequency range 0.25 kHz to 1.67 kHz (400 μs – 600 μs) and amplitude range -0.3 V to 0.3 V. Then, the workability of the proposed S/H circuit is confirmed by Fig. 8 and Fig. 9 which can be varied the important parameters of sampling frequency f_s and time-constant τ.

Conclusions

A simple and accurate CMOS sample-and-hold circuit using DO-OTA as active device, one resistor and one capacitor has been presented. The proposed circuit is unnecessary to use many switches for controlling clock signal such a technique as switched-capacitor, switched-current circuits and MOS switches in order to S/H signal output that has been proposed previously. Then, it has non-overlapping clock signal requirements by replacing the external bias current for OTA which the frequency sampling can be adjusted by it. The proposed circuit without buffer circuit can be obtained. It is a very simple circuit, high accuracy, low-power consumption and suitable for signal processing applications by using on the first part of analog to digital converter. The simulation results are used to confirm the workability of the proposed circuit.

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