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High Efficiency High Voltage Gain Boost Converter using Zero Crossing Switching Multi-stage Voltage-Lift Cells

***Abstract**. A non-isolated high efficiency, high voltage step-up gain boost converter is proposed in this paper. A series of multi-stage voltage-lift cells with simple diode-capacitor-inductor configuration is used to provide very high voltage gain for the conventional boost converter. A passive snubber is connected in parallel with a switch in the boost circuit to provide zero-current turn-on and zero-voltage turn-off and thus achieve low switching losses. Analysis, design and implementation of the proposed circuit are explained and examined by both simulation and experimental prototype. The test results verified the feasibility of the proposed converter with switching frequency of 50 kHz and rated power of 400 W. The proposed converter achieved 96.0% of maximum efficiency and very high voltage gain of 12 for a series of 3 stage voltage-lift cells.*

Streszczenie.** Opisano przekształtnik typu boost o dużej efektywności i dużym napięciu. Szereg celek składających się z diody-kondensatora I indukcyjności został zastosowany do siągnięcia dużego wzmocnienia i małych strat przełączania. Układ został poddany symulacji ale i zbadany eksperymentalnie. Częstotliwość przełączania była 50 kHz a moc 400 W. **Przekształtnik typu boost o wysokiej efektywności i dużym napięciu wykorzystujący przełaćzanie w przejściu przez zero wielu celek napieciowych

Keywords: Charge pumps, Boost converter, Switching converters, Zero current switching, Zero voltage switching
Słowa kluczowe: przekształtnik typu boost, przełączenie w przejściu przez zero, pompowanie ładunku..

Introduction

Transformerless DC/DC boost converters are required in many modern industrial applications such as renewable energy conversion systems, uninterruptible power supplies, motor drives and etc. due to their high efficiency, smaller size and light weight compared to ones with transformers [1], [2]. In several cases, large voltage step-up gain is required for the converters.

A very high step-up voltage gain greater than 4 times cannot be achieved with the traditional boost converter due to limitation of its operating duty cycle. [3-5]. In order to achieve a very high step-up voltage gain with acceptable operating duty cycle, the additional circuits have been added into the conventional boost converter such as ones proposed in [6], [7]. However, these additional circuits can cause the circuit and control complexity, as well as, more voltage stress on the switches. Alternatively, the quadratic boost converters could be more attractive due to their capability of high voltage gain without extreme duty-cycle [8]-[10]; however, the voltage stress on the switches remain relatively high. To eliminate the problem, the boost converters with coupled inductors have been proposed [11]-[13], by increasing the turns ratio of the coupled inductors, a high voltage conversion gain can be obtained. However, the converters with coupled inductors have a major drawback about large leakage inductor energy and hence degrades the converters' efficiency, and also difficulty in winding for inductors.

On the other hand, using capacitive charge pump circuits would be more preferable. These circuits contain capacitors that can store energy within them and create a voltage higher than the supply voltage [14]-[16]. Moreover, most capacitors operate with lower losses at high switching frequency compared to inductors. To combine benefits from both inductors and capacitors, both of them could be used to form the circuits such as ones proposed in [17]-[19]. In addition, both capacitors and inductors can be fabricated as just a single integrated cell and therefore ease for the implementation.

This paper proposed a transformerless high efficiency high voltage gain dc-dc converter with charge pump capacitor and voltage-lift inductor combined active lift-cell converter structure called a voltage-lift cell proposed by [20]. The details of operation, circuit configuration, analysis, design and implementation are presented and verified with both simulation and experimental prototype.

Converter configuration

Figure. 1 shows the circuit of the proposed single voltage-lift cell. This cell is a combination of a charge pump capacitor and a voltage-lift inductor.

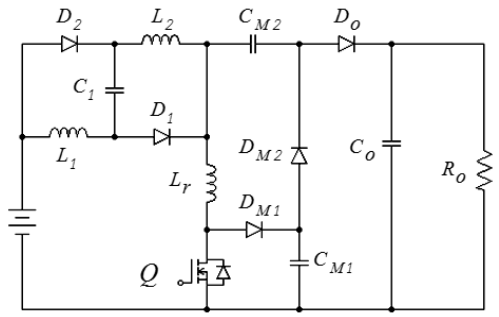

Figure 1. Converter with one unit voltage-lift cell at input

As Figure 1 suggests, the circuit consists of an active switch (Q), four diodes (D_1, D_2, D_{M1}, and D_o), four capacitors (C_1, C_{M1}, C_{M2}, and C_o), two inductors for energy storage ($L_1$and L_2), a small inductor (L_r) for zero voltage switching (ZVS), and a load, i.e., resistive load (R_o) for this case (for simplicity).

While small value of inductor L_r is typically desired, the voltage gain of a one unit voltage-lift cell is approximately equal to

$$\frac{V_o}{V_g} = \frac{4}{1-D} \tag{1}$$

In order to achieve very high voltage gain converter, a series connection of N stage voltage-lift cells could be inserted at the input side of the conventional boost converter as shown in Figure 2.

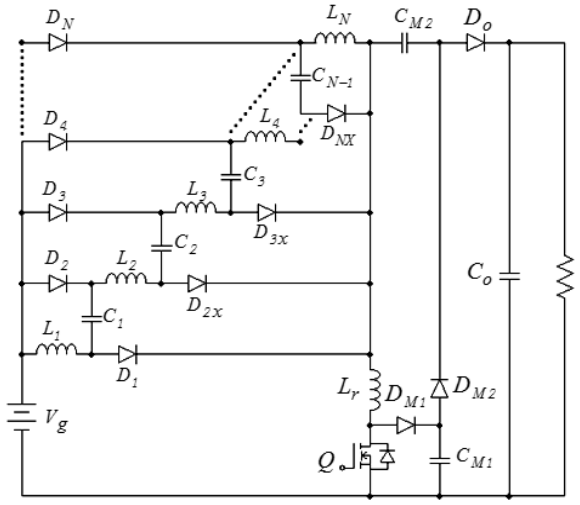

Figure 2. Converter with N stage of voltage-lift cells

To simplify the analysis, the following conditions are assumed;
1) All the devices are ideal
2) All capacitors are sufficiently large, and the voltage stress across the capacitors can be treated as constant.

Operating principle

To analyze operation principle of the proposed converter, some specification and assumption are given as follows:

(i) The input voltage is defined to be V_g .
(ii) The input current is defined to be I_i .
(iii) The values of L_1, L_2, …, L_{N-1}, L_N are the same.
(iv) The voltages across L_1, L_2, …, L_{N-1}, L_N are denoted by V_{L1}, V_{L2}, …, V_{LN-1} , V_{LN} respectively.
(v) The values of C_1, C_2,…, C_{N-2}, C_{N-1} are large enough to keep the voltage across themselves constant, equal to V_{C1}, V_{C2}, …, V_{CN-2}, and V_{CN-1} respectively.
(vi) The output voltage is signified by V_o.

Using the conditions listed above, operation of the proposed converter in one cycle can be classified into five operating modes. The equivalent circuit under continuous current mode (CCM) operation is shown in Figure 3. The duty cycle D is defined as the on state of the switch Q when operating within one switching cycle. Details for each operating mode are as follows:

Mode 1 ($t_0 < t < t_1$) : At $t = t_0$, the switch Q is turned on. All diodes of the voltage-lift cells (D_1, D_2, D_{2X},..., D_N, and D_{NX}) are forward biased While all the input inductors (L_1, L_2, …, L_{N-1}, L_N) and charged pump capacitors C_1, C_2,…, C_{N-2}, C_{N-1} are connected in parallel to each other to absorb energy from the power source. The resonant inductor current (I_{Lr}) resonantly increases from the minimum level to create the zero crossing switching (ZCS) condition. During this time interval, the load current is supplied by the discharge current of C_o. The equivalent circuit in this time is shown in Figure 4. The equations that define this operating mode are given as follows:

(2) $$i_{L_r}(t) = \frac{V_g}{Z_1} sin(\omega_1(t - t_0)) + i_{L_r}(t_4)$$

(3) $$I_L = \frac{V_L}{L} t + I_{L\,min}$$

(4) $$V_L = V_g - L\frac{di_{L_r}}{dt}$$

(5) $$V_L = V_g(1 - \frac{L}{Z_1} cos(\omega_1(t - t_0)))$$

where: $Z_1 = \sqrt{\frac{L_r}{C}}$, $C = C_1 + C_2 + ... + C_{N-1}$, $\omega_1 = \frac{1}{\sqrt{L_r C}}$

$$I_L = I_{L_1} = I_{L_2} = ... I_{L_N}$$

$$V_L = V_{L_1} = V_{L_2} = ... = V_{L_N}$$

The voltages across charged pump capacitor are given by:

(6) $$V_C = V_L$$

Where: $V_C = V_{C_1} = V_{C_2} = ... = V_{C_{N-1}}$

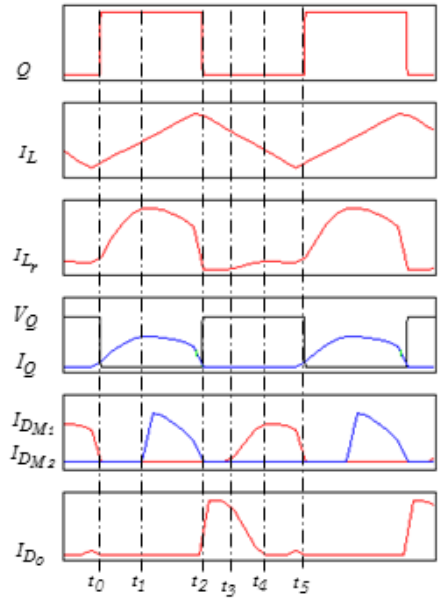

Figure 3. Waveforms of the proposed circuit when operating under CCM conditions

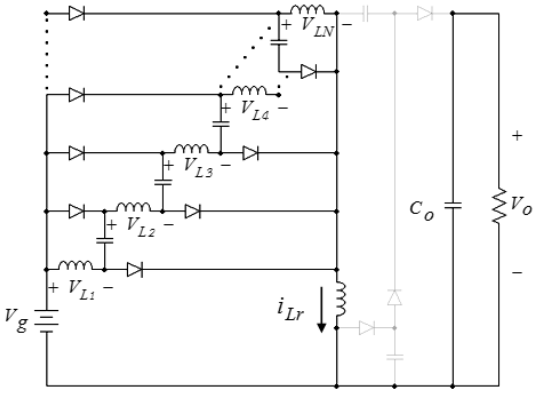

Figure 4. The equivalent circuit in CCM mode 1

Mode 2 ($t_1 < t < t_2$) : Switch Q is still turned on. When C_1, C_2, C_3,…, *and* C_{N-1} are charged to the maximum value, D_{M2} is turned on and the capacitor C_{M1} begins to discharge to C_{M2} through D_{M2}. The current through L_r starts decreasing. The input inductors current is gradually increased to its maximum value. This mode continues until capacitor C_{M1} is completely discharged. The equivalent circuit in this time is shown in Figure 5. The equations related to this operating mode are as follows:

(7) $$i_{L_r}(t) = \frac{V_{C_{M2}}}{Z_2} cos(\omega_2(t - t_2)) - \frac{V_g}{Z_1} sin(\omega_2(t - t_2))$$

(8) $$V_{CM2} + V_{Lr} = V_{CM1} = \frac{V_o}{2}$$

where: $Z_2 = \sqrt{\frac{L_r}{C_e}}$, $\omega_2{}^2 = \frac{1}{L_r(C_e + C)}$, $C_e = \frac{C_{M1}C_{M2}}{C_{M1} + C_{M2}}$

V_o is an output voltage.

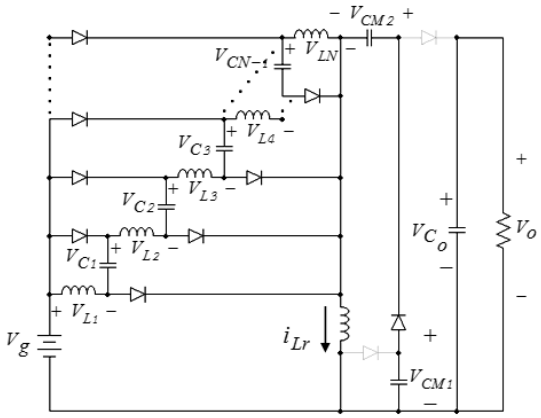

Figure 5. The equivalent circuit in CCM mode 2

Mode 3 ($t_2 < t < t_3$) : At $t = t_2$, the switch Q is turned off, the capacitor C_{M1} is totally discharged, all diodes of voltage-lift cells are reverse biased and output diode D_o is forward-biased. Therefore, the capacitors and inductors in the lift cells begin to discharge in series to each other whilst the C_o is charged. The diode D_{M2} is turned off while the current stops flowing through D_{M2}. During this time, the voltage across the resonant inductor L_r equals zero so the current does not flow through. The equivalent circuit in this operating mode is shown in Figure 6. The equations involved in this operating mode are as follows:

(9) $$i_{L_r}(t) = 0$$

(10) $$V_o = NV_L(t) + (N-1)V_C(t) + V_{CM2}(t)$$

Where: N is step-level of voltage-lift cells

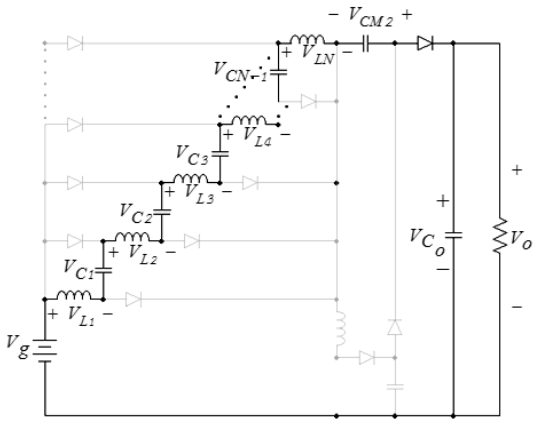

Figure 6. The equivalent circuit in CCM mode 3

Mode 4 ($t_3 < t < t_4$): At $t = t_3$, D_{M1} is forward-biased, then the L_r being discharged to capacitor C_{M1}. The equivalent circuit for this operating mode is shown in Figure 7 and the equations involved are as follows:

(11) $$i_{L_r}(t) = \frac{1}{L_r}(NV_L + (N-1)V_C - V_{CM1})t$$

(12) $$V_{CM1}(t) + V_{L_r}(t) + V_{CM2}(t) = V_o$$

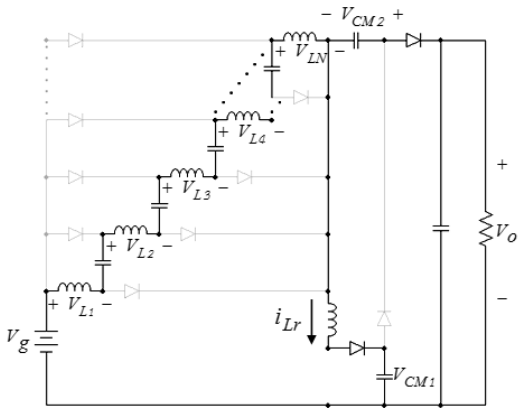

Figure 7. The equivalent circuit in CCM mode 4

Mode 5 ($t4 < t < t5$): When the voltage across L_r equals to zero, the current flows through it will be constant. The stored energy of input inductors L_1, L_2, …, L_{N-1}, and L_N decrease linearly to their minimum values. This mode continues operating until the next switching cycle comes. The equivalent circuit for this operating mode is shown in Fig. 8. The equations involved in this operating mode are as follows:

(13) $$i_{L_r}(t) = I_{L_r}(t_4) = I_{L_r}(t_5)$$

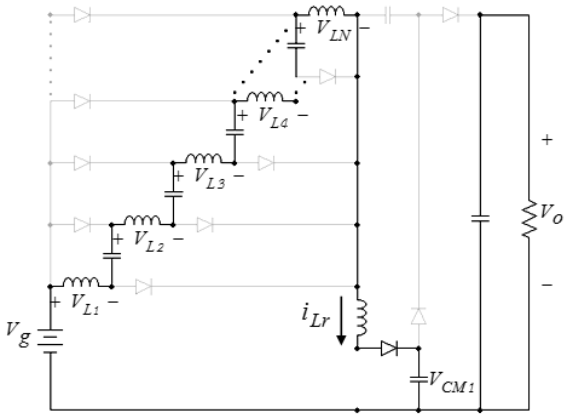

Figure 8. The equivalent circuit in CCM mode 5

Design constraints

To achieve proper operation for the proposed converter, some important constraints have to be taken into consideration, which are detailed as follows:

To achieve the input current to run with CCM operation, the value of input inductors must be ensured greater than the value obtained from (14).

(14) $$L_N \geq \frac{RD(1-D)^2}{8fN} \quad ; N = 1, 2, 3,..$$

The voltage ripple existing across all charge-pump capacitors can be estimated by computing the change in v_{C_1} in the time interval when switch Q is open ($t_2 < t < t_5$) and the current i_L and i_C are the same. According to the voltage ripple of the charge pump capacitors, the value of all charged-pump capacitors can be expressed as

(15) $$C_N \approx \frac{V_g D(1-D)}{2\Delta v_c L_N f^2} \quad ; N = 1, 2, 3,..$$

where $\omega_1 = \frac{1}{\sqrt{L_r C}}$, the resonant inductor L_r can be calculated by using (16)

(16) $$L_r = \frac{1}{4\pi^2 f^2 C_N (N-1)}$$

Therefore, by selecting L_r and C_N, the capacitor C_e can be calculated by using (17):

(17) $$C_e \geq \frac{1}{4\pi^2 f^2 L_r} - (N-1)C_N$$

If capacitor C_{M1} and C_{M2} are equal, then $C_{M1} = 2C_e$

Simulation result

In this section, the validity of the theoretical relations among parameters and corresponding waveforms obtained from the proposed converter with *N*=3 is examined and tested. The simulation parameters used under this study are presented in Table 1; where the simulation program used is the PSIM.

Table 1: Simulation parameter

Parameter	value
$L_{1,,N}$	$80\mu H$
$C_{1,,N}$	$150\mu F$
L_r	$100nH$
C_e	$22\mu F$
R	200Ω
V_g	$24\ V$
Switching frequency	$50\ kHz$
N	3
V_0	$288\ V$

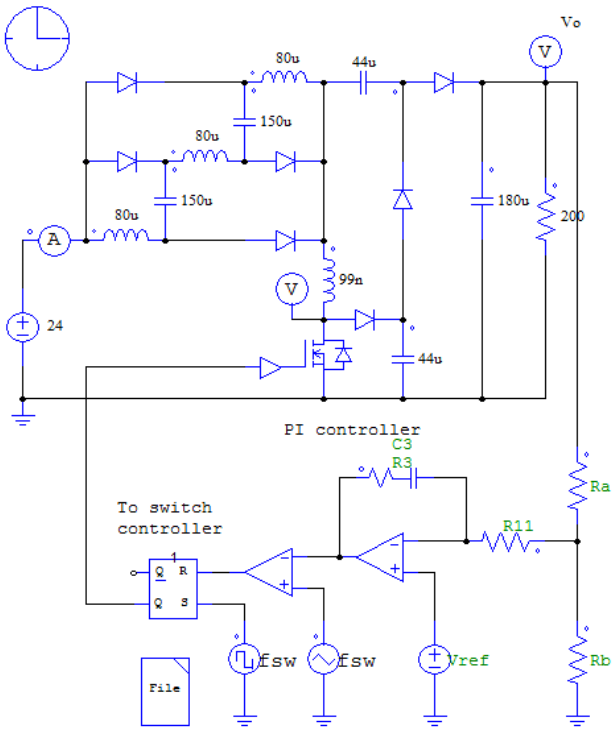

Figure 9. The close-loop control circuit diagram of the proposed converter using the PSIM simulation program

A simple voltage control with a PI-controller is used here to realize the output voltage control for any change in the input voltage and the corresponding reference voltage. Figure 9 shows the simulation circuit diagram of the close-loop control for the proposed converter. The simulation results under CCM operating mode are shown in Figure 10. The voltage and current waveforms of the switch Q, the current through the inductor L_r and the output voltage are illustrated. The switching devices used in this converter have achieved ZCS condition by resonant inductor and charged-pump capacitor at turn ON and OFF.

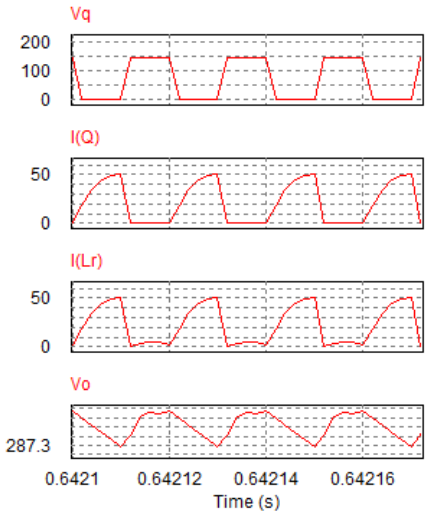

Figure 10. Simulation waveforms of the proposed converter test conditions and parameters in Table 1.

Experimental results

In order to verify the feasibility of the proposed boost converter, a 400W converter prototype of the simulated previous section has been designed and constructed. The photograph of the prototype is shown in Figure 11. The N-channel MOSFET IRFP4568PB was used as the power switch Q. The drain-source on resistance is 4.8mΩ. All diodes in the voltage-lift cells were the diode model MBR6045WT, which have the maximum forward voltage drop is 0.75V. The resonant inductor L_r is placed on the bottom surface of the PCB.

For the input voltage V_g = 24V and the load resistor R = 200 Ω, the output voltage and input voltage waveforms obtained from the operation of the converter prototype are shown in Figure 12, the output voltage was almost constant at 288V. The zero crossing operations of the switching devices are shown in Figure 13, it can be seen that the drain-source voltage and the current waveforms of the main switch Q are operated under the ZCS and ZVS condition. This reduces the switching losses which improves efficiency of converter.

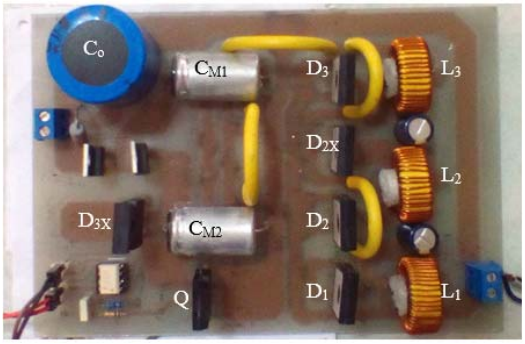

Figure 11. The photograph of the prototype converter with 3 stage voltage-lift cells

Figure.14 shows the curve of efficiency versus output power. The power conversion efficiency was measured at

t = 15 min, while varying the value of load resistance at intervals of 50 Ω . The input and output signals (voltage and current) are recorded at the same time. Through the efficiency formula operation, the efficiency points of different output powers are obtained. The proposed converter achieved η of 96.0% at Po = 400W (rated), 94.0% at Po = 200W. When compared with the converter proposed without passive snubber circuit, there is about 4% efficiency improvement under the rated full load.

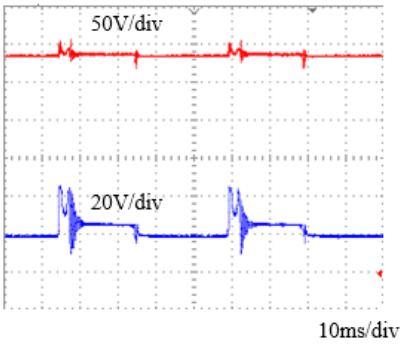

Figure 12. Output voltage V_o (top) and input voltage V_g (bottom)

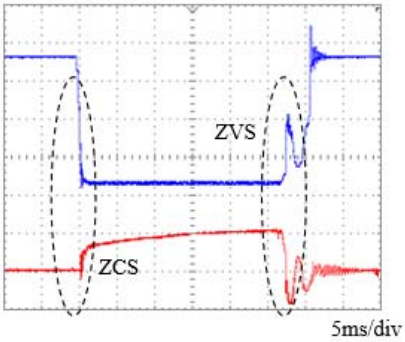

Figure 13. Voltage (top) and current (bottom) waveforms of main switch Q.

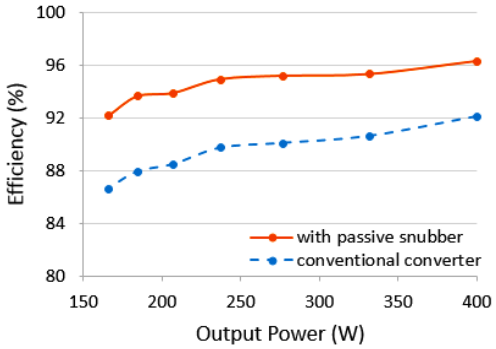

Figure 14. The comparison of efficiencies between the proposed converter and the conventional converter.

Conclusion

The high efficiency high voltage gain boost converter using multistage voltage-lift cells has been proposed in this paper. The proposed converter can achieve a high step-up conversion ratio without a high frequency step-up transformer. Operation principle of the proposed converter has been studied and analyzed.

A passive snubber consists of an inductor, two diodes, and two capacitors, can improve the power conversion efficiency by providing zero-current turn-on and zero-voltage turn-off conditions. At operating condition of V_g=24V, V_0=288V,and P_0=400W. The proposed converter achieved improved efficiency for all the operating load conditions under study and reached the maximum efficiency at 96.0% at rated loads.

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