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Evaluation of SiC and GaN FETs in Zero-Voltage Switching Interleaved Boost Converters

Streszczenie. *W ostatnich latach wzrosła popularność tranzystorów półprzewodnikowych wykonanych z węglika krzemu (SiC) i azotku galu (GaN) w zastosowaniach takich, jak przekształtniki rezonansowe LLC, układy PFC, itp. Niniejszy artykuł prezentuje bezpośrednie porównanie tranzystorów krzemowych, z węglika krzemu oraz z azotku galu w dwufazowym przekształtniku typu boost ZVS o częstotliwości przełączania w zakresie (300 – 500) kHz i mocy 900 W. Poprzez analizę, obliczenia i weryfikację eksperymentalną wykazano, że zastosowanie tranzystorów SiC i GaN skutkuje znaczącym wzrostem sprawności przekształtnika, oraz innymi korzyściami, takimi, jak niższa moc pobierana przez obwody sterowników bramkowych oraz niższa temperatury pracy. (**Ewaluacja stosowania tranzystorów polowych SiC i GaN w wielofazowych przekształtnikach typu boost ZVS**).*

Abstract*. In recent years silicon carbide and gallium nitride transistors have become a popular choice for power converters, such as LLC resonant converters, power factor correction circuits, etc. This paper presents a direct comparison of silicon, silicon carbide and gallium nitride field effect transistors (FETs) in a 900 W, two-phase, zero-voltage switching boost converter with a switching frequency range of (300 – 500) kHz. Through analysis, calculations and experimental examination, it is shown, that using gallium nitride and silicon carbide transistors results in a significant increase in converter efficiency, as well as other benefits, such as lower power consumed by the driving circuits and lower working temperature.*

Słowa kluczowe: wielofazowe przekształtniki typu boost, węglik krzemu, azotek galu, miękkie przełączenia
Keywords: interleaved boost converters, silicon carbide, gallium nitride, zero voltage switching.

Introduction

The advancement of wide bandgap semiconductor technology leads to replacement of silicon (Si) devices, such as power diodes and transistors, with silicon carbide (SiC) and gallium nitride (GaN) components in power electronics applications. Due to their wider bandgap, SiC and GaN devices, allow for higher voltage rating, increased switching frequencies (in relation to Si) and higher power density [1], [2].

As shown in [3], the application of SiC devices has little impact on inverters operating with switching frequency of a few kHz. The same work has also proven the possibility of reducing the size of a low-voltage DC/DC converter, while maintaining high efficiency, by applying SiC devices. The advantage of SiC transistors over Si transistors in high frequency and high power DC/DC and DC/AC converters is discussed in [3] and [4]. Such converters are widely used in renewable energy generation, e.g. photovoltaic systems. A study of SiC MOSFETs performance at high temperature is described in [5]. The article shows that SiC MOSFETs retain good electrical parameters up to 200 °C, although operation under such conditions shortens their lifetime and lowers their reliability.

The authors of [6] show that the use of SiC devices in hard-switching interleaved boost converters, paired with careful design, lead to very high efficiency and power density (ca. 99% and 8 kW/dm^3 respectively) at medium power levels. In [7], a SiC JFET application to a novel zero-voltage zero-current switching (ZVZCS) tapped boost converter topology is described.

Similarly, GaN devices have been increasingly used in power electronic converters recently. In the paper [8], the use of gallium nitride gate injection transistors (GITs) in an inductive power transfer system rated at 2 kW is described. It is shown that GaN devices outperform both SiC and Si devices, achieving up to 95% efficiency in this application. The author of [9] considers the possibility of using GaN devices in class DE inverters, to increase the switching frequency. It is shown analytically that in this application GaN transistors allow higher switching frequency than Si and SiC devices, while maintaining low gate power loss. Gallium nitride devices have also been applied to high frequency LLC resonant converters [10] and power factor correction (PFC) circuits [11] achieving high efficiency and power density.

The aim of this paper is to compare the efficiency of Si-, SiC- and GaN-based multi-phase soft-switching boost converters, which are widely used in photovoltaic systems as step-up stage for the PV module output voltage [12], [13]. Recent development of soft-switching boost converters includes the application of auxiliary switches and diodes ([14], [15], [16]) and passive components ([17], [18]).

Although silicon carbide and gallium nitride transistors have been widely applied to various converter topologies, there is no direct comparison between Si, SiC and GaN FETs under similar conditions, therefore this paper aims to fill this gap. Such a comparison may be useful while choosing transistors for various converters, especially given the differences in pricing of Si, SiC and GaN devices. For the purpose of comparing the performance of Si, SiC, and GaN devices, a classic quasi-resonant two-phase topology has been chosen [19], as it is the simplest multi-phase topology, requiring only two auxiliary capacitors compared to a hard-switching interleaved boost converter.

The article is divided into six sections. Section 1 is the introduction. Section 2 describes the transistors chosen for comparison and details their parameters essential for power loss. Section 3 presents the examined converter topology and details the parameters of the built circuits. Section 4 contains an analysis of transistor power loss in the examined converters. It also provides an analytical comparison of the studied transistors in terms of power loss. Section 5 presents an experimental verification of the analysis. A description of the laboratory setup, as well as the results of temperature and efficiency measurements and comparison are given. Section 6 ends the paper with conclusions drawn from the analysis and experiment.

Examined semiconductor devices

Three TO-247 package transistors were chosen to be examined in the chosen converter topology. The chosen transistors were:

- Si N-channel MOSFET STW36N60M6 [20]
- SiC Cascode UJC06505K [21]
- GaN FET TPH3207WS [22].

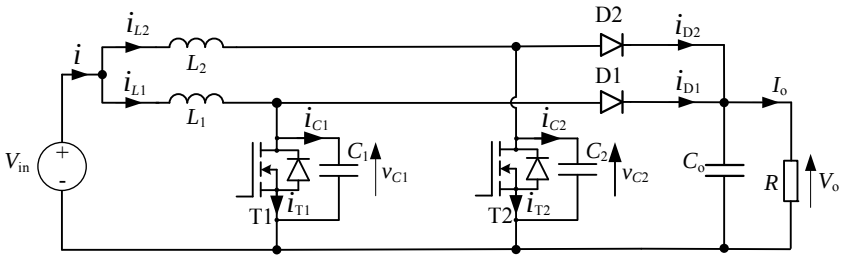

Fig. 1. Topology of the examined converter

Table 1. Chosen parameters of the examined FETs [20-22]

Transistor	STW36N60M6	UJC06505K	TPH3207WS
Material	Silicon	Silicon carbide	Gallium nitride
Max. drain-source voltage	600 V	650 V	650 V
Max. drain current	30 A	36.5 A	50 A
Max. gate voltage	±25 V	±25 V	±18 V
Typical drain-source on resistance	85 mΩ	34 mΩ	35 mΩ
Output capacitance	93 pF	80 pF	202 pF
Total gate charge	44.3 nC	47.5 nC	28 nC
Body diode max. forward voltage	1.6 V	1.9 V	1.9 V

Table 2. Circuit parameters of the converters

Parameter	Value
L_1, L_2	4.5 μH
C_1, C_2	9.9 nF
Nominal V_{in}	60 V
Nominal power	900 W
R	50 Ω
Resonant frequency	Ca. 750 kHz
Switching frequency	(300 – 500) kHz

The semiconductor devices were chosen to have similar drain-source voltage rating and drain current rating. Table 1. compares chosen parameters of each device, important for the resulting power loss.

The chosen boost converter

The topology of the examined converter is shown in Figure 1. ZVS conditions are created by electrical resonances between elements L_1 – C_1 and L_2 – C_2. Two capacitors are added, compared to a hard-switching two-phase boost converter [19]. To simplify the analysis, $L_1 = L_2 = L$ and $C_1 = C_2 = C$ is assumed. There are limitations for soft-switching given by the following formulas [19]:

$$V_o \geq 2V_{in} \tag{1}$$

$$f \leq \frac{1}{2\pi\sqrt{LC}} \tag{2}$$

where V_o is the output voltage, V_{in} is the input voltage, f is the switching frequency and L_1 and C_1 are the inductance and capacitance, respectively.

Three separate converters were built for each of the examined transistor models. The circuit parameters were kept the same for each of the converters. They are given in Table 2. It should be noted that in order to keep the values of C_1 and C_2 the same for each converter, the output capacitance of the examined transistors (see Table 1) had to be considered. Thus, the values of capacitors used were changed accordingly to obtain equivalent capacitances as given in Table 2. STPSC 1006D 600 V, 10 A diodes were used as D1 and D2 (see Fig. 1) in each converter.

Power loss in FETs

A. General expressions

Power losses in FETs may be divided into:

- conduction losses
- gate losses
- switching losses
- freewheeling diode losses.

Due to the nature of the examined converter topology switching losses are near zero and may be neglected, as turn-on occurs at zero voltage conditions and turn-off losses are significantly lowered by adding capacitors C_1 - C_2 [23].

Conduction losses may be calculated by using the following formula:

$$P_c = R_{DSon} I_T^2 \tag{3}$$

where R_{DSon} is the drain-source on resistance, and I_T is the RMS value of the transistor current.

Gate losses general formula is the following:

$$P_G = Q_G V_G f \tag{4}$$

where Q_G is the total gate charge, V_G is the gate-source voltage and f is the switching frequency.

Source-drain freewheeling diode conduction losses can be calculated from:

$$P_{BD} = V_F I_{BD} \tag{5}$$

where V_F is the diode's forward voltage and I_{BD} is the average value of the current flowing through the diode.

B. Conduction power loss

In the case of a two-phase ZVS boost converter the RMS value of current through a transistor is [19]:

$$I_T = I_{0L}\sqrt{\frac{I_{0L}L}{3TV_{in}}} \tag{6}$$

where I_{0L} – inductor current value at the turn off instant, T - switching period of the converter. Therefore, substituting (6) in (3) the following formula for conduction loss in a single transistor is obtained:

$$P_c = R_{DSon}\frac{I_{0L}^3 L}{3TV_{in}} \tag{7}$$

As described in [19], the average output current for one phase can be expressed by:

$$I_o = \frac{I_{1L}T_2}{2T} \tag{8}$$

where T is the switching period, I_{1L} is the inductor current at the time instant when the output diode of the phase starts conducting ([19]), given by:

$$I_{1L} = \sqrt{I_{0L}^2 - \frac{C}{L}(V_o - V_{in})^2} \tag{9}$$

and T_2 is the time of the output diode conducting process in a single period, expressed by:

(10) $$T_2 = \frac{LI_{1L}}{V_o - V_{in}}$$

Solving (7) for I_{1L} yields:

(11) $$I_{1L} = \frac{I_o 2T}{T_2}$$

Thus, by comparing (9) and (11) and substituting T_2 for (10), the following equation is obtained:

(12) $$\sqrt{I_{0L}^2 - \frac{C}{L}(V_o - V_{in})^2} = \frac{I_o 2T(V_o - V_{in})}{L\sqrt{I_{0L}^2 - \frac{C}{L}(V_o - V_{in})^2}}$$

resulting in:

(13) $$I_{0L}^2 - \frac{C}{L}(V_o - V_{in})^2 = \frac{I_o 2T(V_o - V_{in})}{L}$$

Solving for I_{0L} results in:

(14) $$I_{0L} = \sqrt{\frac{I_o 2T(V_o - V_{in}) + C(V_o - V_{in})^2}{L}}$$

In compliance with Ohm's law V_o is:

(15) $$V_o = I_o R$$

Thus, by substituting (15) into (14) one obtains:

(16) $$I_{0L} = \sqrt{\frac{I_o 2T(I_o R - V_{in}) + C(I_o R - V_{in})^2}{L}}$$

Finally, substituting (15) in (6) results in the following formula for a single transistor conduction loss:

(17) $$P_c = \frac{R_{DSon}\left[\frac{I_o 2T(I_o R - V_{in}) + C(I_o R - V_{in})^2}{L}\right]^{\frac{3}{2}} L}{3TV_{in}}$$

Thus connecting conduction loss to the input voltage, output power, switching frequency, resonant circuit *LC* parameters and the drain-source on resistance of the FET.

Using the parameters from Table 1 and Table 2 conduction losses in a single transistor may be calculated for different output power values. Figures 2 and 3 present these calculations for each of the examined transistors. Figure 2 shows the losses at 300 kHz switching frequency, while Figure 3 presents the losses at 500 kHz, with V_{in} = 60 V. The plots show, that the conduction loss rises with the output power, as the RMS value of transistor current also rises. It may further be seen that as the switching frequency rises, the conduction losses drop in value. In both cases the silicon FET STW36N60M6 has the highest loss, as its R_{DSon} is the highest. The losses have similar value for the SiC and GaN transistors, as their R_{DSon} is nearly the same (34 and 35 mΩ respectively). Due to its higher drain-source on resistance, the Si transistor has losses as much as 250% of SiC and GaN switches.

However, the typical value of drain-source on resistance is given in datasheets for a specific junction temperature (usually 25°C). When power loss is dissipated in FETs their junction temperature rises, thus changing the value of R_{DSon}. The characteristic of this change is normally given by the manufacturer in datasheets. The examined FETs' on resistance, at their maximum junction temperature of 150°C reaches up to [20-22]:

- 2.4 times of its typical value for STW36N60M6
- 1.8 times of its typical value for UJC06505K
- 2 times of its typical value for TPH3207WS.

Therefore if the FETs work at temperatures higher than the value at which typical R_{DSon} is given, their drain-source resistance rises, thus raising the conduction loss. Conduction loss reaches its peak at the maximum junction temperature, thus Figures 4 and 5 present the conduction loss as a function of the output power, for each transistor, at the junction temperature of 150°C. As it can be seen, the gap between Si and SiC and GaN FETs further increases. Conduction losses of STW36N60M6 are over 3 times higher than those of UJC06505K. This is because not only Si transistor drain-source on resistance is typically higher than SiC and GaN FETs, but it also has a higher temperature coefficient. The difference between SiC and GaN is also higher, as TPH3207WS has a higher temperature coefficient (2) than UJC06505K (1.8). It should be noted that the calculated losses, plotted in Figures 2-5, are given for a single FET. In the case of the examined converter they should be doubled, as there are two transistors in the topology.

C. Gate power loss

By using equation (4) and the values of total gate charge Q_G (Table 1) of each transistor, the gate loss can be calculated. Gate voltage values were chosen slightly lower than the maximum value. They are also the same as in the experimental setup that is further described in this paper. These values were:

- 23 V for STW36N60M6 transistors
- 23 V for UJC06505K transistors
- 17 V for TPH3207WS transistors.

Gate losses were calculated for each FET in a frequency range of (300 – 500) kHz. The results of the calculations are shown in Figure 6. As it can be seen the gate loss is a positive linear function of frequency ((4)). The rate of this linear increase depends on the total gate charge and gate voltage of the transistor. Silicon carbide FET UJC06505K gate loss is slightly higher than the Si transistor STW36N60M6. This is due to its higher value of total gate charge (Table 1), while the gate voltage value is the same for both FETs.

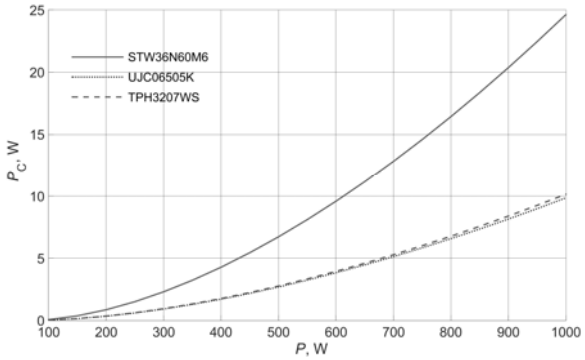

Fig. 2. Calculated conduction loss in a single transistor as a function of output power of the converter at a switching frequency of 300 kHz and junction temperature of 25°C

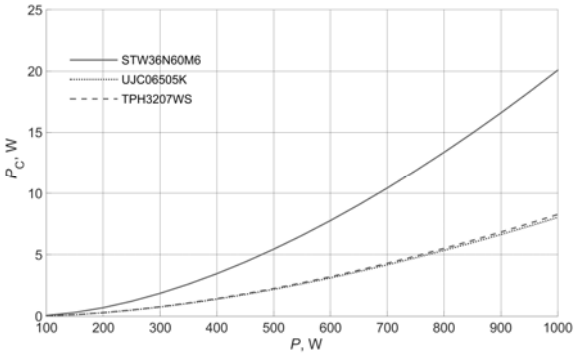

Fig. 3. Calculated conduction loss in a single transistor as a function of output power of the converter at a switching frequency of 500 kHz and junction temperature of 25

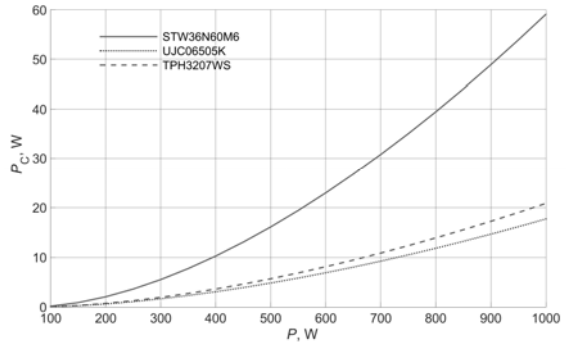

Fig. 4. Calculated conduction loss in a single transistor as a function of output power of the converter at a switching frequency of 300 kHz and junction temperature of 150°C

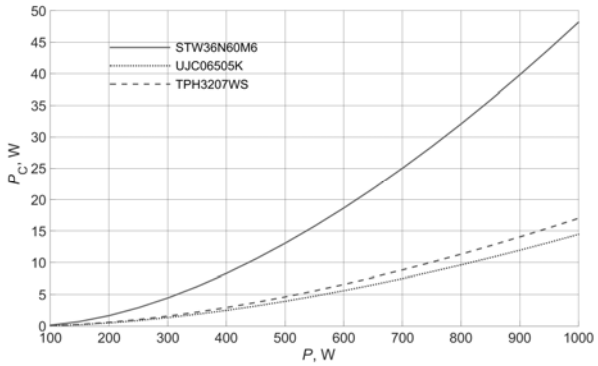

Fig. 5. Calculated conduction loss in a single transistor as a function of output power of the converter at a switching frequency of 500 kHz and junction temperature of 150°C

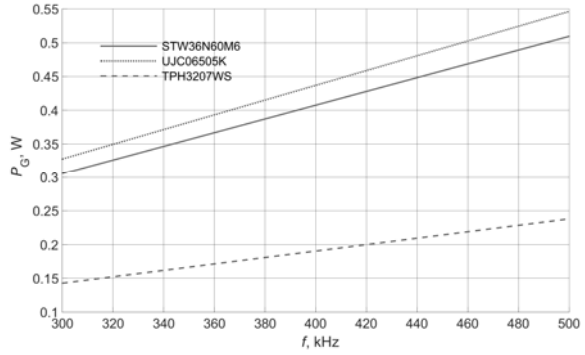

Fig. 6. Calculated gate loss in a single transistor as a function of switching frequency

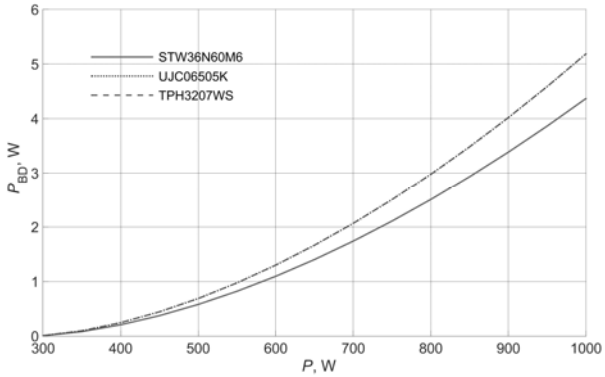

Fig. 7. Calculated freewheeling diode conduction loss in a single transistor as a function of output power of the converter at a switching frequency of 300 kHz.

The gallium nitride transistor gate loss is the lowest, over two times lower than STW36N60M6 and UJC06505K. This is mainly due to its much lower total gate charge (28 nC compared to silicon FET's 44.3 nC and SiC FET's 47.5 nC), but also because of its lower gate voltage (17 V opposed to 23 V).

D. Body diode loss

In the case of a two-phase ZVS boost converter the average value of the current flowing through the body diode is [19]:

$$I_{BD} = \sqrt{\frac{C^{\frac{3}{2}}\left(V_o^2 - 2V_oV_{in}\right)^{\frac{3}{2}}}{3TV_{in}\sqrt{L}}} \tag{18}$$

Thus, by substituting (15) into (18), the following formula is obtained:

$$I_{BD} = \sqrt{\frac{C^{\frac{3}{2}}\left(I_o^2R^2 - 2I_oRV_{in}\right)^{\frac{3}{2}}}{3TV_{in}\sqrt{L}}} \tag{19}$$

Using (19) in (5) yields:

$$P_{BD} = V_F\sqrt{\frac{C^{\frac{3}{2}}\left(I_o^2R^2 - 2I_oRV_{in}\right)^{\frac{3}{2}}}{3TV_{in}\sqrt{L}}} \tag{20}$$

Using the parameters from Table 1 and Table 2 freewheeling diode conduction losses in a single transistor may be calculated for different output power values using equation (20). The losses were calculated assuming the maximum freewheeling diode forward voltage provided by the datasheets [20-22]. Figures 7 and 8 present the results of those calculations.

It can be seen that the silicon FET STW36N60M6 has the lowest body diode loss, as its forward voltage is 1.6 V, compared to SiC and GaN's 1.9 V. By comparing Figures 7 and 8 it can also be deduced, that unlike transistor conduction loss, the body diode loss rises with the switching frequency. It is also noticeable that the body diode loss is about half of the FET conduction loss.

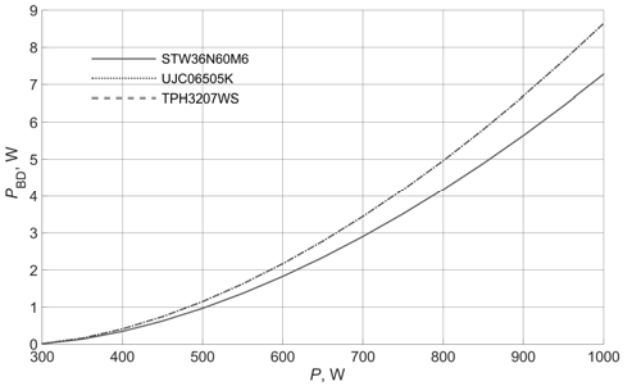

Fig. 8. Calculated freewheeling diode conduction loss in a single transistor as a function of output power of the converter at a switching frequency of 500 kHz

E. Total power loss

The total power loss in a single transistor of the examined converter may be expressed as:

$$P_T = P_C + P_G + P_{BD} \tag{21}$$

The total power loss was calculated using (21) for each of the transistors at both 300 and 500 kHz switching frequencies, and 25°C and 150°C junction temperature. Figures 9-12 present the results of those calculations.

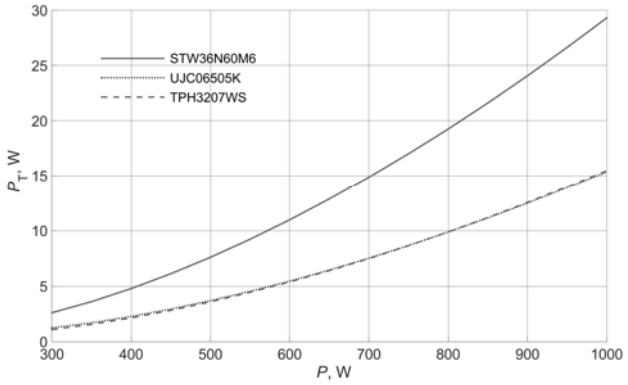

Fig. 9. Calculated total power loss in a single transistor as a function of output power of the converter at a switching frequency of 300 kHz and junction temperature of 25°C

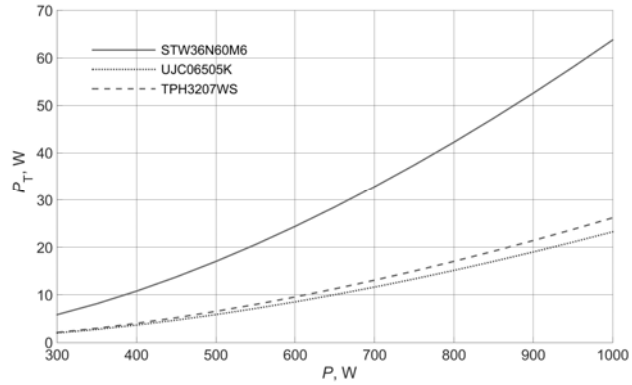

Fig. 10. Calculated total power loss in a single transistor as a function of output power of the converter at a switching frequency of 300 kHz and junction temperature of 150°C

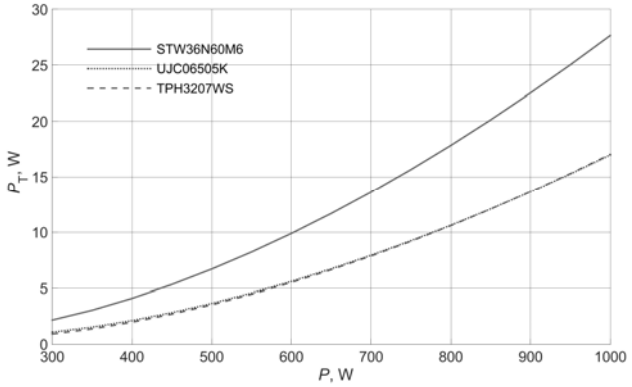

Fig. 11. Calculated total power loss in a single transistor as a function of output power of the converter at a switching frequency of 500 kHz and junction temperature of 25°C

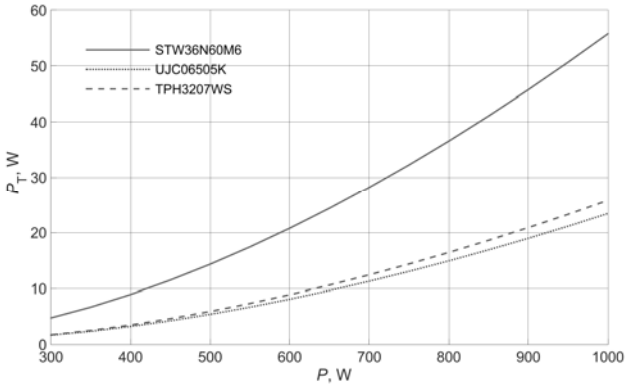

Fig. 12. Calculated total power loss in a single transistor as a function of output power of the converter at a switching frequency of 500 kHz and junction temperature of 150°C

It can be seen that the total power loss of SiC UJC06505K FET and GaN TPH3207WS FET is nearly equal in the examined range of output power at both frequencies, assuming a junction temperature of 25°C. The difference becomes more significant at the maximum junction temperature, as the GaN FET conduction loss rises quicker with temperature. Despite having the lowest freewheeling diode loss and lower gate loss than UJC06505K, the Si transistor, STW36N60M6, has the highest total power loss throughout the output power range, at both switching frequencies and junction temperatures.

Experimental study

A. Experimental setup

As described in Section III, three separate converters were built for each of the examined transistor models. The examined converter was supplied from a 1500 W (0 – 100 V, 0 – 15 A) programmable DC power supply. All three sets of transistors were switched by the same gate drivers, IXDN609CI, supplied from a separate programmable power supply, through push-pull converters. The control signals were generated by an Artix-7-based FPGA system. A 50 Ω laboratory resistor was used as load, while input and output voltage and current were measured by a set of four PC5000A digital multimeters.

B. Temperature measurement

An infrared camera was also used to measure the temperature of the FETs in steady state, at the nominal output power of 900 W. Figures 14-16 present the results of these measurements as infrared photographs. All pictures were taken in the same environment with the ambient temperature varying within the range of 0.5°C of 22°C. Each transistor had the same cooling conditions (heatsinks, thermal paste, etc.) as well. The pictures were taken after loading the converter for 10 minutes. Each photograph contains the view of the whole converter with the transistor heatsinks on the right, and the output diodes heatsinks on the left.

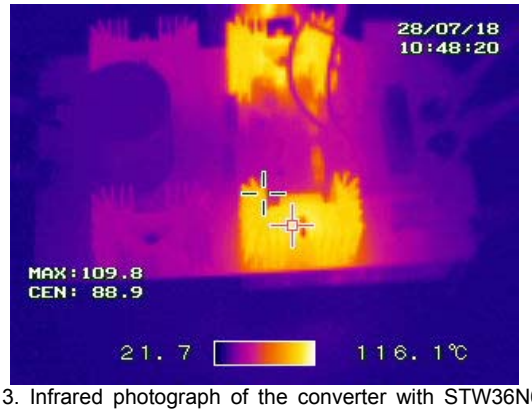

Fig. 13. Infrared photograph of the converter with STW36N60M6 silicon transistors at the nominal output power

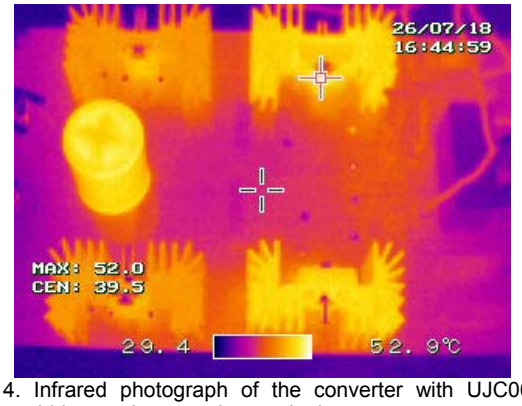

Fig. 14. Infrared photograph of the converter with UJC06505K silicon carbide transistors at the nominal output power

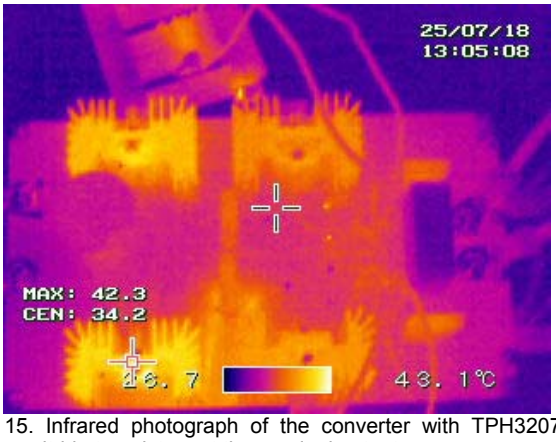

Fig. 15. Infrared photograph of the converter with TPH3207WS gallium nitride transistors at the nominal output power

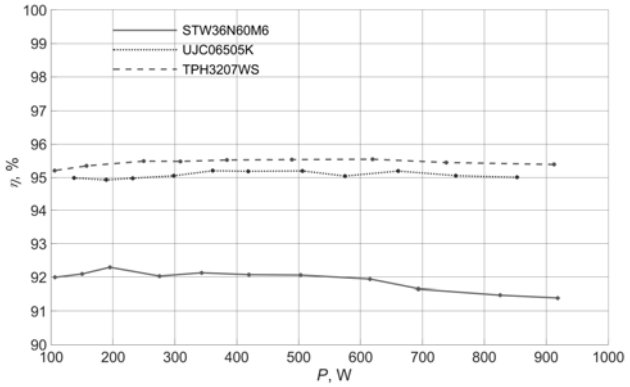

Fig. 16. Overall efficiency of the converter for each of the examined FETs as a function of output power at a switching frequency of 400 kHz

As it can be seen in Figures 13-15, the silicon transistors reach the highest temperatures at nominal load – up to 110°C, while SiC and GaN FETs reach about 52°C and 35°C respectively. This is due to STW36N60M6 transistor higher total power loss, as predicted by Figures 9-12. The examined gallium nitride transistors reach temperatures lower than the output diodes, thus making the diodes a thermal limitation for the converter instead of the switches.

C. Efficiency measurement

Efficiency of the converters was measured as a function of output power, by using digital multimeters to measure the input voltage V_{in}, output voltage V_o, input current I_{in} and output current I_o. The driver circuits power supply output voltage V_{drv} and current I_{drv} were also measured, thus allowing the calculation of efficiency.

The efficiency of the converters was calculated as:

$$\eta = \frac{V_o I_o}{V_{in} I_{in} + V_{drv} I_{drv}} \tag{22}$$

Figure 16 presents the efficiency measurement for each of the transistors at a medium switching frequency of 400 kHz. As it can be seen, the overall efficiency is the lowest when STW36N60M6 silicon transistors are used in the converter, reaching about 92.5%, but dropping to about 91.5% at nominal load, due to the increase of junction temperature. The converter efficiency is the highest when GaN TPH3207WS FETs are used, reaching up to 95.5%, remaining stable at nominal output power as well. The use of silicon carbide transistors UJC06505K results in a significant increase of efficiency, compared to Si transistors and a slight decrease, compared to GaN FETs. The converter reaches up to about 95.2% efficiency when using SiC transistors, remaining above 95% throughout the examined output power range, as well. As predicted by Figures 14 and 15, the output power has little impact on the efficiency of converters using SiC and GaN transistors.. This is due to a very low temperature increase of UJC06505K and TPH3207WS under nominal load. Although analytical predictions suggested, that the efficiency would be highest when using SiC FETs, GaN transistors power loss is lower. This may be due to GaN FETs lower increase of temperature, thus lower conduction losses.

Conclusions

The impact of applying SiC and GaN FETs in two-phase ZVS boost converters has been analysed. It has been established, through calculations and experimental tests that the efficiency rises significantly compared to silicon transistors in the examined frequency and power range. It should be noted that it is possible to decrease power loss in the examined Si FETs, by providing better cooling conditions, thus decreasing drain-source on resistance under load, and therefore decreasing conduction loss. In the examined case however, each FET model was tested under the same cooling conditions.

As the analysis has shown, UJC06505K has the lowest power loss at the same frequency and junction temperature, when compared to other transistors. However, the experimental results show, that the highest efficiency is obtained when using GaN TPH3207WS FETs, possibly due to their lower temperature increase, thus lower conduction losses increase. It should be noted, however that TPH3207WS has a current rating of 50 A, as opposed to 36.5 A current rating of UJC06505K.

The factor of cost should also not be neglected. The price of TPH3207WS is three times higher than the price of UJC6505K, which is also three times higher than that of STW36N60M6, thus making the GaN transistor nine times as expensive as the Si FET. Therefore, as shown by Figures 13-16, SiC transistors are possibly the best economical choice, unless maximum efficiency is essential or the converter works in a high temperature environment.

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