Application of GaN HEMT as a bidirectional switch in matrix converter

Abstract. This paper presents a study of the GaN HEMT as a bidirectional switch. The considerations were conducted for the purpose of application of bidirectional switch in a matrix converter. Semi-soft 4-step commutation method was analysed and laboratory tested on the 2-phase to 1-phase converter to verify all the possible commutation processes which occur in a matrix converter. The problem of wrong sign of current detection and output current interruption has also been raised.

Streszczenie. Artykuł przedstawia badania GaN HEMT jako łącznika dwukierunkowego. Rozważano były prowadzone w celu zastosowania łącznika dwukierunkowego w przekształtniku matrycowym. Metoda 4-krokowej półmiękjej komutacji została przeanalizowana i przebadana laboratoryjnie na przekształtniku 2-fazowym na 1-fazowy, który odzwierciedla wszystkie procesy komutacyjne w przekształtniku matrycowym. Został również poruszony problem błędnej detekcji znaku prądu wyjściowego oraz jego przerwania. (Zastosowanie GaN HEMT jako łącznika dwukierunkowego w przekształtniku matrycowym)

Keywords: matrix converter, bidirectional switch, GaN, semisoft commutation

Introduction
In power electronics, bidirectional (four-quadrant) switches (BDS) are a necessary part of all matrix converters which allow to convert AC voltage directly (without a DC link) to AC voltage with controllable amplitude and frequency. BDS are capable to conduct current in both directions and block voltage of both polarities. There are several configurations of BDS but the most commonly used is antiparallel connection of two RB-IGBT and its main advantage is that the current is passing only through one semiconductor [1]. Nowadays, GaN BDS begin to appear as a single package device with dual gate and are used in matrix converters (MC), e.g. [2, 3], but they are still not available on the market. GaN HEMT could be a competition for RB-IGBT due their lower switching and conduction losses, their high frequency operation which could increase the power density of MCs [3]. GaN HEMT connected in series has not yet been tested as a BDS which was the main reason to conduct the research.

I. Four-step semisoft current commutation method
A. Analysis
The 4-step semisoft current commutation method for BDS was firstly proposed in [4]. It is called semisoft, because half of the commutation process is soft switching and half is hard switching [1]. There are other modifications of that method, e.g. 3-step, 2-step. [5] which are the modification of the 4-step method. To analyse all the commutation processes in a 3-phase MC it is enough to consider only a 2-phase to 1-phase (2f/1f) converter with a DC voltage source and RL load (Fig.1). RC snubbers added to each GaN HEMT significantly reduce the voltage ripple [6], (it is worth mentioning that in [2] for GaN BDS an RCD snubber with 4 diodes, resistor and capacitor is proposed, which could be compared in future work).

Control strategy of the 4-step current commutation method is shown in Table 1. For example, if we want to switch from conducting TAa to open TBa BDS and the current of the RL load is greater than zero, the switching order from column TAa  TBa with Ia > 0 should be selected. A “1100” = TAa1TAa2TBa1TBa2 state means that TAa1 and TAa2 transistors are closed (“1”), TBa1 and TBa2 are opened (“0”). In the first step the transistor TAa2 should be turned off, in the second TBa1 turned on, in the third TAa1 is turned off and in the fourth TBa2 is turned on. For switching under different conditions a correct column should be selected and the switching process is analogous to that described above. For this same sign of current, the sequence of switching process is exactly the same.

Fig.1. Scheme of 2-phase to 1-phase converter with 2 BDS GaN HEMT connected in series with a common source and RL load

B. Simulation studies
Firstly, in order to verify the presented commutation method in a 2f/1f converter simulation studies with the use of an LTspice simulator and the manufacturer (Gan Systems Inc.) spice model of GS66506T transistor which include thermal behaviour and parasitic inductance of leads (around 0.2nH). Also, to reflect a more realistic scenario parasitic inductance of the PCB layers Ls = 40nH has been added at the source and drain terminal, because the GaN HEMT switches current with very high di/dt (even 107) which is the reason of overvoltage. To simulate the turn-on process of BDS in all its four quadrant current-voltage characteristic two variants of Ua and Ub need to be considered.

The work of BDS in the I and II quadrant could be obtained e.g. when Ud = 40V and Ud = 0V and switching between Ta and Tb with duty 0.5 (switching between sequence 12 and 21 with positive current sign). When Ud = 0V and Ud = -40V BDS will work in the other quadrants III and IV (switching between sequence 12 and 21 with negative current sign).

Table 1. Four-step semisoft current commutation for 2f/1f converter

<table>
<thead>
<tr>
<th>Direction of switching order</th>
<th>Step</th>
<th>TAa → TBa (Sequence 12)</th>
<th>TAa ↔ TBa (Sequence 21)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ia &gt; 0</td>
<td>1</td>
<td>1100</td>
<td>1100</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>1000</td>
<td>0100</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>1010</td>
<td>0101</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>0011</td>
<td>0011</td>
</tr>
<tr>
<td>Ia &lt; 0</td>
<td>1</td>
<td>1100</td>
<td>0011</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>1100</td>
<td>0100</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>1010</td>
<td>0101</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>0011</td>
<td>0011</td>
</tr>
</tbody>
</table>

**Table 1.** Four-step semisoft current commutation for 2f/1f converter
Simulation results of that situations have been presented in Fig.2. Other simulation conditions are: switching frequency \( f_s = 5 \text{ kHz} \), load \( R = 16 \Omega, L = 3.51 \text{ mH} \), snubber \( R_s = 50 \Omega, C_s = 1 \text{ nF} \), gate voltage turned on \( V_{\text{GS(on)}} = 6 \text{ V} \) and turned off \( V_{\text{GS(off)}} = -4 \text{ V} \). Dead time between each step of commutation is equal to 200 ns.

Results show that commutation process is proper. The peak of current during commutation which can be seen in Fig.2a is related to the overcharging capacitance of transistors and their snubbers. At drain to source voltages it can be observed that firstly the \( T_{Aa1} \) transistor is turned on so the capacitance has been discharged. Then, only when the current of the switched branch drops to zero (all the load current has been transferred to the other branch) the \( T_{Ba2} \) capacitance is charging (\( T_{Ba2} \) changes the state from reverse conducting to blocking mode) and this charging causes the peak of current. Moreover, the charging current closes at both sources so it could be said that this creates a short-circuit by the capacitance of \( T_{Ba2} \) and its snubber. The same process could be seen in Fig.2d (III quadrant), but when BDS switches in the II and IV quadrant (Fig.2b,c) the current peak does not occur. In that case, the signs of discharging and charging currents of capacitance are the same as the sign of the output current and the process could happen in the same time as the exchange of the load current (not after the exchange like before). The surge of the \( V_{DS} \) voltage is significant during that overcharging process. To reduce that voltage spike, the parasitic inductance had to be reduced and at higher drain to source voltages this is less visible due to lower GaN HEMT capacitances.

\[ \Delta U = R_{DS} I_{DS} + |V_{\text{GS(on)}}| + |V_{\text{GS(off)}}| \]

where: \( R_{DS} \) – drain to source resistance, \( I_{DS} \) – drain to source current, \( V_{\text{GS(on)}} \) – gate to source voltage threshold.

In that case the \( \Delta U \approx 0.67 \Omega \times 1A + |4V| + 1.5V = 5.5 \text{ V} \).

GaN HEMT can conduct in reverse mode only when drain to source voltage \( V_{DS} \) is lower than \( |V_{\text{GS(on)}}| + V_{\text{GS(th)}} \) and the transistor is turned off.

C. Experimental results

To verify this commutation process experimentally two BDS GaN HEMT (Fig.3.) have been designed, built and tested.

One BDS consists of two GS66506T [7] connected in series with a common source controlled by the STM32F407ZE microcontroller. The gate circuit was designed basing on the evaluation board GS66508T-EVBDB2 [8] and an application note [9]. Drain and source of every HEMTs terminal were led out to make the entry check of the switches easier and to allow the modification of the configuration in the future. This, however, increased parasitic inductance. The parameters of the tested model and the switching strategy are the same as those presented in section I A.

Results of the experiment are presented in Fig.4. and they confirm earlier considerations and are very similar to the simulation results. A significant difference could be seen in the \( V_{\text{GS}} \) waveforms where there occurs ringing and undervoltage (which is controlled by +/- 6.5 V TVS). The reason of the oscillation could not be directly indicated because to observe the \( V_{\text{GS}} \) probes with long loops have been used, which could insert additional noise.

After that verification of the commutation method the 2f/1f converter was supplied by 2 phases from the grid by an autotransformer to lower the voltage amplitude. Converter switching between \( T_{Aa} \) and \( T_{Bb} \) with constant frequency \( f_s = 50 \text{ kHz} \) and duty 0.5 generate a sinusoidal current at the output. In cases presented above there was no need to measure the current because it had constant sign. Now, switching between 2 phases required an output current measurement so a current sensor to detect that sign
has been introduced. The result of that experiment could be seen in Fig.5. The converter was protected against power failure or improper current sign detection by a clamp circuit connected to the load to intercept the energy from the inductor. A clamp circuit (CC) (commonly used in MC) has been presented in Fig.6 and consists of a one phase full-bridge rectifier, a 2 μF capacitor, and a 10 kΩ resistor. The

CC had to be built using fast switching diodes to be able to catch the voltage surge in time. The resistance of the load has been changed to 8 Ω, the amplitude of each phase is equal to 30 V and the rest of the parameters are the same as in point I.B.

![Image](image1.png)

**Fig.4.** Experimental results of BDS in all four-quadrant characteristic I-V with a 4-step semisoft current commutation: (a) TAa turning on in I quadrant, (b) TBa turning on in II quadrant, (c) TAa turning on in IV quadrant, (d) TBa turning on in III quadrant. IA, IB, UAa, UBa are in accordance with the scheme from Fig.1. and VGS: TAa1, TAa2, TBa1, TBa2 refer respectively to the gate to source voltage of each HEMT.

![Image](image2.png)

**Fig.5.** Waveforms UDS(TAa1) (CH1), IA (CH2), UA (CH3), IA (CH4) of the two-phase to one-phase converter with constant switching between two phases.

![Image](image3.png)

**Fig.6.** 2f/1f converter with clamp circuit protection.

![Image](image4.png)

**Fig.7a** presents simulation results of wrong current detection (current IA was lower than zero, but the algorithm chose the sequence 21 with IA greater than zero). The voltage UAA and UBB reached around -500 V because the current flows through the capacitance of the HEMTs and their snubbers. For the same case of improper current sign detection a simulation with a CC added to the load has been done, as it could be seen in Fig.7.b. Even if the commutation was wrong the current IA was not interrupted because when the output voltage UA rose over the voltage of the CC the current IA could flow by the capacitor in the CC.

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D. Sign of current detection problem

As it was mentioned in the previous point, the 2f/1f converter has been protected by a CC in case the flow of current IA through the inductor is interrupted. This could cause a voltage surge which would damage the transistor. The same problem could occur at the input of the converter, so the commonly used CC consists of two full-bridge rectifiers connected to the same capacitor.

Another kind of protection could be the varistors added at the input and output of the converter between each phase and the ground. Together with varistors suppressor diodes have also been inserted between the drain and the gate of each HEMT [1].

To show the effects of improper current sign detection a simulation study has been conducted and the results are presented in Fig.7. Only one case has been considered with UA = 0 V, UB = -40 V, and the switching strategy and other circuit parameters remaining the same as in point I.C. Fig.7a presents simulation results of wrong current detection (current IA was lower than zero, but the algorithm chose the sequence 21 with IA greater than zero). The voltage UAA and UBB reached around -500 V because the current flows through the capacitance of the HEMTs and their snubbers. For the same case of improper current sign detection a simulation with a CC added to the load has been done, as it could be seen in Fig.7.b. Even if the commutation was wrong the current IA was not interrupted because when the output voltage UA rose over the voltage of the CC the current IA could flow by the capacitor in the CC.
Fig. 7. Simulation results of BDS during: (a) wrong current sign detection without clamp circuit, (b) wrong current sign detection with clamp circuit, (c) proper current sign detection (I_A, I_B, U_Aa, U_Ba are in accordance with the scheme from the Fig.1. and V_GS: T_Aa1, T_Aa2, T_Ba1, T_Ba2 refers adequate to the gate to source voltage of each HEMT).

The voltage of the U_Ba switch reached only -80 V when in proper commutation (Fig7.c) it reached only -50 V. The capacitance of the CC should be chosen depending on the energy that could be stored in the inductance of the load.

Finally, Fig. 8 shows an example of CC protection when all transistors are suddenly turned off and the energy is transferred to the CC. After turning the transistors off the interrupted current of the load I_b was captured by the clamped circuit. When I_b approached zero amperes the oscillation of the current and the output voltage occurred, but the maximum value of the voltage during that state achieved -100V and could still be better limited using proper values of R and C of the CC.

II. Conclusions

Simulation and experimental studies has been conducted on a 2f/1f converter with BDS built from two GaN HEMT connected in series with a common source. The 4-step current semisoft commutation method was verified in detail and confirmed. The current peak occurs during switching BDS in the I and III quadrant of the I-V characteristics and it is caused by the overcharging of the capacitance of BDS and their snubbers. The application of a tested BDS in the matrix converter is possible. The current sign detection problem was mentioned and a commonly used CC protection to limit that problem was verified.

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