Marek NOWAK, Stanislaw PIRÓG

Rzeszow University of Technology

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Implementation of the Proportional Resonant controller in the FPGA system

Abstract. *The article presents the process of discretization and implementation of the Proportional Resonant controller in a digital programmable system of FPGA type. The synthesis of the regulator in a continuous version is presented and on its basis the discretization has been carried out. The digital form of the regulator has been implemented into the FPGA system. The device has been simulated in real time and this paper presents some of the results of this research. Its aim was to evaluate the operation of the regulator in a digital form, prior to the implementation into a real device. The article is a continuation of the research aimed at the implementation of the regulator in the real device.*

Streszczenie. *W artykule przedstawiono proces dyskretyzacji i implementacji regulatora P+R w cyfrowym układzie programowalnym typu FPGA. Zaprezentowano syntezę regulatora w wersji ciągłej i na jej podstawie przeprowadzono dyskretyzację. Cyfrowa postać regulatora została zaimplementowana do układu FPGA. Przeprowadzona została symulacja urządzenia w czasie rzeczywistym a niniejsza praca prezentuje niektóre wyniki tych badań. Jej celem była ocena pracy regulatora w cyfrowej postaci, przed implementacją do rzeczywistego urządzenia. Artykuł jest kontynuacją badań zmierzających do uruchomienia regulatora w rzeczywistym urządzeniu. (**Realizacja regulatora Proporcjonalno-Rezonansowego w układzie FPGA**)*

Keywords: P+R controller, renewable energy sources, one phase inverter, real time simulation studies, FPGA
Słowa kluczowe: regulator P+R, odnawialne źródła energii, falownik 1-fazowy, badania symulacyjne w czasie rzeczywistym, FPGA

Introduction

The PI regulators are traditionally used in the control systems of single-phase inverters which couple energy sources (e.g. renewable) with the power grid while in three-phase systems the PI regulators are used after transformation to the rotating dq system. The other option is to use a proportional-resonant controller P+R, which works directly on alternating signals. The regulator can be used directly in single-phase and in three-phase systems after transforming the natural system to αβ. [1]

P+R controller, in an ideal version, has infinite gain and zero phase shift to the signal which is tuned with controller. Signals with other frequencies are dumped and phase shifted in relation to the input signal – according to the amplitude and frequency characteristic. In the real solutions, a controller with limited amplification for resonant frequency is used. In the scientific literature there are also examples of the modified structures of the regulator which aim to improve its operation in unstable power supply conditions.. [1-3]

Control systems may be based on microprocessor systems or faster programmable logic devices (e.g. FPGA or CPLD). In the FPGA device, controller and modulation system may be implemented, what is troublesome in the microprocessor system. [4]

Additionally, in the FPGA system, it is possible to perform real time simulation. The advantage of such a solution is the possibility of testing the regulator, with structure and parameters, which will operate in a real device. For that , discrete model of the converter, which will be controlled by regulator and power source models (to be connected by converter) should be developed. [5, 6].

In this publication a Terasic ADC-SOC development board with Cyclone V 5CSEMA4U23C6N series FPGA system was used as a platform for simulation (fig. 1)

The research presented in the article is a continuation of the simulation research presented in [7]. It concerned the continuous structure of the P+R regulator proposed in [1]. The obtained results proved that the tested P+R structure can be used as a current regulator in the inverter that couples the energy source with the power grid. The next stage of the research is to discrete the regulator, what is presented in this publication.

Fig.1. FPGA development board with Cyclone V 5CSEMA4U23C6N device.

P+R synthesis

The transmittance of the controller is [1]:

$$G_{P+R}(s) = K_P + \frac{2K_I \xi \omega s}{s^2 + 2\xi\omega s + \omega^2} \tag{1}$$

Synthesis of the resonance part of the controller [7] :

$$G_R(s) = \frac{Y_R}{X} = \frac{s}{s^2 + 2\xi\omega s + \omega^2} \tag{2}$$

where: X – input signal, Y_R – output signal of the resonance part

Equation (2) can be transformed as follows:

$$Y_R s^2 + 2Y_R \xi\omega s + Y_R \omega^2 = Xs \tag{3}$$

$$Y_R + \frac{Y_R 2\xi\omega}{s} + Y_R \frac{\omega^2}{s^2} = \frac{X}{s} \tag{4}$$

$$Y_R = \frac{X}{s} - Y_R \frac{2\xi\omega}{s} - Y_R \frac{\omega^2}{s^2} = \frac{1}{s}\left[X - 2\xi\omega Y_R - \frac{\omega^2}{s} Y_R \right] \tag{5}$$

Assuming that:

(6) $$\xi\omega = \frac{k}{2T_1}; \omega = \frac{1}{\sqrt{T_1 T_2}}$$

the resonance part can be implemented in the following way:

(7) $$Y_R = \frac{1}{T_1 s}\left(X - kY_R - \frac{1}{T_2 s} Y_R \right)$$

The result is a structure consisting of simple blocks (P or I). An integral with T_2 integration time and a proportional part with k gain creates a parallel structure of the PI regulator. The structure of the P+R regulator is shown in fig. 2 - the resonance part of the regulator is distinguished by a dashed line.

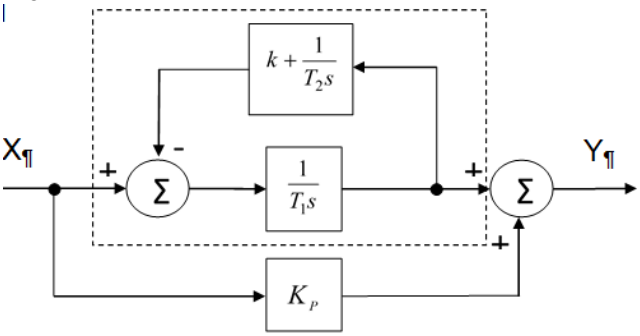

Fig.2. Proposed structure of the P+R controller

It is assumed that $T_1=T_2=T$. Therefore, the relation of X ents from the equation (1) i (7): Y

(8) $$k = \frac{1}{K_i}; \ \omega = \frac{1}{T}; \xi = \frac{1}{2K_i}$$

Discrete PI and P+R controller

The output signal of the PI controller in the time domain is described by equation:

(9) $$y(t) = Px + \frac{1}{T_i}\int_0^t x dt$$

where: P – proportional part gain T_i – integration time, x – input signal, y – output signal.

Realizing the integration with the rectangle method, the PI structure equation in discrete steps of time n:

(10) $$y(n) = Px + \frac{\tau_i}{T_i}\sum_0^n x(n)$$

where: τ_i – integration step.

(11) $$y(n) = Px + I\left[S(n-1) + \frac{\tau_i}{T_i} x(n) \right]$$

where: I – scaling factor of the integrating part,

The $S(n-1)$ factor is equal to the sum of the previous integration steps:

(12) $$S(n-1) = \frac{\tau_i}{T_i}\sum_0^{n-1} x(n)$$

The parallel structure of the PI regulator with the limitation of the output signal due to the operating conditions of the system is shown in fig. 3.

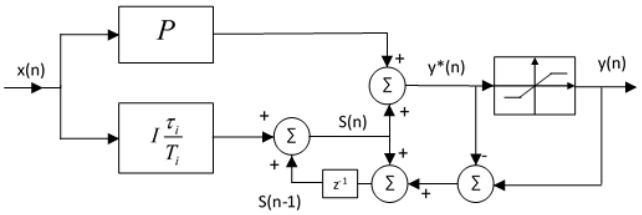

Fig.3. Discrete structure of the pararell PI controller

Real time simulation of 1 phase inverter with P+R controller

The simulation tests of a single-phase inverter with a P+R controller were carried out in real time using the Quartus II software package. The P+R controller was part of an inverter control system that couples a single-phase power line with an energy source.

The blocks implemented in the program were divided into two parts - a simulating power circuit (energy source, inverter and power supply line) and a control system (regulator, modulation system, generation of a pattern current signal). Table 1 presents the assumptions adopted during the simulation of the system with the digital P+R controller.

Table 1. The parameters of the simulation

Grid	
Voltage	One phase, 230 V RMS
Frequency	50 Hz
Power supply line	R_L=1 Ω
Inverter	
Power P_N	3 kW
Maximum current	13 A RMS
DC Supply voltage	400 V
Modulation	unipolar
Pulse frequency	24 kHz
Line choke	L_C=2 mH
P+R Controller	
K_p	1
K_I	100
T	0.003183
Operating frequency	5 kHz

The reference waveform of the line current is obtained by multiplying the scaled current amplitude value (kI_{sRef}) by the scaled phase voltage at the point of connection of the system to the network. The kI_{sRef} coefficient is limited by software, so that the maximum current value is not exceeded. A properly scaled phase voltage signal is added to the regulator output signal. ($k_u u_s$). As a result, assuming that the output signal of the P+R regulator is equal to 0, no current will flow through the line. The diagram of the tested system is presented in figure 5.

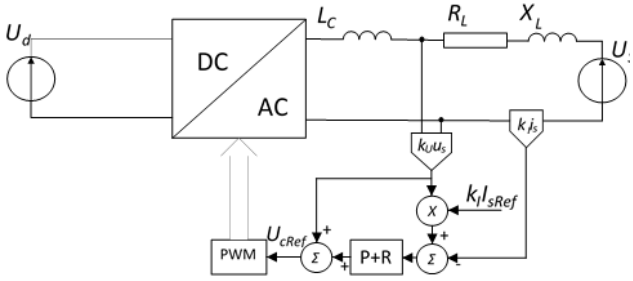

Fig.5. Diagram of the tested system

Because in the low voltage AC lines $R_L>>X_L$ its reactance has been skipped in the calculations. The current flowing in the line is the result of the voltage difference of the inverter. Its waveform is described by the equation:

$$i(t)=\frac{u_L}{R_L}\left(1-e^{-R_L t/L_C}\right) \tag{13}$$

In the simulation studies the digital representation of the equation (13) was used [2]:

$$G_O(z)=\frac{i(z)}{u(z)}=\frac{1}{R}\frac{1-e^{\frac{-T_P}{T}}}{z-e^{\frac{-T_P}{T}}} \tag{14}$$

where: $T=L/R$, and T_P is the sampling period.

On the basis of equation (14), the values of the line current were determined at discrete intervals. These calculations were carried out at a frequency of 240 kHz.

$$i(n)=\frac{u_L(n-1)}{R_L}(1-e^{\frac{-T_P}{T}})+i(n-1)e^{\frac{-T_P}{T}} \tag{15}$$

where: $i(n)$ – is the current value in the nth time sample, $i(n-1)$ – current value in previous time sample, $u_s(n-1)$ – value of voltage difference between inverter and line voltages

The inverter block, based on transistor control signals, determines the output value, that depends on the source voltage value - $+U_d$, $-U_d$ or 0 as a result of pulse width modulation. It has been assumed that the transistors of the inverter are ideal switches and dead times have been taken into account in their operation.

The blocks that make up the control system are the P+R regulator, and the unipolar modulator consisting of a triangular course generator and two numerical comparators. The triangular waveform generator has been implemented as a counter in code U2. It counts clock pulses of control signals to a given value and then changes the counting direction. As a result, a triangular waveform with a frequency of 24 kHz is obtained at the counter output. Two numerical comparators compare the output signal from the regulator and the triangular waveform, thus generating signals controlling transistors.

Figure 6 shows the block diagram of the i modules implemented in the FPGA system in order to carry out simulation tests.

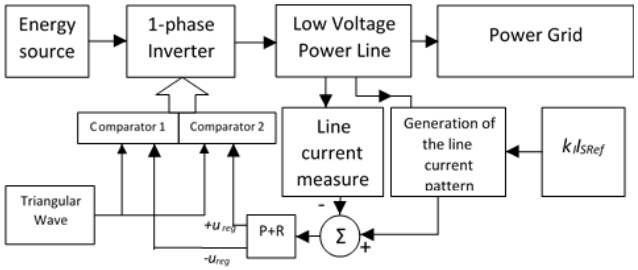

Fig.6. Schemat blokowy układu do badań symulacyjnych, zaimplementowany do układu FPGA.

Simulation tests in real time included the following issues - system start-up, changes in the setpoint value of the line current and the situation when controller was not tuned to the grid frequency. The results of the simulation were presented using SignalTap II Logic Analyzer. It uses the JTAG communication protocol to communicate with the development environment. Samples of the tested signals are stored in the memory cells of the device and then read out by the program by JTAG. In order to illustrate the operation of the system, SignalTap II observed the waveforms of voltage and current of the line. To improve the accuracy of the calculation and also the operation of the control system, some of the signals have an extended range. The relevant signals are multiplied by 2^N depending on the needs and available resources of the device. The format of a physical quantity with such an extended range is marked as QN. Voltage value is given in Q5 format and line current in Q10 format. For clarity, the voltage shown on the waveforms has a value in Q0 format.

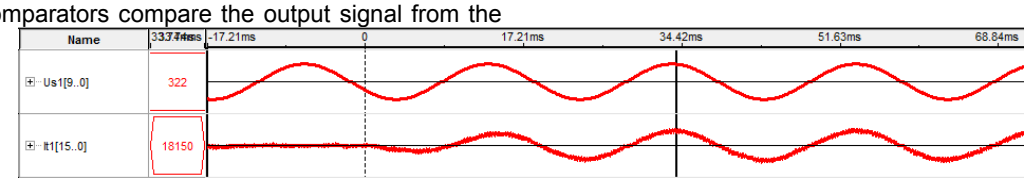

Fig.7. Device start-up, change of amplitude of preset current from 0 A to 13 A RMS (18150_{Q10}=$17,72_{Q0}$)

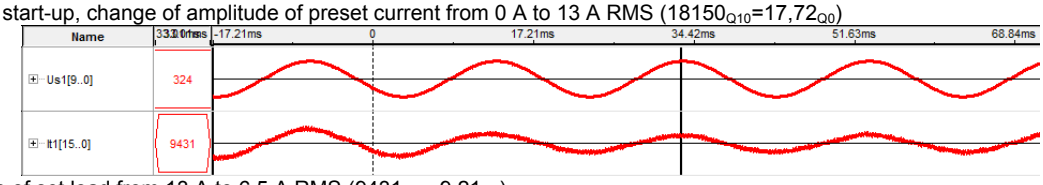

Fig.8. Change of set load from 13 A to 6.5 A RMS (9431_{Q10}=$9,21_{Q0}$)

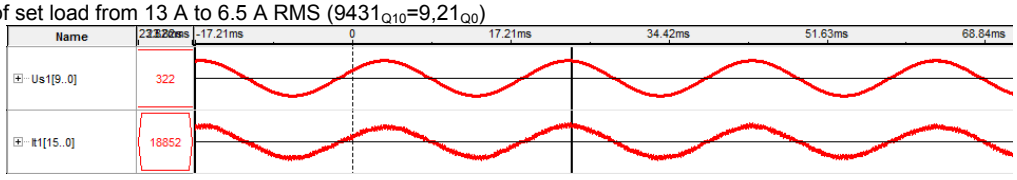

Fig.9. The waveform of voltage and current of the line in the unadjusted state of the controller frequency to the network frequencyi $f_r<f_s$ (18852_{Q10}=$18,41_{Q0}$)

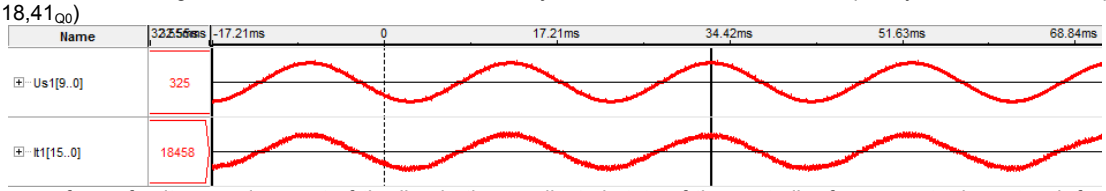

Fig.10. The waveform of voltage and current of the line in the unadjusted state of the controller frequency to the network frequency $f_r>f_s$ (18458_{Q10}=$18,02_{Q0}$)

Figure 7 shows the voltage and current waveforms of the power line supplying the system during start-up. The set power changed from 0 to P_N (13 A RMS, which corresponds to the maximum power) The system reacted correctly and in the second period after the set change, it reached the set course.

Figure 8 shows the change of the inverter setpoint load from P_N to $0.5P_N$ (from 13 to 6.5 A RMS). As in the previous test, in the second period after the preset change, the line current reached the preset value.

Figures 9 and 10 show the results of a test in which the controller is slightly unadjusted to the mains frequency (± 1 Hz). Figure 9 shows the waveform when the resonance frequency of the controller f_R is less than the f_S (49 Hz), and in the figure 10 f_R was bigger than f_S (51 Hz). The voltage and current flows of the supply line are in phase with each other. Because of this, a slight unadjustment of the controller has no negative impact on the operation of the system.

Summary

The carried out simulation tests showed the correct operation of the digital structure of the P+R controller. It can be used as a current regulator in a real inverter coupling the energy source with the power grid. It reacted well to the load changes. Slight unadjustment of the regulator's parameters to the network to which the inverter was connected to the energy source did not cause any visible irregularities in its operation.

The real time simulation studies was performed with the use of a platform with FPGA. The advantage of such a solution is the possibility of testing the control system in the form in which it can be implemented in a real device. During such tests, the control system cooperates with blocks in which parameters concerning, as in this case, the power grid, inverter and energy source are artificially generated. It is difficult to assess how it will work with real devices, e.g. A/D converters or transistor controllers. It may turn out that the structure, which worked properly during the simulation tests, may require improvements in the real device. Therefore, an experiment should be carried out to finally verify the operation of the P+R regulator.

***Authors**: Marek Nowak, MSc, Eng., Rzeszow University of Technology, Faculty of Electrical and Computer Engineering, W. Pola 2, 35-959 Rzeszów, E-mail: mnowak@prz.edu.pl; Prof. Stanisław Piróg, PhD, Eng., Rzeszow University of Technology, Faculty of Electrical and Computer Engineering, W. Pola 2, 35-959 Rzeszów, E-mail: pirog@prz.edu.pl.*

REFERENCES

[1] R. Teodorescu, F. Blaabjerg, M. Liserre, P.C. Loh, "Proportional-resonant controllers and filters for grid-connected voltage-source converters", IEE proceedings-Electric Power Applications, vol. 153, no. 5, pp. 750-762, Sep. 2006.

[2] Tuan Ngo and S. Santoso, "Improving proportional-resonant controller for unbalanced voltage and frequency variation grid," 2016 IEEE/PES Transmission and Distribution Conference and Exposition (T&D), Dallas, TX, 2016, pp. 1-5.

[3] D. Stojić, M. Milinković, S. Veinović and I. Klasnić, "Novel proportional-integral-resonant current controller for three phase PWM converters," 2016 4th International Symposium on Environmental Friendly Energies and Applications (EFEA), Belgrade, 2016, pp. 1-4.

[4] R. Stala, M. Baszyński, „Sterowanie i modelowanie przekształtników energoelektronicznych w układach FPGA", AGH Uczelniane wydawnictwo naukowo dydaktyczne, Kraków, 2011.

[5] A. Penczek, R. Stala, Ł. Stawiarski, M. Szarek, "Hardware-in-the-Loop FPGA-based simulations of switch-mode converters for research and educational purposes", Przegląd Elektrotechniczny, R 87, NR 11/2011.

[6] M. Mudrov, A. Zyuzev, K. Nesterov, S. Valtchev, "FPGA-based Hardware-in-the-Loop system bits capacity evaluation based on induction motor model," 2017 IEEE International Conference on Environment and Electrical Engineering and 2017 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I&CPS Europe), Milan, 2017, pp. 1-5.

[7] M.Nowak, S. Piróg, "Simulation studies of the Proportional Resonant controller", Przegląd Elektrotechniczny NR 6 (2018), s. 128