Kazimierz MIKOŁAJUK, Zbigniew STAROSZCZYK, Andrzej TOBOŁA

Warsaw University of Technology

doi:10.15199/48.2019.06.18

Synchronization of the iterative process for voltage harmonic mitigation

Abstract. *The paper presents the method of the reference signal generation for the shunt active power filter control. The signal is iteratively tuned basing on voltage harmonics frequency domain observations. The process needs few steps of iteration (each a period long) to obtain steady-state compensator current assuring neglected levels of voltage.*

Streszczenie. *Podano metodę wyznaczania sygnału referencyjnego do sterowania aktywnego filtru energetycznego. Prądowy sygnał filtru jest obliczany na podatnie harmonicznych napięcia. W metodzie wykorzystywany jest obserwator działający w dziedzinie częstotliwości.. Proces wymaga kilku kroków iteracji do uzyskania prądu redukującego harmoniczne napięcia.* ***Synchronizacja iteracyjnego procesu redukcji harmonicznych napięcia***

Keywords: active power filters, detection of voltage harmonics, iteration algorithm.
Słowa kluczowe: energetyczne filtry aktywne, eliminacja harmonicznych napięcia, algorytm iteracyjny.

Introduction

The control of active power filters can be divided into three groups: control based on instantaneous power, control based on current, and control based on voltage measurements. The shunt active filters based on voltage detection at the points of compensator installation seem to be more flexible then current-controlled compensators [1]. The power necessary for active filtering can be maintained at a very low level with an accurate design of control and of the passive components. For example, the power usage of the active filter can be about 1.5% of the nominal value. The voltage-controlled method, which does not require the knowledge of the load current, determines the reference signal basing only on voltage waveform observations at the point of filter installation (PCC) and then injects the proper compensating current. Such filters should be installed in the power system rather not by consumers, but by the grid operator.

The voltage-controlled method proposed in [2] forms a feedback control loop. The filter detects voltage harmonics at the point of filter installation, and then injects a compensating current. The active filter forms a short-cut for all harmonic except of the fundamental frequency. For fundamental harmonics it forms the open circuit. This method is fast as it is based on instantaneous voltage and current observations. However time delays (phase shifts) in active controller deteriorate harmonics damping and can lead to filter instability. The modifications presented in [3] are based on the assumption that all harmonics of the compensator current should be orthogonal to voltage harmonics (phase shift of π/2) as the grid impedance has dominating inductive character. More information on system parameters can be obtained from the experiments proposed in [4,5].

The vector control is the another common approach to harmonics compensation. With the synchronous reference frame implemented in grid-tie converters the varying quantities appear as constant and can be eliminated by PI feedback controllers. The details of the method based on multiple reference frame control are presented in [1].

The other methods [6,7,8] can be classified as iterative or repetitive. The methods presented in [9,10] belongs to iterative methods. These methods operate in a frequency domain and need the identification process being extended for a longer time interval. Such process is described in this paper. The synchronization of the signals within the compensation process is necessary because of the delays in the feedback loop.

The block diagram presented in Fig. 1 illustrates the process of reference current obtaining, by the iterative method.

The compensating process starts from transformation of grid voltage time function to frequency representation. This operation is carried out in the block named SLIDING DFT.

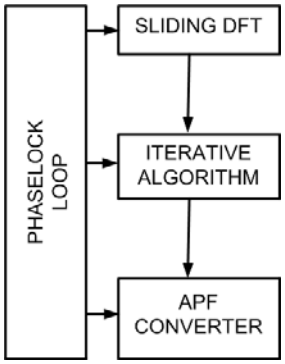

Fig. 1. Block diagram illustrating the iterative process of reference current detection for APF

It is assumed that the grid voltage is periodical or close to periodical time function. Hence, the operation of the sliding DFT produces set of complex numbers representing voltage harmonics. These harmonics are further processed in the block ITERATIVE ALGORITHM, which generates the control signal for the next block APF CONVERTER. The supervising PHASELOCK LOOP block synchronizes the processing of the mentioned three blocks on longer time intervals. The blocs presented in Fig. 2 are described below, with the main focus on the phase-locked loop and the sliding DFT used in the iterative signal processing.

Phase-locked loop, window synchronization

The phase-locked loop technique (PLL) was originated in 1930's and was designed for synchronous reception of radio signals. Since then, it has found many applications in different areas. Among others, it is used for the generation of the reference current for power quality conditioners and for synchronization of power quality converters. The bibliography concerning the phase-locked techniques oriented on power electronic application is numerous [11,12,13].

To explain the principle of the PLL implemented in the procedure proposed in the paper, the SIMULINK model shown in Fig. 2 is considered. This model is similar to that being presented in [12], but extends it with the additional path for period value calculation.

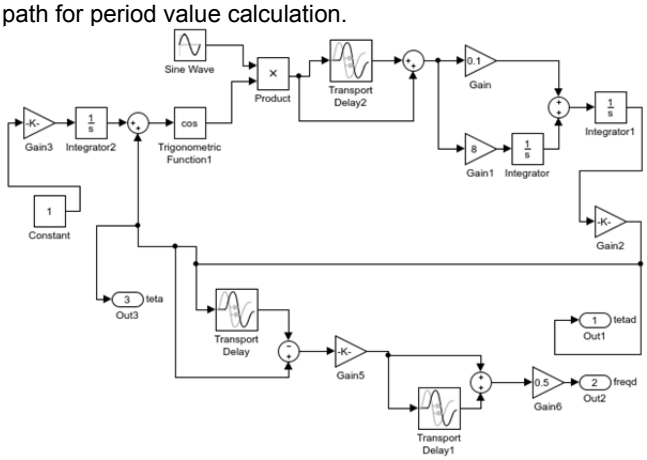

Fig. 2. SIMULINK PLL model

The precise estimation of the system voltage period is essential for the iterative control described in this paper. This parameter is necessary in order to compute accurate Fourier representation of the processed voltage. The phase (running phase) of this voltage is the second important signal useful at the presented method. The knowledge of initial phases is needed for accurate signal synchronization on long time intervals.

Four frequencies f_{ini}, f_i, f_d, f are used in the model: rating frequency $f_{ini} = 50Hz$, grid frequency $f_i = 51Hz$ difference of frequencies in quest $f_d = f_i - f_{ini}$, grid frequency f as the result of the PLL action.

The model in Fig. 2 contains two signal sources. Block Sine Wave with input parameters: ($frequency = 2\pi f_i$, $f_i = 51$Hz initial phase $\psi_i = \pi/2$) and amplitude $U_i = 2$ represents grid voltage. Block Trigonometric Function generates the oscillator cosine signal. The running phase of the oscillator is composed of two functions. Linear time function is generated by blocks: Constant (const value =1), Gain3 ($2\pi f_{ini}$, $f_{ini} = 50$ Hz) and Integrator2. The feedback signal is added to linear time function and this sum becomes the argument of the cosine block. The block Product multiplies two signals - grid voltage and oscillator signal. The result of this block operation can be expressed according to the general trigonometric property

$$2\sin\alpha\cos\beta = \sin(\alpha+\beta)+\sin(\alpha-\beta) \quad (1)$$

In the considered application $\alpha = 2\pi f_i + \psi_i$, $\beta = 2\pi f_{ini} + \psi_{ini}$. For $f_i \neq f_{ini}$ one component is slowly varying time function, for $f_i = f_{ini}$ this component becomes constant. The remaining fast varying component is close to the second harmonic.

Second harmonic should be reduced, the ripples causes errors and impedes the control. The constant component is reduced to zero owing to the feedback loop containing integer blocks. It is seen from (1), that zero constant component means α=β, and for $f_i = f_{ini}$, it means $\psi_i = \psi_{ini}$. The oscillator initial phase follows the grid voltage initial phase, for the assumed value $\psi_{ini} \to \frac{\pi}{2}$

The second harmonic generated in multiplier is reduced with the use of block Transport Delay2 $delay = \frac{1}{4 f_{ini}} = 0.005$ s [12]. The feedback path contains two integrators (Gain2=0.6E+3). Owing to the integrators the error of the running phase brought to cosine function block is reduced to zero.

The second path designed for frequency calculation contains two Transport Delay blocks. The essential here is the activity of the first block with delay equal to twice nominal periods (0.04s) The second block (Transport Delay1) with delay equal 0.005s additionally reduces ripples observed in the feedback path. Simulation results are presented in Figs. 3,4,5,6.

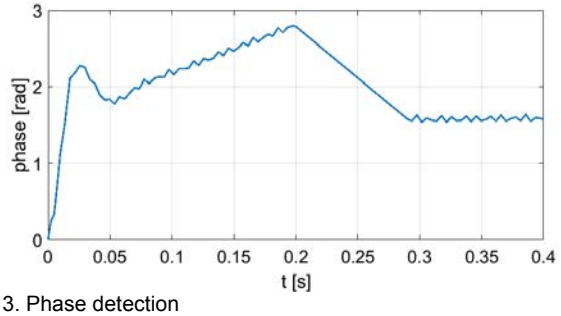

Fig. 3. Phase detection

As was mentioned, Fig.2 model contains two main paths. The first path with the output Out1 (described above) forms the feedback loop. It delivers the running phase resulting from the discrepancy between the assumed oscillator and the actual grid frequencies (frequency error). For both stable frequencies, this running phase form a linearly varying time function, with the slope proportional to the frequency error. The variation of the running phase informs on frequency instability. The linear variation of the phase can be observed in Fig. 3 within simulation time interval (0.05s,0.2s). The phase waveform observed during the interval (0,0.05s) describes the initial transient state. Comments on the final segment of the waveform are given below. The observed waveform ripples result from imperfect filtration of the second harmonic.

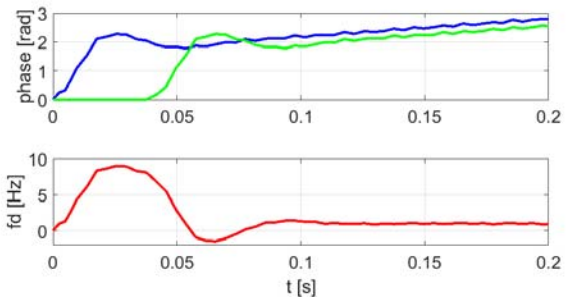

Fig. 4. . Illustration for the deviated frequency calculation

The power system frequency deviates from nominal value by small amount. As was mentioned, the frequency difference between oscillator and grid leads to the phase variation. The variable phases before delay and after delay (Fig. 2) are shown in Fig. 4. In Fig. 4 the blue line shows the variability of the supplemented phase before delay and green line shows this phase after delay.

The access to the difference between phases enables one to compute the frequency amendment, according to the expressions

(2) $$2\pi f_d t - (2\pi f_d (t - \Delta t) = -\Delta\theta(t)$$

(3) $$f_d = \frac{\Delta\theta}{2\pi\Delta t}$$

The expression (2) was used to determine Gain6 of model shown in Fig. 2. The red line shows the frequency amendment. From the waveform shown in Fig. 4 (red line), for $t = 0.2$ s, we have $f_d = 0.9734$ Hz. It means, that estimated grid frequency is $f = 50.9174$ Hz, and period $T = 0.0196$ s. This period can be used for DFT as the window length. This new frequency was applied in model shown in Fig.2 for the lengthened simulation time (0.2s, 0.4s). The result can be observed in Fig. 3. We can see, that after the frequency correction the phase remains constant. According to general condition (1) this constant function takes the value equal to the initial phase given for the grid voltage (block Sine Wave in Fig.2). From the phase waveform (Fig. 3) for $t = 0.4$ s, we have , $\psi(0.04) = 1.5616$ rad, which is close to the inserted value $\psi_i = \pi/2$. Resuming the above comments, we can state, that PLL presented in Fig. 2 delivers two important parameters of the identified voltage – its frequency and initial phase.

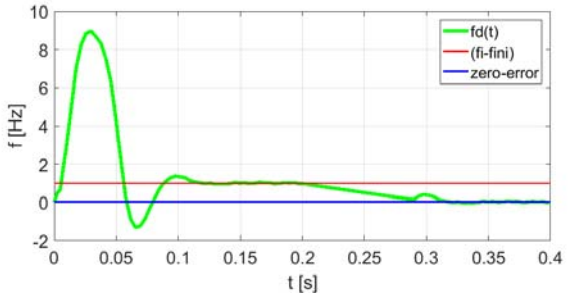

Fig. 5. Frequency detection process

The simulation results shown in Fig. 3 were continued for $t > 0.2$ s till $t = 0.4$ s, with corrected oscillator frequency equal to 50,09734 Hz, put into Gain3 (Fig. 2). After putting new oscillator frequency, the phase remains constant, as it is seen in Fig. 3. The frequency amendment f_d behaves, as shown in Fig. 5. It can be seen, that frequency does not need any change, till 0.4s. The red line in Fig. 5 points the value 1 Hz.

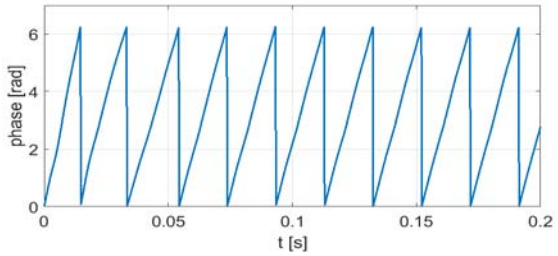

Fig. 6. Running oscillator phase reduced to 2π

The additional proposal can be drawn from the signal available at Out3 (Fig.2). This signal means the resulting phase of the oscillator tracking the grid voltage. This phase reduced to 2π i is shown in Fig. 6.

This waveform points the division of the whole control process into time sections, equal to the actual value of the detected voltage period. The knowledge of these beginnings makes possible to synchronize the process.

The additional drawing shown in Fig. 7 can facilitate the explanation.

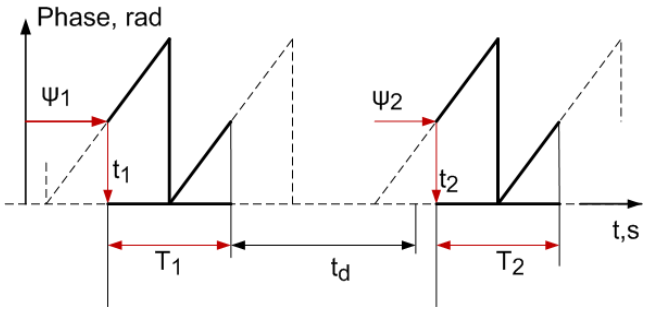

Fig. 7. Window synchronization

Two windows with periods T_1 and T_2 are shown. The first window starts at t_1, this beginning instance results from the crossing initial phase ψ_1 (red arrow) and running phase (dotted triangle) , both available from PLL. Period T_1 is also available at instance t_1. These two parameters determine window location and length. DFT transform is computed from the grid voltage probes belonged to this window. Operations demanded by the algorithm needs time, which is denoted in Fig. 7 as t_d . After this delay next window starts at t_2 with $\psi_2 = \psi_1$. This process can be observed at the simulation waveforms shown in Fig. 8.

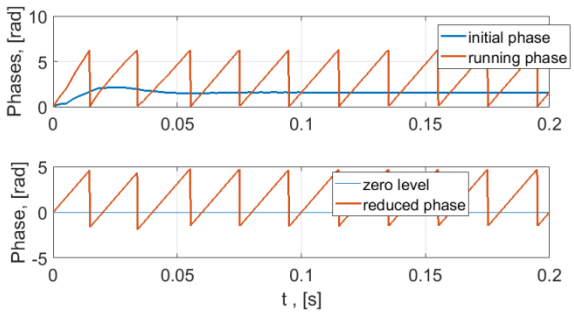

Fig. 8. Window synchronization-simulation waveforms.

The waveforms were obtained in PLL model shown in Fig.2. The source representing grid voltage was put as

(4) $$u_i(t) = 2\sin(2\pi 50t + \pi/2) + 0.2\sin(2\pi 250t + \pi/2)$$

The source voltage contains fundamental harmonic of 50 Hz and fifth harmonic. The upper picture in Fig. 8 shows two waveforms: running phase reduced to 2π and initial phase. The windows (periods) start at instants, when running phase is equal to initial phase. These instants are depicted in lower picture (Fig. 8).

Discreet Fourier Transform (DFT)

For good harmonics evaluation with the DFT the coherent signal processing is required which needs the signal window length and phase synchronization with slowly fluctuating, close to 50 Hz, power signals. Hence, the sequenced windows are time delayed, but have to start at the same phases. The process of the windowing is illustrated in Fig. 9.

Two parallel, phase and time axes are depicted. The phase and time scale result from the voltage data given in (3). The point of the phase zero crossing determines the window starting point. The known period determines its length. The second window is naturally delayed but, but it should have the same phase edges, as shown in Fig. 9.

For example, FFT is applied to the sine wave source put in the SIMULINK model (Fig. 2) representing grid voltage given in (3). This transform is applied for two windows marked in Fig.9. The results are as follows

Window 1: $abs(U_1)=1.9999, angle(U_1)=0.0000$

$abs(U_5)=0.1871, angle(U_5)=-1.5708$

Window 2: $abs(U_1)=1.9997, angle(U_1)=0.0000$

$abs(U_5)=0.1866, angle(U_5)=-1.5773$

where, *angle* means the matlab phase of FFT complex number. We can see, that for properly synchronized windows the FFT results remained unchanged, since the time function was the same within two processed windows.

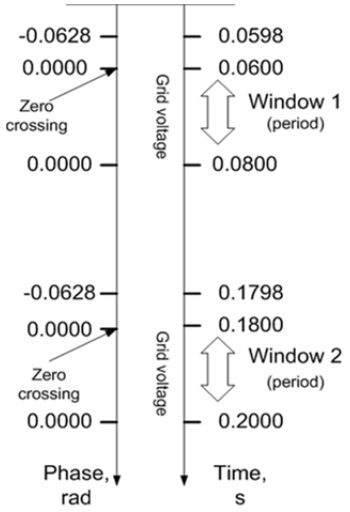

Fig. 9. Window synchronization-grid voltage processed

If the voltage period remains unchanging within longer time duration, then the length of DFT window also remains unchanging and sliding DFT has its advantages.

The sliding DFT (SDFT) algorithm performs an *M*-point DFT on time samples within a sliding window [14]. The *n*th harmonic of *M*-point DFT is defined by

$$X(n)=\sum_{m=0}^{M-1} x(m)e^{-j2\pi mn/M} \tag{5}$$

The frequency–domain index n is an integer in the range $0 \le n \le M-1$. The principle used for SDFT is known as the DFT shifting theorem. We express this process by

$$S_n(m)=S_n(m-1)e^{j2\pi n/M}-x(m-M)+x(m) \tag{6}$$

where bin $S_n(m)=x(m)e^{-j2\pi mn/M}$ is the new spectral component, $S_n(m-1)$ is the previous spectral component. The subscript *n* reminds, that the spectra are those associated with the *n*th DFT bin.

If the processed voltage is periodical and the window is equal to the period, then $x(m-M)=x(m)$ and $|S_n(m)|=|S_n(m-1)|$. Harmonic amplitudes remain unchanged, only phases are shifted by $2\pi n/M$. Sliding DFT needs to have unchanging window *M* within process given (5). This restriction is important for considered application.

Iterative algorithm

The presented computations are concentrated on periodical state of the system under sinusoidal excitation. Time function of voltage $u(t)$ is transformed to the set of harmonics $U(\omega_n)$ for chosen harmonic ranks $n=2,3,...,N$.

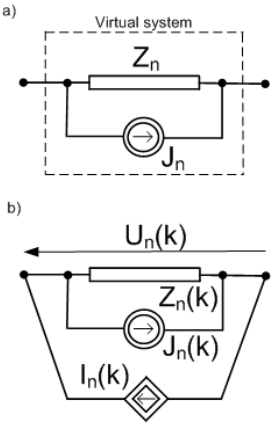

Fig. 10. State observer

The accuracy of harmonic computation is essential for the presented method. In order to obtain sufficient precision DFT, window size should be chosen close to voltage period. During the iteration process, the system is stimulated with the compensator current and satisfactory steady state must be reached and detected.

The essential for proposed method is the block named system state observer (frequency model) (Fig. 10). This model is composed of the set of *N* virtual circuits [9,10]. Each *n*-th cell (component) is associated with *n*-th harmonic and it is responsible for generation of *n*-th harmonic $i_n(t)$. The parallel connection of two elements J_n and Z_n forms the circuit shown in Fig. 10a. Current source J_n can be treated as the phasor representing current harmonic generated in nonlinear system (grid). Harmonic impedance Z_n means the transfer function between compensator current as input and the system voltage as output for the *n*-th harmonic.

In the *k*-th step, while the iteration process, this phasor and impedance take the complex values $J_n(k)$ and $Z_n(k)$. The pair J_n and Z_n can be interpreted as a describing function , known in control theory of nonlinear systems [16]. Two measured signals, system voltage U_n and compensator current I_n, cooperate with the pair J_n and Z_n ,while iterative process is performed. At *k*-th iterative step, these four complex numbers are denoted as $U_n(k)$, $I_n(k)$, $Z_n(k)$, $J_n(k)$ as shown in Fig. 10b. The circuit shown in Fig. 10b leads to the set of equations having the unique solution. These equations and solutions constitute the base for the algorithm presented below.

Step 1.

The virtual system parameters $Z_n(1)$, $J_n(1)$ *and compensator current* $I_n(2)$ *for step 2 are computed.*

Measure voltage $U_n(0)$ for zero compensator current $I_n(0)=0$.

For circuit in Fig.10b

$$U_n(0)=-Z_n(1)J_n(1) \tag{7}$$

Measure the voltage $U_n(1)$ for optional chosen nonzero compensator current $I_n(1)$

For circuit in Fig. 10b

(8) $$U_n(1) = -Z_n(1)J_n(1) + Z_n(1)I_n(1)$$

From (6) and (7) is obtained

(9) $$Z_n(1) = \frac{U_n(1) - U_n(0)}{I_n(1)}$$

and

(10) $$J_n(1) = -\frac{U_n(0)}{Z_n(1)}$$

For step 2

(11) $$I_n(2) = J_n(1)$$

Equation (5) can be explained as follows. The desired voltage in the next step should be zero, $U_n(2) = 0$. For the estimated system parameters (8) and (9) , it means that the following equation should be fulfilled

(12) $$0 = -Z_n(1)J_n(1) + Z_n(1)I_n(2)$$

Hence, equation (8) is proposed.

Step 2.

The virtual system parameters $Z_n(2)$, $J_n(2)$ *and compensator current* $I_n(3)$ *for step 3 are computed.*

Measure voltage $U_n(2)$ for compensator current $I_n(2)$ given in (10). Taking in consideration (10), for circuit in Fig. 10b, we obtain equations similar as (8) to (10)

(13) $$Z_n(2) = \frac{U_n(2) - U_n(0)}{J_n(1)}$$

and

(14) $$J_n(2) = -\frac{U_n(0)}{Z_n(2)}$$

(15) $$I_n(3) = J_n(2)$$

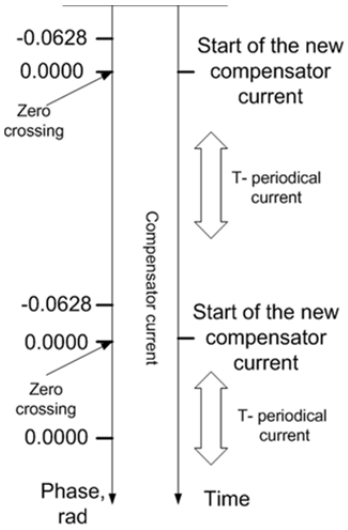

Fig. 11. Synchronization of compensator current intervals

Formulae (11) to (13) can be generalized for *k*-th step.

(16) $$Z_n(k) = \frac{U_n(k) - U_n(0)}{J_n(k-1)}$$

(17) $$J_n(k) = -\frac{U_n(0)}{Z_n(k)}$$

(18) $$I_n(k+1) = J_n(k)$$

The algorithm should be executed for *k=1,…,K*, where index *K* should be chosen in the proper stop criterion, for example taking $|U_n(K)| < U_{\max}$, for *n*=2,…,*N*.

The algorithm given in equations (14)-(16) for single harmonic can be simultaneously performed for all chosen harmonics. The each iteration step should be synchronized with the initial phase appointed by PLL. Fig. 11 illustrates this relation.

DC/AC inverter

Voltage source – current source

A shunt compensator operates as a current source controlled by a grid voltage waveform. This current source is realized as standard DC/AC voltage inverter with the additional inductor connected in series, as shown in Fig. 12.

The *dc* side of the converter is connected to the capacitor *C* with voltage U_{dc}. We assume that capacitor is charged and its voltage is maintained on a proper level, higher than the peak value of the voltage $u_{ac}(t)$ at the *ac* inverter side . The inverter should generate the average voltage waveform $u_{ac}(t)$. This waveform results from the wanted impensator current obtained from the iterative algorithm. It is seen in Fig. 12, that the voltage $u_{ac}(t)$ is equal to the sum of the grid voltage $u(t)$ and the voltage drop on the inductance *L*. This voltage drop follows from the current waveform obtained in the iterative process. The iterative process is performed in the frequency domain. The voltages and currents are expressed in the form of Fourier series. The additional drawing shown as Fig. 13 facilitates us to compute the voltage drop and the wanted voltage at the *ac* inverter side. As the result of the iterative algorithm, the set of complex harmonic amplitudes I_n for $n = 2,3,...,N$ has been obtained.

The circuit for these current phasors is shown in Fig. 13. For this circuit, we have

(19) $$Z_{Ln} = R_L + jn\omega L$$

(20) $$U_{acn} = U_n + Z_{Ln}I_n$$

(21) $$u_{ac}(t) = \frac{1}{2}\sum_{n=-N}^{N} U_{acn}e^{jn\omega t}$$

where $U_{ac(-n)} = U'_{acn}$ conjugate complex value, and the sum includes index $n = 1$, but $n \neq 0$.

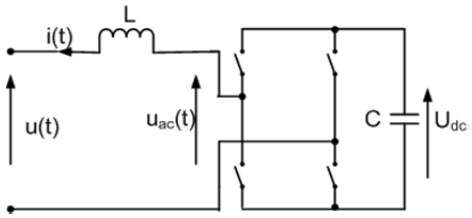

Fig.12. Current source realization , DC/AC bipolar converter

Voltage $u_{ac}(t)$ should be generated by the proper PWM converter control. When iterative method is applied, the control signal should be imposed for whole forward period, and the process is distributed within the sequence of periods.

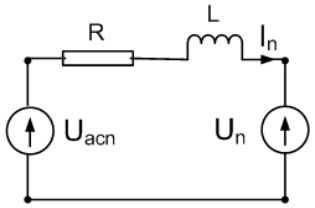

Fig.13. Impedance and voltage drop for *n*-th harmonic

The DC/AC inverter (Fig. 12) together with the series inductance *L* generates desired current for each step of the iterative algorithm for the ordered set of the current complex amplitudes I_n.

Power angle δ, capacitor voltage control

The iterative control performed in the frequency domain enables one to use the fundamental current harmonic to control the exchange the energy between the grid and the capacitor. The control of the fundamental harmonic voltage generated by the inverter enables one to regulate the power flow between the inverter and grid. This energy exchange can be realized by the angle control between the phasors of the fundamental harmonics of the grid and inverter voltages. This angle δ is known as a power angle.

It was assumed in (20), that inverter generates the voltage containing the fundamental harmonic equal to this observed in the grid $U_{ac1} = U_1$. It means that the amplitudes and phases of these voltages for $n = 1$ are equal and no current for this harmonic is injected from the inverter to the grid. However, it is possible to use the fundamental harmonic for the power flow control. It is known, that this power depends on the angle between voltages.

Let's consider two sinusoidal voltage sources connected as shown in Fig.13. The inductor resistance is omitted here for easier explanations. Assume that U_1 and U_{ac1} denote the complex amplitudes of the first harmonic of the grid voltage and the inverter voltage, respectively. Let $U_1 = |U_1|$ and $U_{ac1} = |U_{ac1}|e^{j\delta}$. Angle δ determines the power P_1 flowing between the sources. Let

$$I_1 = I_{1a} + jI_{1r} \tag{22}$$

Applying the voltage Kirchhoff law, for the circuit shown in Fig. 13, we obtain

$$I_{1a} = \frac{|U_{ac1}|}{X_1}\sin\delta \tag{23}$$

$$I_{1r} = \frac{|U_1| - |U_{ac1}|\cos\delta}{X_1} \tag{24}$$

where reactance $X_1 = \omega_1 L$.

Let's concentrate on the active (average) power P_1 exchanged between converter and the grid on fundamental frequency , $n = 1$. For this purpose, it is possible to restrict the consideration and assume that $U_{ac1} = U_1$. This power

$$P_1 = \frac{1}{2}\frac{|U_1|^2 \sin\delta}{X_1} \tag{25}$$

can be availed in order to maintain the inverter capacitor voltage.

The reactive power resulting from the reactive component of the fundamental harmonic current can be treated as a tool for a grid voltage control. This problem is beyond the scope of this paper.

The influence of the power angle on the capacitor voltage of the inverter is illustrated in the next section.

Influence of the power angle on the capacitor voltage

The influence of the power angle on the capacitor voltage was investigated with the use of the PLECS model of the inverter shown in Fig. 14.

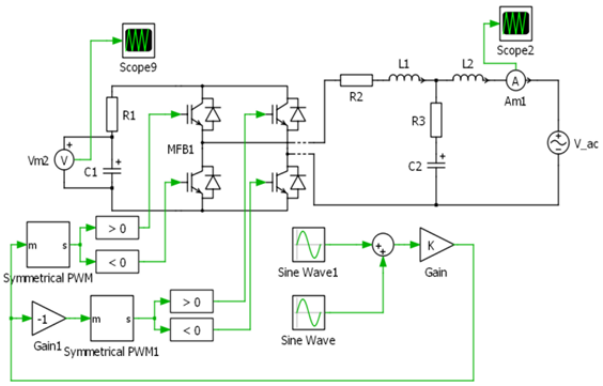

Fig. 14. PLECS model of the PWM inverter

The PLECS model consists of PWM converter, dc voltage capacitor , sine wave blocks generating input signals, voltage source representing grid voltage, inductance connecting inverter with the grid and the additional capacitor reducing current ripples.

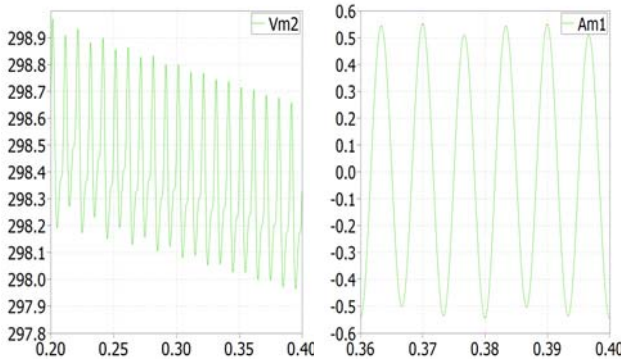

Fig. 15. Simulation waveforms for $\delta = 0$ a) capacitor voltage, b) compensator current (third harmonic)

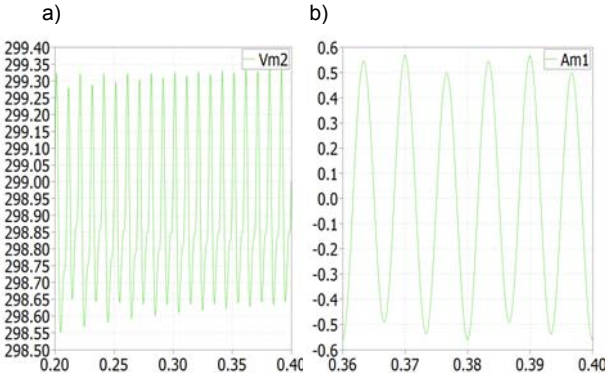

Fig. 16. Simulation waveforms for $\delta = -0.00007$ a) capacitor voltage, b) compensator current (third harmonic)

The waveforms show the capacitor voltage and the current injecting into the grid. The waveforms are shown in Figs. 15 and 16 for two values of the power angle δ.

The parameters of the inverter model are as follows. The carrier frequency of the converter $f_{conv} = 5kHz$, input

signal $s_{in} = 200\sin(2\pi 50t + \frac{\pi}{4} + \delta) + 50\sin(2\pi 150t)$, gain K = 1/300, grid voltage $u_g = 200\sin(2\pi 50t + \frac{\pi}{4})V$, capacitor of the dc voltage $C_1 = 1000\mu F$, $u_{C1}(0) = 300V$, $R_1 = 1\Omega$ inductance transforming the voltage into the current and ripple filter parameters $L_1 = 95mH$, $L_1 = 5mH$, $C_2 = 5mH$, $R_2 = R_3 = 1\Omega$.

Numerical example

In order to illustrate the iterative process the resistive circuit shown in Fig. 17 was simulated. The results have been obtained for the following values of the circuit parameters: $e(t) = E\sin(2\pi f_i + \psi_i)$ with $E = 300V$, $f_i = 50Hz$, $\psi_i = \pi/2$, resistances $R_1 = 25\Omega$, $R_2 = 5\Omega$, nonlinear resistance $u_n = r_n i_n^5$, where $r_n = 50\frac{V}{A^5}$.

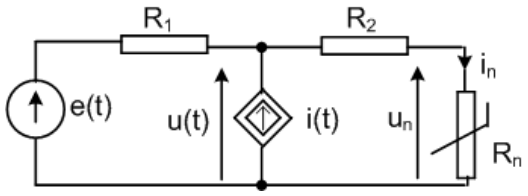

Fig. 17. Circuit for the considered example

The controlled current source shown in Fig. 16 represents the compensator. The current waveform $i(t)$ is getting out from the voltage waveform $u(t)$ in the iterative process described below.

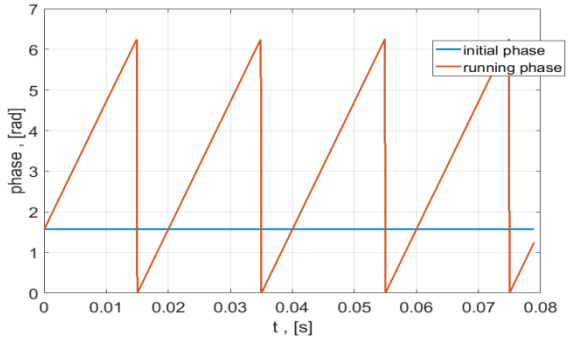

Fig. 18. Crossing of the phases shows windows beginnings

As it was explained in the previous sections the size of FFT window should be equal to the voltage period and the initial phase of the each window should be stable (the same) for all iterations. For the simplified illustration the numerical simulation is done without the PLL. Fig. 18 shows phases of the voltage source $e(t)$. The red line shows the running $(2\pi f_i + \psi_i)$ and the blue line shows the initial phase ψ_i. The crossings of these two lines appoint the time set of window beginnings. For assumed frequency $f_i = 50Hz$ this set is 0.00, 0.02, 0.04, 0.6 ,… seconds.

The iterative algorithm applied to the circuit shown in Fig. 17 gives the numerical results presented in Table 1. The columns of this table contain the numerical results of the iterative algorithm presented in the preceding section. The first column points the windows whose bounds are explained above. The second columns contains the harmonic order associated with f the complex values shown

In the next columns.

The algorithm starts from *step 1*, the voltage is measured, when compensator current is zero, this measurement is realized within time window 1. The results of FFT transform is placed in Table 1 while the first window 1 lasts, although it should be placed in the in the next time window, because of delay needed for computation.

Table 1. Iterative process

Wind. Nr.	Harm. Nr.	U V	Z Ω	J A	I A
1	1	248.4-72.21i	-	-	-
1	3	5.928-6.866i	-	-	-
1	5	-0.771+4.041i	-	-	-
1	7	-0.845-1.624i	-	-	-
2	1	248.0-72.18i	-	-	-
2	3	2.427-3.274i	-	-	-0.200+0.000i
2	5	-0.806+1.929i	-	-	0.100+0.000i
2	7	-0.382+0.488i	-	-	-0.100+0.000i
3	1	-	-	-	-
3	3	-	17.50-17.95i	-0.361+0.022i	-0.200+0.000i
3	5	-	-0.347-21.11i	0.190+0.039i	0.100+0.000i
3	7	-	-4.63-21.13i	-0.081+0.022i	-0.100+0.000i
4	1	248.2-72.17i	-	-	-
4	3	0.598-0.129i	-	-	-0.361+0.022i
4	5	0.787-0.094i	-	-	0.190+0.039i
4	7	0.193-0.298i	-	-	-0.081+0.021i

Such delays are omitted also in the table illustration of the next steps. The next window is assigned for the measurement and voltage processing when the compensator current has nonzero freely chosen waveform. In the similar way the next two algorithm steps are presented in the table. The algorithm closes in three iteration steps. The final results are shown in Fig. 19.

We observe three patterns of the compensator current. In the first step the current is null. The second interval is stretched on two windows (0.02,0.039) and (0.04,0.059). Within this interval the compensator current is tied to the complex numbers obtained from the algorithm and placed in window 3 (Table 1).

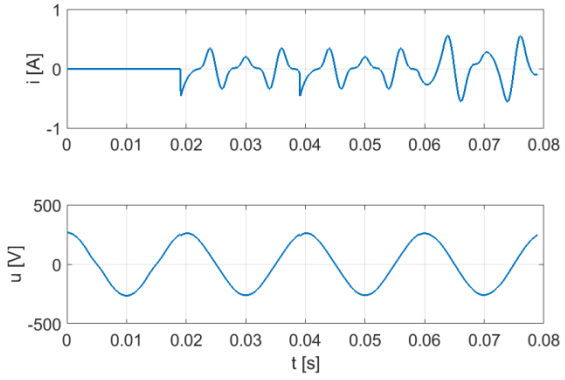

Fig. 19. Compensator current (upper waveform) and improved voltage (lower waveform) within compensating process

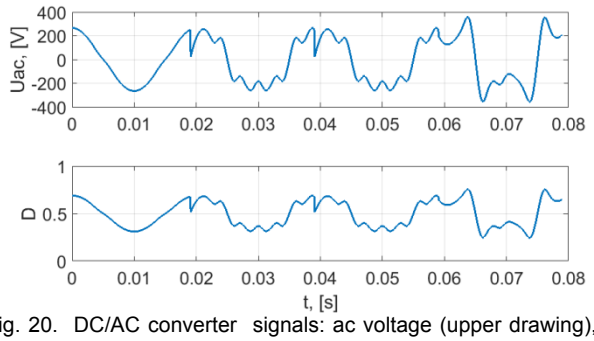

Fig. 20. DC/AC converter signals: ac voltage (upper drawing), b) duty ratio (lower drawing)

The voltage shown in lower waveform is close to sinusoid, as the harmonics are small in the comparison with the fundamental harmonic.

The DC/AC inverter (Fig. 12) can generate the current shown in Fig. 18, if the duty ratio of the control signal follows the lower waveform shown in Fig. 19. Such duty ratio function was obtained for $U_{dc} = 700V$.

The voltage at the alternating side of the converter is shown in the upper drawing of Fig. 20. This waveform was calculated according to equations (17) –(19) for $L = 0.25H$ and $R_L = 0$.

The compensating current derived by the iterative algorithm should be generated using techniques differing from this achieved for commonly used active power filters. The iterative control has its specific, and differs from the control operating in time domain.

Conclusions

The iterative control needs few steps to reach its target, so the time response of the method is in the range of few hundreds ms. Each iterative step must be stretched on at least two windows, each a fundamental period long. One window means one measuring unit for DFT operation, even if the sliding DFT is applied each window must be synchronized with the fixed initial phase and have to be exactly one period long. Such requirements lead to the specific kind of control stretched over the necessary time interval. Such the control process is proposed in the paper and is illustrated in Fig. 9, Fig. 11 and Table 1.

The accuracy of harmonic computation is essential for the presented method. In order to obtain sufficient precision the window of DFT should be chosen close to voltage period. The window beginnings should be precisely synchronized. The synchronization errors have influence on compensator current harmonic phases. The higher harmonics are more sensitive on the synchronization errors. The satisfactory steady state must be reached and detected. During the iteration process, the system is stimulated with compensator current. Within the compensating process the system parameters are continuously estimated .

In this paper the synchronization is presented on the base of PLL techniques. For frequency iterative control this synchronization techniques can be modified. If follows from this reason that Fourier series must be computed for the iteration process. Having Fourier representation, the running phase is available as the phase of voltage fundamental harmonic.

***Authors**: prof. dr hab. inż. Kazimierz Mikołajuk, dr inż. Zbigniew Staroszczyk, mgr inż. Andrzej Toboła Politechnika Warszawska, Instytut Elektrotechniki Teoretycznej i Systemów Informacyjno Pomiarowych, ul. Koszykowa 75, 00-669 Warszawa, E-mail: K.Mikolajuk@iem.pw.edu.pl Z.Staroszczyk@iem.pw.edu.pl, A.Tobola@iem.pw.edu.pl*

REFERENCES

[1] S. D'Arco, M. Ochoa-Gimenez, L. P. Piegari, P. Tricoli, "Harmonics and Interharmonics Compensation With Active Front-End Converters Based Only on Local Voltage Measurements", Ieee Trans. Ind. Electron. , Vol. 64, pp. 796-805, No. 1, Jan. 2017

[2] H. Akagi, "Control Strategy and Side Selection of a Shunt Active Filter for Damping of Harmonic Propagation in Power Distribution Systems" , *IEEE Tarans. Power Delivwery*, Vol. 12, January 1997, pp. 354-362

[3] C. Mingfeng, Lei Wanjun, N. Cheng, W. Huajia, W. Yue, A novel contrl algprithm of shunt active power filter based on voltage detection, 2016 China Int. Conf. on Electricity Distribution, Xi'an, 10- 13 Aug., 2016

[4] Czarnecki L. S., Staroszczyk Z.: "On-line measurement of equivalent parameters for harmonic frequencies of a power distribution system and load", *IEEE Trans. on Instrumentation and Measurements*, vol. 45, No. 2, April 1996. pp. 467-472

[5] Staroszczyk Z.: "Wide frequency band power system linear and linear time variant model identification – signal processing problems". *11th IMEKO TC-4 Symposium on Trends in Electrical Measurements and Instrumentation*, 13-14 September, 2001, Lisbon, Portugal

[6] D. Menniti, A. Burgio, N. Sorrentino, A. Pinnarelli, Implementation of the shunt harmonic voltages compensation approach, *ELSEVIER Electric Power Systems Research* 81 (2011) 798-804

[7] X. Wang, F. Blaabjerg, Z. Chen, "Synthesis of Variable Harmonic Impedance in Inverter-Interfaced Distributed Generation Unit for Harmonic Damping Throught a Distribution Network", *IEEE Trans. Ind. Applications*, Vol. 48, No 4 2012, pp. 1407-1417

[8] J. He, Y. W. Li, M. Shirajum, "A Flexible Harmonic Control Approach Through Voltage-Controlled DG-Grid Interfacing Converter", *IEEE Trans. Ind. Electronics*, Vol.. 59, No. 1, January 2012, pp. 444-455

[9] K. Mikołajuk, A. Toboła, "Voltage harmonic damping with the framework based on Kalman approach", vol. 93, No. 10, pp. 123-126

[10] K. Mikołajuk, A. Toboła, "Reference Signal Detection for Voltage Harmonic Damping in Three-Phase Systems ", CPEE 18th Int. Conf. Kutna Hora , Czech Re. 11-13 sept. 2017

[11] S. Golestan, J. M. Guerrero, J. C. Vasquez, "Single-Phase PLLs: A Review of Recent Advances", IEEE Trans. Power Electron., vol.32, No. 12, pp.9013-9030, Dec. 2017

[12] D. Jovcic, "Phase Locked Loop Systems for FACTS", IEEE Trans. Powe Electron., vol. 18, No. 3, pp. 1116-1124, Aug. 2003

[13] M. Cichowlas, M. Malinowski, M. P. Kaźmierkowski, D. L. Sobczuk, P. Rodriguez, J. Pou, „Active Filtering Function of Three-Phase PWM Boost Rectifier Under Different Line Conditions", IEEE Trans. Ind. Electron., Vol. 52, No. 2, pp. 410-419, Apr. 2005

[14] E. Jacobsen, R. Lyons, "The Sliding DFT", IEEE SIGNAL PROCESSING MAGAZINE,, MARCH 2003, pp. 74-80

[15] K. Sozański, Digital Signal Processing In Power Electronics Control Circuits, Springer, 2017

[16] J. E. Gibson, Nonlinear automatic control, Mc Graw-Hill, 1963

[17] R. Strzelecki, H. Supronowicz, Współczynnik mocy w systemach zasilania prądu przemiennego I metody jego poprawy. Oficyna Wydawnicza Politechniki Warszawskiej, 2000

[18] Pasko M., Adrikowski T., Białoń T., Buła D., Krzysztof Dębowski, Grabowski D., Lewandowski M., Lewicki A., Maciążek M., Niestrój R., Sztymelski K., *Zastosowanie w elektrotechnice metod analizy i syntezy układów do poprawy jakości energii i sterowania*, w: XXXIX Konferencja z Podstaw Elektrotechniki i Teorii Obwodów. 39th Conference on Fundamentals of Electrotechnics and Circuit Theory. SPETO 2016, Gliwice - Ustroń, 18-21.05.2016, s. 3-3l.