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Regulation of Current Harmonics in Grid with Dead-beat Controlled Shunt Active Power Filter

Abstract. *Hardware implementation of Shunt Active Power Filter (SAPF) to regulate harmonics in the grid current is presented in this work. Dead-beat controller is employed to regulate the harmonics injected by SAPF using Spartan-6 FPGA processor. The effectiveness of the control strategy is tested under different operating conditions through MATLAB simulations and experimental approach to reduce the grid current harmonics and to meet the IEEE519:2014 recommendations for harmonic regulation guidelines, at the Point-of-Common-Coupling(PCC).*

Streszczenie. *Zaprezentowano bocznikowy filtr aktywny zaprojektowany do redukcji harmonicznych w sieci. Sterownik typu dead-beat jest zastosowany wstrzykiwania prądu z wykorzystaniem procesora Spartan-6 FPGA. Zbadano efektywność sterownia w różnych warunkach pracy przy spełnieniu rekomendacji IEEE519:2014.* ***(Aktywny filtr bocznikowy wykorzystujący sterownik typu dead-beat do redukcji harmonicznych)***

Keywords: Shunt active power filter, dead-beat control, harmonic compensation, PCC, THD, FPGA
Słowa kluczowe: bocznikowy filtr aktywny, redukcja harmonicznych, sterownik dead-beat

Introduction

The load on the existing power system network keeps on changing in both magnitude and v-i characteristics. The dynamic nature of the load magnitude leads to fluctuations in the system voltage. These fluctuations in the voltage magnitude are characterized based on the voltage magnitude variation and its duration viz., sag, swell, under voltage, over voltage etc.

Now-a-days, the magnitudes of nonlinear loads have increased due to the advancements in the field of semiconductor technology and power converters. Due to this the electric power network is subjected to various issues like harmonics, distortion, increased losses, increased temperature rise in the connected equipment and transmission line. This results in reduced life time of the equipment, poor efficiency, frequent failure, malfunctioning of sensitive load equipment, life-saving equipment and various process in the industries etc. These nonlinear loads, draw non-sinusoidal current from the utility grid through transmission and distribution network. These non-sinusoidal currents flowing in the AC system develops a non-sinusoidal voltage drop across the transmission line reactance. The net voltage at the load terminals is sinusoidal voltage from the utility grid minus non-sinusoidal drop across the transmission line reactance. Thus, voltage distortion is introduced into the power system. This distorted voltage when applied to a linear load, it draws non-sinusoidal current from the supply. Hence the amount of harmonics injected into the power system is increased [1].

Several strategies have been formulated to limit the harmonic voltages/currents in the power system network so as to increase its reliability. Initially properly designed passive filters are installed in the system so as to limit the harmonic propagation in the power network at suitable locations. But due to development of sophisticated electronic devices and equipment which draws nonlinear current from the supply mains, the nature of harmonic currents is unpredictable. Hence the provision of previously installed passive filters can no longer work properly to limit the harmonics. Also, other problems associated with passive filters like increased size, cost, inflexible in operation, and resonance at harmonic frequencies limits the application of passive filters.

In order to provide flexibility in harmonic control and due to the development of high-speed computers/controllers and the development of fast switching power devices, control of harmonics with greater flexibility and dynamic control is made possible. Also, developments in the field of sensors and signal processing techniques, more versatile controllers evolved. Hence, active power filters are developed and applied in several applications where power rating ranges from few watts to several Megawatt [2] - [5].

In this paper, the necessity of harmonic filtering, its type and functionality in regulating harmonic levels in the power network is carried out. The performance of the controllers, its implementation and requirements are stated based on the realization in simulation environment. A prototype convincing the theoretical aspect was developed and tested in the laboratory environment. The importance of the work is vital in this time so as to move on to the new generation of control strategies with reduced sensors and signal conditioning circuits.

The organization of the paper is as follows: Section1 gives overview about the harmonic generation and compensation necessity pertaining to power system in various scale. the principle of current harmonic compensation using SAPF. The principle of harmonic extraction is discussed in section 2 giving the user, a guideline to select the compensation power under different operating environment. The theory of compensating current generation is discussed in section 3. MATLAB simulations and results were presented in section 4 and section 5 demonstrates the hardware implementation of the SAPF and its control with results. In section6, the results were analysed and discussed.

Principle of Harmonic Compensation

The principle of current compensation is shown in Fig.1. At PCC, Kirchhoff's law yields $i_s = i_L + i_f$. The current drawn by the nonlinear load is non-sinusoidal. The load current can be resolved using Fourier series to sum of infinite sinusoids whose frequencies are integer multiples of supply frequency. The instantaneous load current (i_L) is the sum of instantaneous fundamental component(i_{L1}) and instantaneous harmonic components(i_{Lh}). If the filter current is equal to the harmonic component of the load current, then the instantaneous source current(i_s) is equal to the instantaneous fundamental component of load current.

The compensation of i_{Lh} results in harmonic free source current at fixed power factor. If unity power factor is desired, then along with i_{Lh}, component corresponding to reactive power must also supplied by the compensator. The compensation strategies with *pq-theory* employed is constant instantaneous power control strategy ensuring unity power factor.

SAPF is used as shunt compensator to compensate for current harmonics. SAPF is installed at PCC in power network where the system parameters are accessible by both utility and the customer.

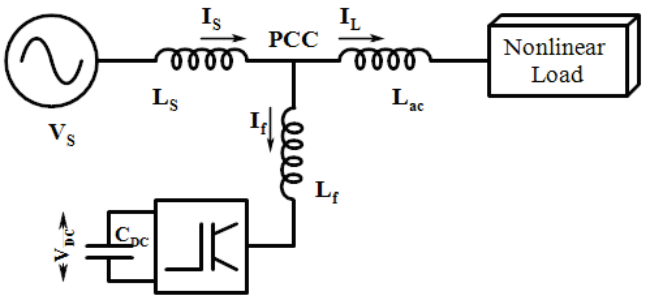


Fig. 1. Principle of harmonic compensation

The power circuit of a typical SAPF is shown in Fig.2. It consists of a voltage source converter (VSC) with capacitor powered DC link, interfacing filter (L_f) and a filter controller. The filter controller plays a vital role in the working of VSC as APF. The filter controller senses the utility voltage and load current continuously. The data acquisition system in the filter controller processes the voltage and current signals to compute the harmonic currents that has to be generated by the VSC. Also, the controller regulates the DC link voltage constant throughout its operation. The computed currents are compared with the actual current output of the filter and passed on to the controller to generate the gating signals for the VSC in order to minimize the tracking error. The VSC upon gating by the filter controller generates the desired harmonic current which is filtered for switching frequency harmonics by a small passive filter provided between the output of VSC and PCC of the utility grid [6],[7]. Harmonics of any order can be compensated by appropriately selecting the compensating powers and generating the current reference. Several strategies are available in literature for the generation of harmonic current references from the distorted voltages and currents.

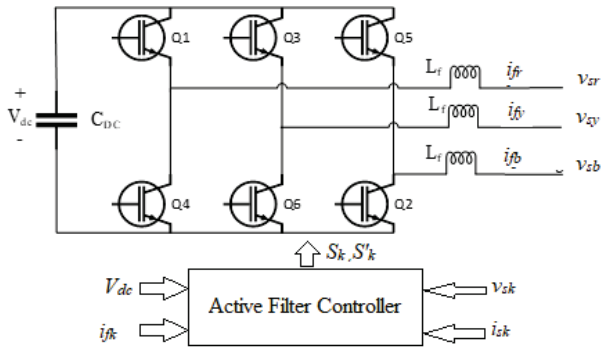


Fig. 2. VSC as shunt active power filter

The current tracking is effected by shunt active filter controller adopting suitable control strategy from literature [8] - [13]. The function of the controller is to minimize the tracking error by its controlling action and to generate appropriate gating signal for the VSC. Based on the error magnitude, the duty ratio of the gating signal is adjusted by the controller. The role of controller is hence vital in these applications.

Computation of Harmonics

Akagi. H [14] developed a new theory for computing instantaneous real and reactive powers in a power system *(pq - theory)*. It is based on Clarke's transformation of instantaneous voltages *(v)* and currents *(i)* in the power system. The transformation is aimed to convert a set of time varying space varying phasors in to two orthogonal components and a zero-sequence component like in symmetrical component transformation. The *pq-theory* is valid for all conditions like the system voltages balanced or unbalanced, distorted or undistorted, transient or in steady-state in three phase system with or without neutral conductor.

Without change in power, the Clarke's transformation of instantaneous voltages and currents are governed by equation (1).

$$\text{(1a)} \qquad \begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} v_r \\ v_y \\ v_b \end{bmatrix}$$

$$\text{(1b)} \qquad \begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = \sqrt{2/3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} i_r \\ i_y \\ i_b \end{bmatrix}$$

The instantaneous real power (p) and reactive power (q)is calculated in the transformed domain as in equation (2).

$$\text{(2a)} \qquad p = v_\alpha i_\alpha + v_\beta i_\beta + v_0 i_0$$

$$\text{(2b)} \qquad q = v_\beta i_\alpha - v_\alpha i_\beta$$

It is observed that the instantaneous powers in (2) comprises of two components namely average and oscillating components as represented in equation (3).

$$\text{(3)} \qquad p = \bar{p} + \tilde{p}; q = \bar{q} + \tilde{q}$$

The components of power include both fundamental and harmonic powers. The average and oscillating components of power are separated from the computed power by a higher order Butterworth low-pass filter with a cut-off frequency around the supply frequency. The compensating currents for the SAPF are computed from equation (3) after separating the average and oscillating components. The currents are calculated as in equation (4).

$$\text{(4)} \qquad \begin{bmatrix} i^*_{c\alpha} \\ i^*_{c\beta} \end{bmatrix} = \frac{1}{\sqrt{{v_\alpha}^2 + {v_\beta}^2}} \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} p^*_c \\ q^*_c \end{bmatrix}$$

The compensation currents calculated using equation (4) cannot be used directly and must be transformed back to the time domain using inverse Clarke's transformation dictated by equation (5).

$$\text{(5)} \qquad \begin{bmatrix} i^*_{cr} \\ i^*_{cy} \\ i^*_{cb} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \sqrt{3}/2 \\ -\frac{1}{2} & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i^*_{c\alpha} \\ i^*_{c\beta} \end{bmatrix}$$

The currents computed using equation (5) is used as the reference current for the SAPF.

Simulation of shunt active power filter

The simulation model of SAPF is developed in MATLAB/Simulink environment. The conditions chosen for simulations are balanced nonlinear load, balanced non-linear load with balanced linear load, unbalanced nonlinear load. The source voltage is assumed to be distortion free throughout the simulation. The complete simulation model of SAPF is shown in Fig. 3. The parameters used for the simulation are listed in Table 1.

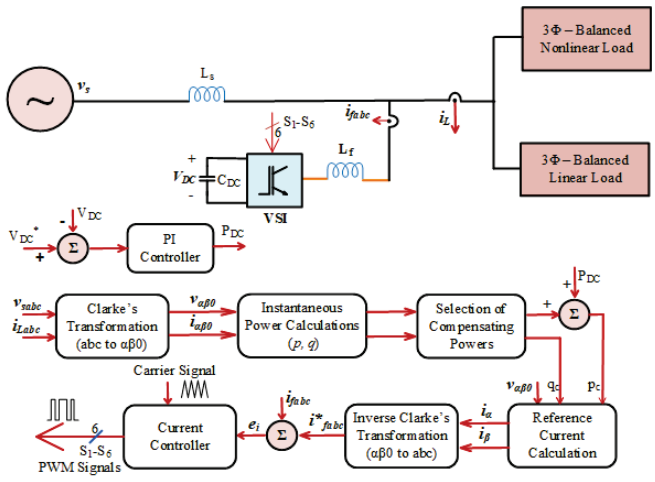


Fig. 3. MATLAB/Simulink implementation of SAPF

Table1: Simulation Parameters of the system under study

Parameter	Values
Source side parameters:	
Source Voltage:	415V, 50 Hz, 3ϕ
Resistance(R_s):	0.1Ω
Inductance (L_s):	5 mH
Load Side Parameters:	
Three Phase diode bridge rectifier:	P = 1 kW; Q = 500 VAr
Single Phase diode bridge rectifier:	P = 1 kW; Q = 500 VAr
Filter Parameters:	
DC link Voltage (V_{DC}):	700 V
DC link Capacitor (C_{DC}):	400 μ F
Interface Inductor (L_f):	5mH

The simulation results include waveforms of the source voltage, source current, injected filter currents, calculated reference currents, dc-link capacitor voltage and percentage harmonic distortion variation in source current are shown in Fig.4. The source voltage is measured with respect to neutral in Fig.4a. At time t=0, the filter remains in 'OFF' state. The capacitor in the dc link is charged through the anti-parallel diodes of VSC switches.

A large source current spike in Fig.4b is due to the capacitor charging. The source current drawn by the load is non-sinusoidal with peak current of 6.9 A and the THD of 22.75%. Initially the filter is 'OFF' and hence the injected current is zero. At t = 0.2s, the filter is turned 'ON' the capacitor voltage is regulated to set reference voltage of 700V, and the filter is injecting harmonic current in quadrature to the load current at PCC. As a result, the source current become sinusoidal with a peak of 7.49A with THD of 3.92% less than the limits specified by IEEE519:2014. The dc-link voltage is regulated by PI-controller whose output is measured as real power required to main the capacitor voltage constant. To emphasis the dynamic operating condition, an additional load is switched 'ON' at t = 0.4s and the corresponding source and injected filter currents are also shown in Fig.4b - 4c. Similarly, at t = 0.6s another single-phase diode bridge rectifier load is turned 'ON' creating unbalance. It is observed that the source current is still maintained by SAPF as balanced sinusoidal. The injected filter currents are shown in Fig.4d and the dc-link voltage in 4e. The compensation is achieved in less than half cycle period of supply voltage.

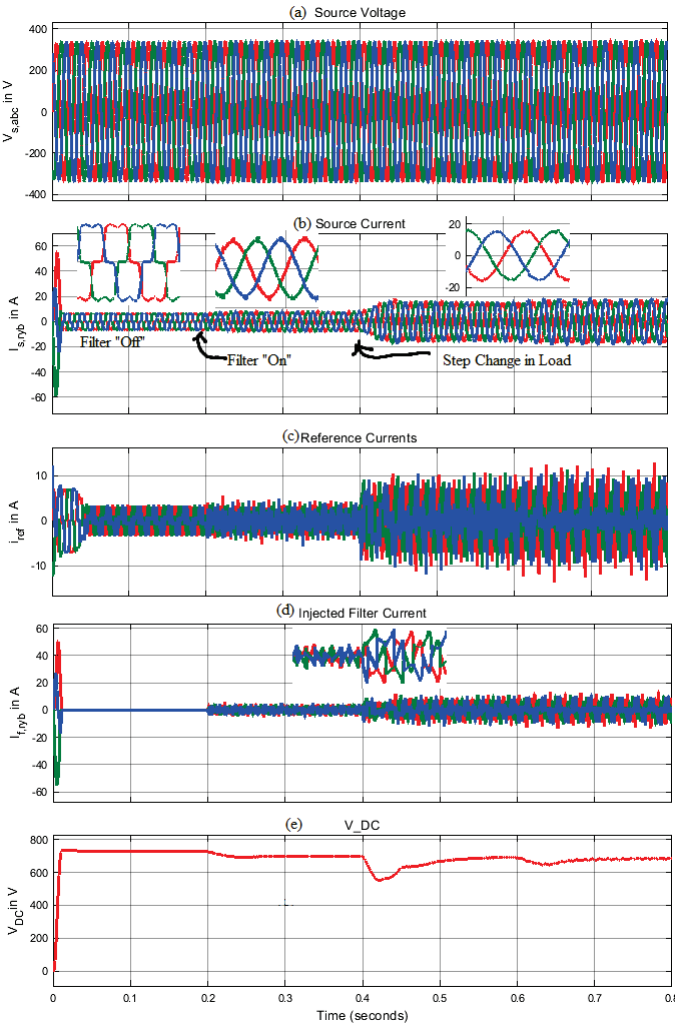


Fig. 4. Simulated waveforms of (a) source voltage, (b) source current, (c)reference filter currents, (d) injected filter current, (e) dc-link capacitor voltage

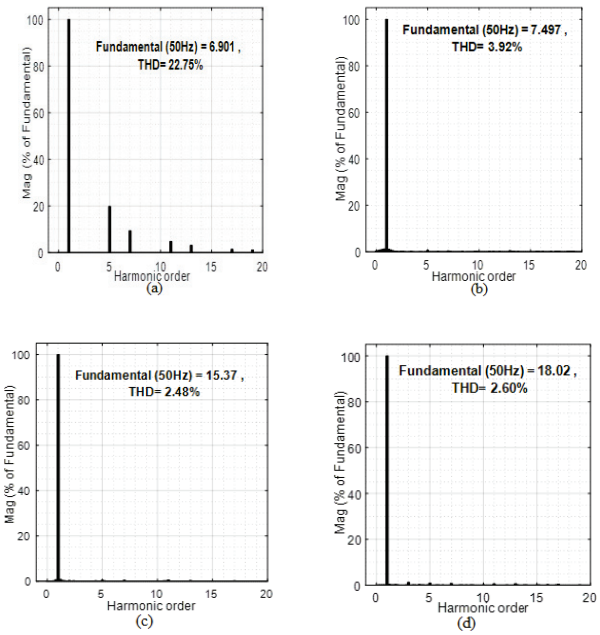


Fig. 5. Harmonic spectrum of source current (a) Before compensation (b) After compensation (c) After step load change (d) After unbalance

The harmonic spectrum of source current computed before and after compensation for different operating conditions is illustrated in Fig.5 . It signifies that the dominant lower order harmonics of 5^{th} and 7^{th}, 11^{th} and 13^{th} order harmonics in the source currents in Fig.5a are eliminated by SAPF. The spectrum of source current in Fig.5b – 5d signifies that these harmonics are suppressed due to the filtering action.

Hardware implementation of SAPF

The proposed control strategy for SAPF was implemented in hardware. The prototype is tested for reduced voltage and power level in the laboratory environment for validating the principle of harmonic compensation. The VSC employs Semikron IGBT Inverter module (SKM300GB126D), gated by IGBT SKHI10/12 driver. The pulses are isolated by means of on-board isolation transformer and has in-built short circuit and overvoltage protection.

Filter controller is implemented with Spartan6 FPGA-XC6slx25t processor. Essential voltage and current sensing circuits with signal conditioning circuits were designed and implemented. FPGA processes the measured source voltages, source current, load current and filter current through its analog input port. The analog input is equipped with bipolar analog-to-digital converter (ADC) to translate the analog signal into digital word to the FPGA processor[15]-[17]. The processor computes the power drawn from the source by the nonlinear load in $\alpha\beta 0$ domain. The dc-link is provided with two split capacitors in series, which enables SAPF to compensate for both three-phase three wire or four wire loads with neutral point clamping. The DC link voltage is monitored using LV25P voltage sensor and is compared with the reference dc-link voltage in order to maintain the dc-link voltage constant. This enables compensation feasible by the SAPF. PI controller regulates the dc-link voltage of VSC constant around set value of 375V. The FPGA processor generates the reference currents according to equation (4). The experimental setup of the SAPF is shown in Fig.6. The detailed specifications of the experimental setup are provided in table 2.

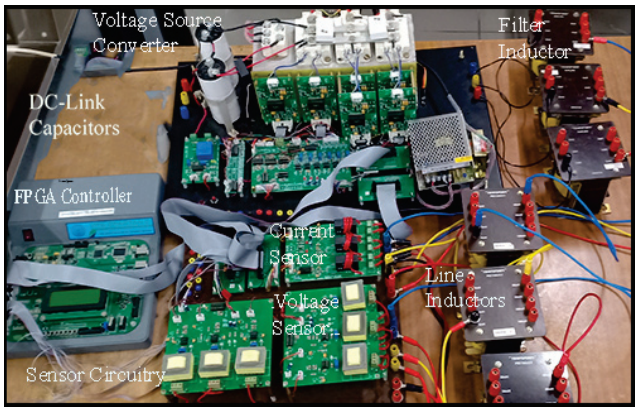


Fig. 6. Experimental setup of SAPF

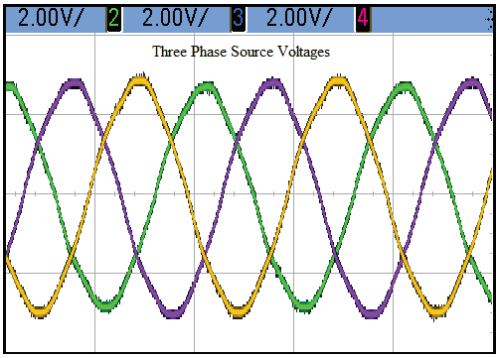
The measurements are taken with Fluke 435B power quality analyser and Agilent MSO7014B 4-channel MSO. The ac line voltages are sensed using potential transformers and current sensors with bipolar output are employed for current measurements. Tektronix current clamps are used for current measurements with Fluke and MSO. The performance of the SAPF was tested for the operating conditions like balanced nonlinear load, balanced nonlinear and linear load, and single phasing operation.

Table2: Parameters of SAPF hardware

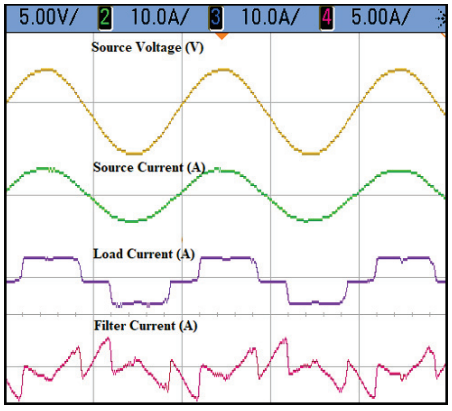
Parameter	Values
Source side parameters:	
Source Voltage:	110V, 50 Hz, 3ϕ
Resistance(R_s):	0.1Ω
Inductance (L_s):	5 mH
Load Side Parameters:	
Three Phase diode bridge rectifier:	2 kW Resistive load
Three Phase linear load:	1 hp Induction Motor
Filter Parameters:	
DC link Voltage (V_{DC}):	375 V
DC link Capacitor (C_{DC}):	400 μ F
Interface Inductor (L_f):	5mH

0.1 Case 1: Balanced nonlinear load

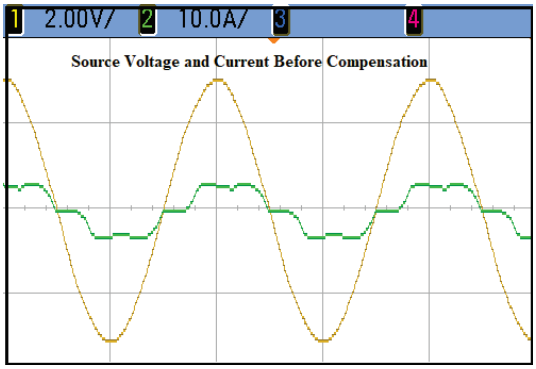
In this case, a three-phase diode bridge rectifier feeding 2 kW resistive load is considered. The supply voltage in the lab environment has a THD of 5.5% at 110V RMS per phase with 3^{rd} and 7^{th} harmonics as significant. The diode bridge current is continuous and the load is shared among all three-phases at the source. The source current is non-sinusoidal with a THD of 25.1%. The dc-link voltage is maintained at 375V. The response of the SAPF, source voltage, source current, load current and filter currents before and after compensation were shown in Fig.7a - 7d measured with MSO. It is observed that the compensation is effective and hence the source current is sinusoidal and in-phase with the source voltage thereby attaining unity power factor operation at the source end. The dynamic response of dc-link voltage is shown in Fig.7e. it shows the variation in dc-link voltage when the filter is switched 'ON', for step increase in load and for step decrease in load. The dc voltage is PI regulated and hence the dynamic response will be much faster.



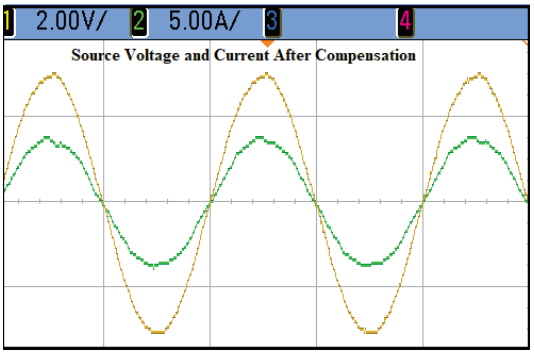
(a)Three phase source voltages



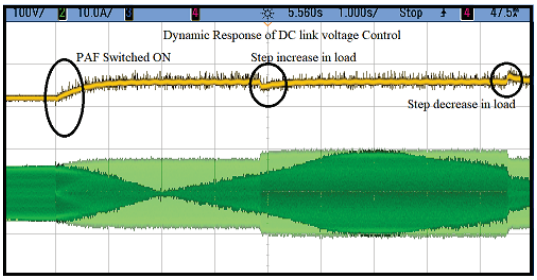
(b)Source voltage, source current, load current, filter current



(c) Source voltage and current in Phase A before compensation



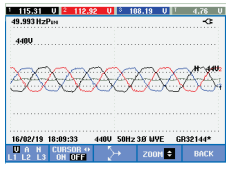
(d) Source voltage and current in phase A after compensation



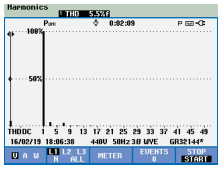
(e) Dynamic response of dc-link controller in SAPF

Fig. 7. Response of SAPF

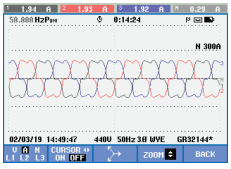
The measurements of current and voltage harmonics, power and power factor are carried out with Fluke 435B power quality analyser. The measurements of power analyser are shown in Fig.8a – 8h measuring the source voltage, current, power, power factor and harmonics. The load current shows an THD of 23.9% with $5^{th}, 7^{th}, 11^{th}$ and 13^{th}order harmonics as significant. After compensation, the net active is increased to 2.2kW at 0.99 power factor (lag) with significant reduction in THD to 3.5%.



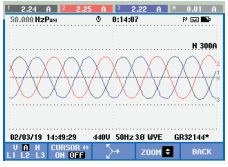
(a) Three Phase Source Voltages



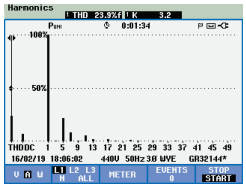
(b) Spectrum of Phase 'r' voltage



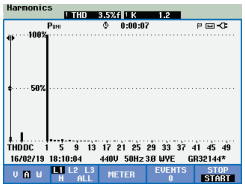
(c) i_s (before compensation)



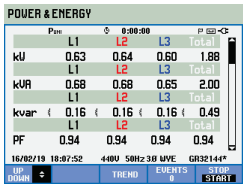
(d) i_s (after compensation)



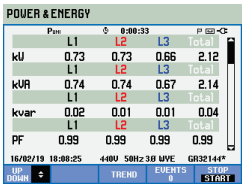
(e) Spectrum of i_s (before compensation)



(f) Spectrum of i_s (after compensation)



(g) Power and Power factor (before compensation)

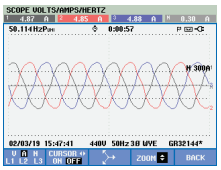


(h) Power and Power factor (after compensation)

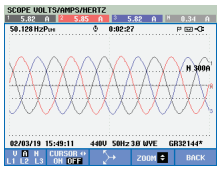
Fig. 8. Case1: Performance of SAPF with balanced nonlinear loads

0.2 Balanced nonlinear and linear loads

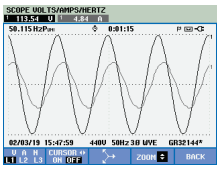
In this case, a three-phase 1hp induction motor is connected in parallel to the three-phase bridge rectifier load. The source current harmonics are now limited to 6.8% and the currents are sinusoidal as in Fig.9c. But the power factor at the source is reduced to 0.79 lag due to the induction motor. In this case, the SAPF is now forced to deliver the reactive power so as to improve the power factor at the source. The effect of diode bridge rectifier is partially offset by the induction motor load. The measurements from power analyser are shown in Fig.9a – 9h.



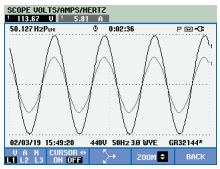
(a)i_s (before compensation)



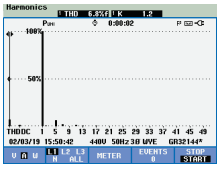
(b) i_s (after compensation)



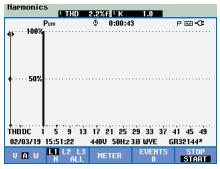
(c) Voltage & Current (before compensation)



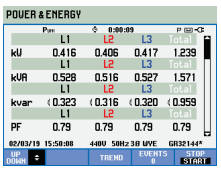
(d) Voltage & Current (after compensation)



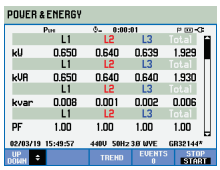
(e) Spectrum of i_s (before compensation)



(f) Spectrum of i_s (after compensation)



(g) Power and Power factor (before compensation)

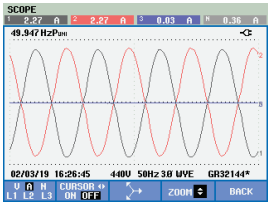


(h) Power and Power factor (after compensation)

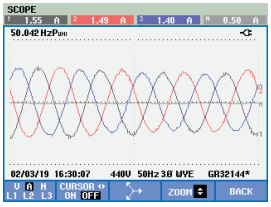
Fig. 9. Case 2: Performance of SAPF with balanced nonlinear and linear loads

0.3 Single-Phasing Operation

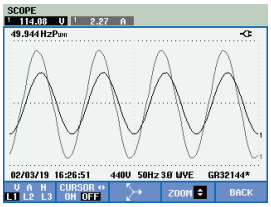
Single phasing refers to the condition of one phase open at the source/load end. With the nonlinear diode bridge, the single phasing initiated by opening the phase B. This results in three phase diode bridge to work as a single-phase bridge rectifier feeding a resistive load. The source current is still distortion free, but not balanced. The power exchange happens between the two phases leading to poor power factor at the source. The SAPF compensate for the unbalance and improves the power factor at the source end. The measurements of power analyser are shown in Fig.10a – 10h measuring the source voltage, current, power, power factor and harmonics.



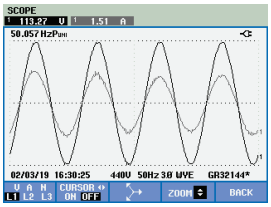
(a) i_s (before compensation)



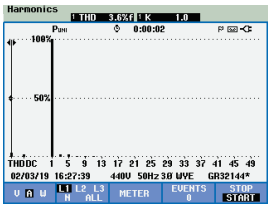
(b) i_s (after compensation)



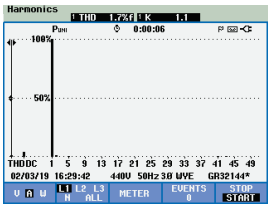
(c) Voltage & Current (before compensation)



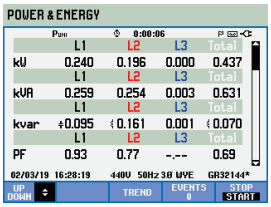
(d) Voltage & Current (after compensation)



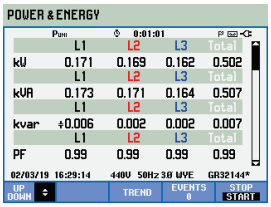
(e) Spectrum of i_s (before compensation)



(f) Spectrum of i_s (after compensation)



(g) Power and Power factor (before compensation)



(h) Power and Power factor (after compensation)

Fig. 10. Case 3: Performance of SAPF under single phasing operation

The system acts as a two-phase network with neutral isolated, one of the two phases provide return path for the current and hence the current in both the phases are equal and 180 degree out of phase. The current in third phase is zero as shown in figure 10a. in this case, the THD is less than 5% (Fig.10e) but it introduces unbalance in the source current resulting in negative sequence components. The negative sequence must be suppressed in the source. Hence SAPF generates compensating currents that will make the three phase currents in the source to be balanced sinusoidal as in Fig.10b. The load is distributed in all three phases and hence source currents in the conducting phases are reduced to 1.5A/Ph from 2.3A/ph. The THD in source current is now 1.7% and power factor of 0.99 is achieved.

Conclusion

SAPF with deadbeat control was implemented and tested through simulation and experimental setup. The performance of SAPF is tested for different loading conditions on the grid. The results obtained through simulation are verified functionally with hardware prototype for the operating conditions considered in simulation. The experimenal results proves the feasibility of the control in regulating the harmonics in grid current over wide range of load conditions. The objective of near unity power factor and grid current harmonics less than 5% were achieved. The results were presented both pictorial and with numerical values with suitable measurement arrangements with power analyzer. The controller is easier to implement and flexible to modify to achieve the desired performance.

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