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Practical hybrid solutions based on nonlinear controllers applied to PFC boost converter

Abstract. In this work, it has been investigated the combination of nonlinear controllers applied to PFC (Power Factor Corrector) boost converter. Advantages of each included technique are discussed and considered: SFL (State Feedback Linearization), PBC (Passivity based control), IDAPBC (Interconnection and Damping Assignment Passivity Based Control) and the PLL (Phase Locked Loop). We also add the analyses of tuning gains of the nonlinear control methods. In addition, we propose practical hybrid solutions to the PFC boost ($\alpha\beta$ -IDAPBC), which carry out robustness advantages. To evaluate the feasibility of the proposed methods, a Hardware in The Loop (HIL) tests are developed.

Streszczenie. W pracy zbadano możliwość zastosowania nieliniowego sterownika do przekształtnika typu boost stosowanego do poprawy współczynnika mocy. Wzięto pod uwagę: SFL – State Feedback Linearizaton, PBC - Passivity Based Control, IDAPBC – Interconection and Damping Assignement PBC oraz PLL - Phase Locked Loop. Przeanalizowano też strojenie wzmocnienia. Zaproponowano praktyczne hybrydowe rozwiązanie.(Praktyczna hybrydowa realizacja przekształtnika typu boost z nieliniowym sterownikiem w zastosowaniu do poprawy współczynnika mocy)

Keywords: Nonlinear control, PBC, SFL, IDAPBC, αβ-IDAPBC, PLL, boost converter, PFC, tuning, hybrid solutions Słowa kluczowe: przekształtnik typu boost, nieliniowy sterownik, poprawa współczynnika mocy.

Nomenclature

- E Input voltage.
- E_{in} Input grid voltage.
- E_{max} Input grid voltage peak value.
 - I_{in} Input grid current.
 - μ Duty cycle.
 - x_1 Inductor current.
 - x_2 Capacitor voltage.
 - x_{20} Initial capacitor voltage.
 - V_d Desired output voltage.
 - L Inductance.
 - C Capacitance.
 - L_f Line Filter Inductance.
 - C_f Line Filter Capacitance.
 - G Load conductance.
 - R Load resistance.

Introduction

In recent years, power factor correction remains a crucial issue, since the structure of residential and industrial network are becoming more and more electronic. Until such problematic is well-known by the academic community [1]-[3], nonlinear loads are one source of distortion in current and voltage waveforms of the electrical grid. Therefore, it is necessary that the local energy company focus on solutions for power quality problems, such as power factor correction (PFC) and reduction of harmonic content. Another and more direct way to achieve this goal is by upgrading the power supplies for electronic devices in means of control techniques applied to switched converters [4].

Among the different topologies available, the boost converter is the most suitable for this application. It's structural advantages, such as reduction in the number of components, simple actuation and the input inductor, which can reduce the grid current's THD (Total Harmonic Distortion) fits the application [5]. Disadvantages include the mode of operation, that only allows to raise an input voltage, the switch position, that doesn't offer a protection against short circuit or over-current, and the inexistance of a galvanic isolation between the input and output [6].

The central idea of this work is to verify and combine different nonlinear controllers designed to PFC systems. Firstly, two nonlinear control techniques are applied to the PFC boost converter: State Feedback Linearization (SFL) and Passivity Based Control (PBC). The validation of the PBC control can be seen in [7] and SFL in [8]. Moving onward, we strive to attack other crucial points, e.g. : adding a PLL (Phase Locked Loop) to the input and including Hamiltonian approaches (based on IDAPBC control) to increase system robustness. Disturbances in the load and voltage source are minimized with the nonlinear control without the need of variating the storage elements of the converter. In classical control, to keep the quality of results, mainly to generate low harmonic content, it is necessary to increase the nominal values of capacitors and inductors, which entails an increase of cost.

Harmonic reduction is an important issue discussed in [9] and [10] . In [8], the nonlinear control is compared with linear techniques for the boost rectifier with power factor correction. So, it have been demonstrated that the nonlinear control presents better THD index in the grid current.

This work is organized as follows. Section II presents SFL and PBC control equations and Section III describes the tuning of controller gains. Section IV shows the inclusion of PLL and Section V proposes hybrid solutions. Results and conclusions are discussed in Sections VI-VII.

PFC Boost Converter Modeling and Control

The converter topology involves a diode rectifier and a boost converter, as shown in Fig.1. Note that the rectified sine wave voltage, E, is always positive. The state variables are the inductor's current (x_1) and the capacitor's voltage (x_2) . The two possible switch states, opened or closed, are determined as a function of the control parameter μ , which is the duty cycle.

According to [7], [11], the Euler-Lagrange Model (ELM) supports the design of nonlinear models and control laws of the studied converter. With the Euler-Lagrange model, PBC control equations are obtained. The SFL control uses a State Space Model (SSM) description. Note that each model is associated with a control technique. Both nonlinear methods use the general procedure shown in Fig.1.

The SFL control represents an effective and intuitive procedure, being the most suitable for a first contact with nonlinear control techniques. Moreover, it cancels the nonlinearities of a system through a nonlinear feedback of the state output, conveniently chosen. Then, it is possible to validate the control of the studied system, through well established linear control tools. Concepts, equations and details of this technique can be seen in [12].

Passivity Based Control, on the other hand, aims to modify the dissipative structure, since the inputs and the storage elements are constant. The basic premise is to keep the en-



Fig. 1. Standard nonlinear control procedure of boost PFC and boost DC-DC converters. The control goal is to get the equation for μ . With the signal of the duty cycle synthesized, it is necessary to limit it between 0 and 1, and then the corresponding PWM signal is produced for input to the converter. The converter state variables (inductor current and capacitor voltage) and references (desired values of output voltage and current in the inductor) are fed back into the synthesizer. On the other hand, for the calculation of the duty cycle, it is necessary to estimate the value of the load represented by G_s and add an integral action.

ergy stored in the capacitors and inductors always smaller than the one injected by the source. This effect is achieved by adding "virtual" resistors in parallel or in series with the load. Such resistances are emulated by the controller by means of the duty cycle signal conditioning and the changes in the energy matrices.

According to [13], the average circuit of the boost converter can be written by Euller-Lagrange equations described by (1) and (2) as:

(1)
$$D_B \dot{x} + (1-\mu)J_B x + R_B x = F_A$$

with

$$x = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}, D_B = \begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix},$$
(2)
$$R_B = \begin{bmatrix} 0 & 0 \\ 0 & G \end{bmatrix}, F = \begin{bmatrix} E \\ 0 \end{bmatrix}, J_B = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}.$$

The equivalent state space equations are:

(3)
$$\dot{x}_1 = -(1-\mu)\frac{1}{L}x_2 + \mu \frac{E}{L},$$

(4)
$$\dot{x}_2 = (1-\mu)\frac{1}{C}x_1 - \frac{G}{C}x_2,$$

where, μ is the converter duty cycle, $0 \le \mu < 1$. As can be seen from (3) and (4), there are two state variables, x₁ and x₂ and one input (control) variable, the duty cycle μ . Briefly, the following steps are required for state feedback linearization [12]:

- 1. Choose the state variable to be controlled: the current,
 - x_1 (indirect control), or voltage, x_2 (direct control);

- derive the output g_r times until an explicit relation between output (y) and the input (E) is obtained;
- 3. choose $\mu = \mu$ (v, x) in order to cancel the non-linearities and ensure convergence of the tracking error;
- analyze the stability of internal dynamics.
 Defining L_f as the derivative of Lie [12] and choosing:

(5)
$$\begin{aligned} x_1 &= h(x), y = x_1, x_2 = L_f h, \dot{y} = 1 \dot{x}_1, \\ \dot{x}_1 &= -(1-\mu) \frac{1}{L} x_2 + \frac{E}{L}. \end{aligned}$$

Since we have to derive $g_r = 1$ times to obtain a relation between the input and output, the relative degree is $g_r = 1$. In this way, the new coordinate system is:

(6)
$$\begin{bmatrix} \dot{z}_1 \end{bmatrix} = \begin{bmatrix} z_2 \end{bmatrix} = \begin{bmatrix} v \end{bmatrix}, \\ \begin{bmatrix} z_1 \\ z_2 \end{bmatrix} = \begin{bmatrix} x_1 \\ v \end{bmatrix}.$$

Using the control law $v = r^{(g_r)} - k^T e$, with k and e given by:

$$k = [k_1],$$

 $e = [e_1] = [x_1 - r]$

obtains:

(7)

(8)

$$v = \dot{r} - k_1 e_1$$

(9)
$$-(1-\mu)\frac{1}{L}x_2 + \frac{E}{L} = \dot{r} - k_1(x_1 - r).$$

Isolating μ and considering the reference r=x_{1d}, the general expression for the duty cycle equation is:

(10)
$$\mu_{SFL} = 1 - \frac{[E + Lk_1 (x_1 - x_{1d}) - L\dot{x}_{1d}]}{x_2}.$$



Fig. 2. Real and imaginary components of the eigenvalues for indirect DC-DC control in view of three different configurations: config.1 (A), config.2 (B) and config.3 (C).

It can be seen that as the relative system degree is one (there is only one switch to control two variables), it is necessary to perform only one branch, which is already inferred directly from (3). Thus, we need only one control equation given by (10).

For PBC control, let us consider the state error as a function of the desired vector x_d :

(11)
$$\begin{aligned} \tilde{x} &= e, \\ \tilde{x} &= x - x_d. \end{aligned}$$

The error equation formulated as in (1) and (2) becomes:

(12)

$$D_B\dot{\tilde{x}} + (1-\mu)J_B\tilde{x} + R_B\tilde{x} + R_{damp}\tilde{x} = \psi,$$

$$\psi = F - [D_Bx_d + (1-\mu)J_Bx_d + R_Bx_d] + R_{damp}\tilde{x},$$

In order to guarantee the error vector to converge to zero, one has to impose $\Psi = 0$, which can be written as:

(13)
$$\begin{array}{l} L\dot{x}_{1d} + (1-\mu) \, x_{2d} - R_{1damp} \tilde{x}_1 = E, \\ C\dot{x}_{2d} - (1-\mu) \, x_{1d} + \frac{G}{C} x_{2d} - R_{2damp} \tilde{x}_2 = 0. \end{array} ,$$

where R_{damp} is the damping matrix defined as:

(14)
$$R_{damp} = \begin{bmatrix} R_{1damp} & 0\\ 0 & R_{2damp} \end{bmatrix}.$$

 R_{damp} is the damping added to the system which shapes its energy. Some fundamental definitions regarding passivity, and the derivation of the control equations, in view of this method, can be found in [11] and [7]. Aiming at rendering the system passive, by the condition established in (13), one has:

(15)
$$\dot{x}_{2d} = \frac{(1-\mu)x_{1d} - Gx_{2d} + R_{2damp}(x_2 - x_{2d})}{C},$$

(16)
$$\mu_{PBC} = 1 - \frac{[E + R_{1damp}(x_1 - x_{1d}) - L\dot{x}_{1d}]}{x_{2d}}$$

Also, in order to minimize errors in steady state of the output voltage, at a desired value V_d , it is useful to add a proportional integrative term in the control law, given by:

(17)
$$G_{Int} = -k_{int} \int_0^t [x_2(s) - V_d] ds.$$

The load estimation is given as (18):

(18)
$$\dot{G}_s = -k_g x_{2d} (x_2 - x_{2d}).$$

Control tunning

In [14] it is proposed an approach for gain estimation of the PBC control based on real-time calculation. However, the methodology does not apply to a sinusoidal input system, since the main figure of merit of a PFC system is the harmonic distortion rate of the grid current (THDi).

Unlike the classical control, the gain of nonlinear controllers does not occur directly, because there is no Laplace transform. In this sense, one objective of this work is to deduce an intuitive method to obtain the gains of nonlinear controllers, SFL and PBC, applied to boost PFC converters. Since the equations similatiry, the two methods are analyzed together.

0.1 Steps

In summary, the following steps of the proposed methodology, which can be used for PBC and SFL control, are listed:

Step 1. Find starting R_{1damp} :

The first step is to find the DC-DC system analogous to the AC-DC system. To do this, the value of the input in the DC-DC system corresponds to the effective rms value of the input in the PFC system.

Plot the real and imaginary parts of the eigenvalues in view of variations of R_{1damp} for the corresponding DC-DC system. This graphic is important for estimating the value of R_{1damp} , which response is no longer oscillatory (when the imaginary part of an eigenvalue is null). In [14] it is suggested the following formula to find an ideal R_{1damp} , with fast response and low oscillation:

(19)
$$G_{1damp} = \frac{1-\mu}{1-\gamma} \sqrt{\frac{C}{L}} - G,$$

 $(20) R_{1damp} = \frac{1}{G_{1damp}}$

where $\gamma = 0.5$, *C* is the capacitor's value, *L* the inductor's value and *G*, the conductance of the load. The initial value of the capacitor voltage starts at $x_{20} = V_d$. Since we're interested in the current tracing, the dynamics of the desired voltage regulation is ignored.

For the same reason, consider $x_2 = V_d$ and $x_{2d} = V_d$ in (10) and (16). In those same equations, for SFL and PBC controls, note the relation:

Step 2. Variation of R_{1damp} :

Table 1. Parameters used in tests.

Parameters	Configuration	Configuration	Configuration		
	1	2	3		
R	52.5 Ω	151.51 Ω	30 Ω		
Rmin	1 Ω	5 Ω	5 Ω		
Rmax	105 Ω	250 Ω	60 Ω		
L	0,6 mH	1,54 mH	10 μH		
С	2800 µF	760 μ F	50 μ F		
X ₂₀	140 V	200 V	3 V		
E_{in}	100 Vrms	141,42 Vrms	1 Vrms		
Emax	141,42 V	180 V	1,41 V		
V_d	180 V	300 V	5 V		

Gradually increase the value of R_{1damp} , obtaining the THD of the grid current;

The nominal load is varied to 100%, since the worst case (high THD) is considered for light loads.



Fig. 3. Variation of R_{1damp} : Normalized grid voltage (142 Vpp/20 - light line - middle), grid current (dark line - top) and normalized duty cicle (bottom, sloped gray) for a load variation from 52.5 to 105 and $R_{1damp} = 0,1$ (A), $R_{1damp} = 33$ (B) e $R_{1damp} = 60$ (C).

Step 3. Variation of the integral gain k_{int} :

The value of the integral gain k_{int} is gradually increased, obtaining the THD of the mains current.

Step 4. Variation of the load adaptive gain k_g :

The value of the adaptive gain k_g is gradually increased, obtaining the THD of the mains current. In addition, for the gains variation tests it is important to know the maximum value of the adaptive gain k_g . In [8] it is proven and suggested the following expression for the limit value of k_g .

(22)
$$0 < k_g < \varepsilon_1 \frac{\beta Gmin - \gamma C^{-1} Gmax^2}{\gamma (x_{20} - V_d)^2}$$

$$\beta = \frac{Emax\xi}{C}$$

(24)
$$\gamma = \frac{L\xi^2 G_{max}}{2C}$$

$$(25) \qquad \qquad \xi = \frac{2V_d^2}{E_{max}}$$

(26)
$$Rmin = \frac{1}{Gmax}.$$

Where ε_1 is a small constant considered, x_{20} is the initial value of the capacitor, sufficiently larger than the input voltage with peak value E_{max} , C is the capacitance, L the inductance, V_d is the desired value for the output voltage, G_{min} and G_{max} are the minimum and maximum conductances, respectively.

Step 5. Variation of R_{2damp} :

The value of R_{2damp} is gradually varied, obtaining the THD of the mains current. The use of this gain is optional when using the integral gain.

The gain R_{1damp} is the main one, because besides being common in the SFL and PBC control, it is responsible for tracking the current x_1 (the chosen variable to be controlled) at its desired value x_{1d} . Its behavior is analogous to the proportional gain for classical controllers. Note that it is not necessary to integrate (10) and (16), as the gain R_{1damp} multiplies the current error $(x_1 - x_{1d})$. The gain R_{2damp} is analogous to the integrative gain, since it tends to minimize errors in the steady state of the output voltage x_2 . Note that it becomes necessary to integrate (15) to return the desired value x_{2d} . For the DC-DC system, the higher the value of R_{1damp} , the higher the tracking speed of the desired current x_{1d} , leading the error $(x_1 - x_{1d})$ to approach zero faster. However, in practice, there are limits to the value of R_{1damp} due to the sampling process [8].

0.2 Design example and simulation

In this section the nonlinear controller's gains are estimated. Three different configurations (based on [7]-[8]) are presented for the boost PFC, according to Table 1. Mainly, the gain values that correspond to a quick response (less than 0.5s), small overshoot (less than 10%) and minor oscillatory dynamics are investigated. Likewise, the main performance criteria is the THD index (as lower, the better).

The following steps are necessary for the three different configurations shown in Table 1:

1. Start damping, R_{1damp}, calculation:

$$\begin{aligned} G_{1damp1,2,3} = & \frac{1 - \mu_1}{1 - \gamma} \sqrt{\frac{C_1}{L_1}} - G_{1,2,3}, \\ R_{1damp1,2,3} = & \frac{1}{G_{1damp1,2,3}}, \end{aligned}$$

(27)

$$R_{1damp1} = 0, 42; R_{1damp2} = 1, 53; R_{1damp3} = 1, 1625$$

- *R*_{1damp} variation and achievement of the grid current THD index (Fig.2 and Table 2)
- Variation of *k_{int}* and achievement of the grid current THD index (Table 3).
- Variation of the adaptive gain k_g and achievement of the grid current THD index (Table 4).

Letting $\varepsilon_1 = 1$ and the given values of Table 1, the gain values $k_{g1max} = 0,022$, $k_{g2max} = 0,0015$ and $k_{g3max} = 200$ are found for the three configurations of the boost converter.

Figs. 4 and 5 present the voltage response for a load disturbance, where consecutive step of 70% to 100% are applied in the simulated systems. In each 0.5s the gains R_{1damp} and k_{int} are also variated.

Inclusion of PLL

As previously mentioned, step-up or boost converters has high performance and is, therefore, strongly recom-

Table 2. THDi as a function of $de R_{1damp}$ for SFL control.

		1						
R_{1damp1}	THDi (%)		R_{1damp2}	THDi (%)		R_{1damp3}	THDi (%)	
*	R		*	R		*	R	
	52,5 Ω	105 Ω		151,55 Ω	303,02 Ω		30 Ω	60 Ω
0,05	28,12	33,54	0,1	25,54	30,93	0,01	9,04	23,9
0,1	25,81	30,71	1	13,62	18,80	0,1	7,88	18,24
3	5,59	9,73	60	2,67	4,29	0,6	6,96	16,79
10	5,01	8,25	65	2,58	4,13	0,65	6,83	18
30	4,79	8,12	85	2,50	4,06	1	7,22	28,94
31	4,84	8,21	88	2,50	3,96	2	26,6	32,29
32	4,84	8,20	90	2,67	4,22	3	30,46	29,16
<u>33</u>	4,78	8,1	91	2,77	4,41	10	28,70	27,49
34	4,8	8,1	93	5,22	7,79	12	28,88	27,46
45	7,16	18,85	99	13,29	13,55	35	28,58	27,43
60	25.81	32 35	100	14.63	16 43	100	28 56	27 42



Fig. 4. Software simulation result for Boost PFC using control techniques SFL (black), PBC (gray). Output voltage x_2 for load variation (70 - 100 %) in each 0.25s (highlighted arrow) and R_{1damp} variation (0.3 - 3 - 60) in each 0.5s (dashed arrow).



Fig. 5. Software simulation result for boost PFC using control techniques SFL (black), PBC (gray). Output voltage x_2 for load variation (70 - 100 %) in each 0.25s (highlighted arrow) and $|k_{int}|$ variation (10 - 100 - 1000) in each 0.5s (dashed arrow).

mended to work in regulated power supplies. Nonetheless, without adequate control such converters eventually provide high levels of THD (Total Harmonic Distortion) and low power factor (PF). Thus, different works has been validated linear and nonlinear controllers applied to static converters [8]. However, through these studies it was observed that the qual-

Table 3. Variation of the integral term, grid current THDi and Settling time.

<i>k</i> _{int1}	THDi (%)			Settling time(s)
	Load (Ω)			
	25	52,5	105	Та
-2	2,02	4,65	9,86	0,33
-500	0,93	2,95	8,01	0,3
<u>-1500</u>	0,89	2,08	6,7	0,3
-2000	2,55	1,83	5,4	0,31
-2500	3,18	1,47	4,7	0,31
-5000	27,6	32,3	11	0,55
k _{int2}	THDi (%)			Settling time(s)
	Load (Ω)			
	75,75	151,51	303,02	Ts
-0,2	2,75	4,28	8,3	0,25
-2	2,69	4,21	7,8	0,2
-20	2,73	4,03	7,2	0,2
-100	2,47	4,02	7,02	0,05
-200	2,56	3,62	6,42	0,05
-500	4,17	4,47	9,99	0,05

ity of results is associated with the input signal voltage. Thus, the insertion of the PLL (Phase-Locked Loop) is justified by the poor quality of networks.

That is, the power supply voltages are not purely sinusoidal and usually have very harmonic content. Thus, lower THD levels can be obtained by adding the PLL for imposing a sinusoidal reference signal to the input voltage [15]. This inclusion is optional, however, the objective of this section is to verify the use of a PLL (Phase-Locked Loop) associated with a high power factor and low THD boost rectifier. For illustration purposes, the examples consider the passivity based control.

Table 4. Grid current THDi in function of the adaptive gain k_q

k _{g1}	THDi (%)			Settling Time (s)
	Load Ω)			
	25	52,5	105	Ts
0,0022	2,75	4,17	8,75	0,15
0,022	0.89	3,62	6,42	0,1
0,22	8,21	12,67	8,59	>0 ,6
k_{g2}	THDi (%)			Settling Time (s)
k_{g2}	THDi (%) Load Ω)			Settling Time (s)
<i>k</i> _{g2}	THDi (%) Load Ω) 75,75	151,51	303,02	Settling Time (s) Ts
<i>k</i> _{g2} 0,00015	THDi (%) Load Ω) 75,75 2,32	151,51 5,16	303,02 8,75	Settling Time (s) Ts 0,15
<i>k</i> _{g2} 0,00015 0,0015	THDi (%) Load Ω) 75,75 2,32 2,56	151,51 5,16 3,91	303,02 8,75 6,42	Settling Time (s) <i>Ts</i> 0,15 0,05

It should be noted that, with the inclusion of the PLL, the value of E is replaced by E_{PLL} which in this case is the sine signal returned by the synchronization of the PLL. So, Equation (16) becomes:

(28)
$$\mu_{PBC} = 1 - \frac{[E_{PLL} + R_{1damp}(x_1 - x_{1d}) - L\dot{x}_{1d}]}{x_{2d}}$$

Improving performance using α and β operators

Now, let us continue improving results obtained in Eqs. (10) and (16). Briefly, we consider two control laws based on IDAPBC, previously and recently found in the literature. In[16], Classic IDAPBC, which will refer as CIDAPBC, is applied to boost converters attaining a simplified and open loop control equation described by: **CIDAPBC**:

(29)
$$\bar{\mu} = 1 - \frac{E}{V_d}, \mu = 1 - (1 - \bar{\mu}) \left(\frac{x_2}{V_d}\right)^{\alpha}.$$

Yet, [17] proposed an evolution of (29) given by: IDAPBC:

(30)
$$\mu = 1 - \frac{E\beta}{2E(x_2 - x_{2d}) + \beta x_{2d}}$$

Control law adaptations (31)-(35) are suggested, taking into account the control equations found in the SFL and PBC control. Such adjustments are made by replacing the equations of the duty cycle - found in the SFL and PBC methods in IDA-PBC control laws (29)-(30):

 α -IDAFLC (combines SFL and CIDAPBC solutions):

$$\bar{\mu}_2 = 1 - \frac{[E + R_{1damp}(x_1 - x_{1d}) - L\dot{x}_{1d}]}{x_2},$$

(31)
$$\mu = 1 - (1 - \bar{\mu}_2) \left(\frac{x_2}{V_d}\right)^{\alpha}$$

 α -IDAPBC (combines PBC and CIDAPBC solutions):

$$\dot{x}_{2d} = \frac{(1-\mu)x_{1d} - Gx_{2d} + R_{2damp}(x_2 - x_{2d})}{C},$$
$$\bar{\mu}_3 = 1 - \frac{[E + R_{1damp}(x_1 - x_{1d}) - L\dot{x}_{1d}]}{x_{2d}},$$

(32)
$$\mu = 1 - (1 - \bar{\mu}_3) \left(\frac{x_2}{V_d}\right)^{\alpha}$$

 $\alpha\beta$ -IDAPBC (CIDAPBC and IDAPBC solutions):

(33)
$$\mu = 1 - \left(\frac{E\beta}{2E_{max}(x_2 - x_{2d}) + \beta x_{2d}}\right) \left(\frac{x_2}{V_d}\right)^{\alpha}$$

 $\alpha\beta\text{-PBC}$ (combines PBC, CIDAPBC and IDAPBC solutions):

(34)

$$\mu = 1 - \left(\frac{E\beta + R_{1damp}(x_1 - x_{1d}) - L\dot{x}_{1d}}{2E_{max}(x_2 - x_{2d}) + \beta x_{2d}}\right) \left(\frac{x_2}{V_d}\right)^{\alpha}$$

Table 5. Power factor and THDi with and without PLL, and by considering load/input variations.

Load(Ω)/ E_{in}	THDi (%)	THDi (%) with	Power Factor
(V)	without PLL	PLL	with PLL
52,5 / 100	8,6	2,8	0,99
35 / 100	9,3	2,5	0,99
105 / 100	11,7	3,8	0,99
52,5 / 85	8,5	3,3	0,99
52,5 / 115	9,5	3,0	0,99

 $\alpha\beta p$ -PBC (combines CIDAPBC and the mean of PBC and IDAPBC solutions):

(35)
$$F_{1} = \frac{E\beta}{2E_{max}(x_{2} - x_{2d}) + \beta x_{2d}};$$
$$F_{2} = \frac{E + R_{1damp}(x_{1} - x_{1d}) - L\dot{x}_{1d}}{x_{2d}};$$
$$F = F_{1} + F_{2}; \mu = 1 - \frac{F}{2} \left(\frac{x_{2}}{V_{d}}\right)^{\alpha}$$

Equations (31)-(35) have the same zero-order dynamics of (16),(30), which stability proofs have already been proved in [7] and [17].

Main results

In order to analyze the combination of several methods, simulation results have been developed in Matlab/Simulink and Hardware in The Loop. In Fig.6, are shown the voltage and current network (A), the output voltage x_2 on the capacitor (B) and details of input voltage and current network (C) using PLL in view of the following nominal conditions: R = 52,5 Ω , L= 0,6 mH, C =2800 μF , line filter with L_f = 50 μ H and C_f = 5 μ F , E_{in} =100 V_{rms} (with 8.5 % THD), α =-0.44, β =330, V_d = 180 V and the best gains of Tables II-IV. It should be noted that the input current tracks the input voltage and the output voltage is regulated to 180V.

Fig. 6 and Table V show the benefits of the PLL inclusion, furthermore, a small total harmonic current distortion (TDHi) is obtained. Therefore, in applications that deal with critical current harmonics, the addition of the PLL with nonlinear controllers has proven to be an efficient solution.

As sketched in Figs.6-7, the output voltage can asymptotically track the set-point even if the load perturbation is present. The hybrid nonlinear controllers attain low THDi (<3%), low overshoot (<10%) and fast response speed (<0.05 s). The power factor achieved for the nominal condition is PF = 0.99. In Fig.7-B are shown the input current in phase with input voltage (ac-dc measurement using oscilloscope). Again, the experimental waveforms are mostly sinusoidal. The Hardware in The Loop load perturbation is sketched in 7-C.

Conclusion

In this paper, the nonlinear control (state feedback linearization control- SFL, and the passivity based control -PBC) gains are estimated, by considering the grid's current total harmonic distortion index, TDHi, as the main performance criteria in a PFC boost converter application. The most appropriated gains for the three configurations are listed and highlighted in Tables 2, 3 and 4. The addition of PLL was also verified and recommended in crucial harmonics reduction.

Moreover, it was proposed hybrid solutions (derived from SFL, PBC and IDAPBC) that can be applied to PFC systems: α -IDAPBC, $\alpha\beta$ -IDAPBC, $\alpha\beta p$ -IDAPBC and $\alpha\beta$ -PBC. The resultant output voltages and input currents are practically sinusoidal. We highlight some advantages: $\alpha\beta$ -IDAPBC needs



Fig. 6. α -IDAPBC results.Input currents waveforms compared with PLL (moved +10 A) and without PLL (A). 50 % Load variation with PLL: output voltage x_2 (B). Details: normalized input voltage E_{in} (142 Vpp / 20) and input current I_{in} (C).



Fig. 7. Simulink Simulation (A) and Hardware in The Loop experimental (B-C) tests using control techniques $\alpha\beta$ -IDAPBC(continue cyan), $\alpha\beta$ -PBC (dashed magenta) and $\alpha\beta$ p-IDAPBC (green). Output voltage x_2 in view of load variation (70 \rightarrow 100 %) in 0.15s. Details: normalized input voltage $|E_{in}|$ and normalized input current $|I_{in}|$ in HIL (B). Load variation test in HIL (C).

only the measurement of x_2 and input voltage E, and $\alpha\beta p$ -IDAPBC has smaller overshoot.

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