

A Synchronous Resonant Switched-Capacitor DC-DC Boost Converter - Experimental Results And Feasibility Model

Abstract. This paper presents results of experimental research of a resonant switched capacitor voltage multiplier (SCVM) in the synchronous topology (SYSCVM). The classical SCVM utilizes diodes in the branches responsible for charging the switched capacitors. In the SYSCVM, additional MOSFET switches are connected in parallel with the diodes. Therefore, an improvement of efficiency is achieved. The paper presents experimental results of operation and efficiency of the SYSCVM. Furthermore, the issues related to the design of the converter with synchronous switches and the problems of the supply of the gate drivers are discussed.

Streszczenie. W artykule przedstawiono wyniki badań eksperymentalnych rezonansowego przekształtnika DC-DC o przełączanych kondensatorach powielającego napięcie stałe w topologii synchronicznej (SYSCVM – Synchronous Switched Capacitor Voltage Multiplier). W klasycznym rozwiązaniu analizowany przekształtnik o przełączanych kondensatorach wykorzystuje diody w obwodach ładowania przełączanych kondensatorów. W układzie SYSCVM diody połączone są równolegle z tranzystorami MOSFET dla uzyskania większej sprawności układu. Artykuł przedstawia wyniki pomiarów eksperymentalnych układu dotyczących weryfikacji działania oraz jego sprawności. Ponadto, problemy związane z praktyczną implementacją koncepcji synchronicznego układu (SYSCVM) zostają również omówione. (Układ powielacza napięcia w technice przełączanych kondensatorów w topologii synchronicznej - badania eksperymentalne i studium wykonalności).

Słowa kluczowe: Przekształtnik wielopoziomowy, przekształtnik DC-DC, przełączane kondensatory, powielacz napięcia, pompa ładunku
Keywords: Multilevel converter, DC-DC converter, switched-capacitors, voltage multiplier, charge pump

Introduction

The switched-capacitor (SC) converters have some important advantages in comparison to other concepts, such as high voltage gain, quasi inductiveless design, low weight of the converter, high efficiency and very simple control. The SC DC-DC converters represents a wide family of topologies, with multiple representation in the scientific literature [1]-[14].

sources of losses is located in the diodes placed in the charging circuits.

Thus, the concept of improvement of efficiency using the multiplier SYSCVM (Fig. 1b) was introduced in [9]; however, without an experimental confirmation. This paper presents results of the analytical and experimental research of the SYSCVM, demonstrating the operation, feasibility and efficiency performance of the converter.

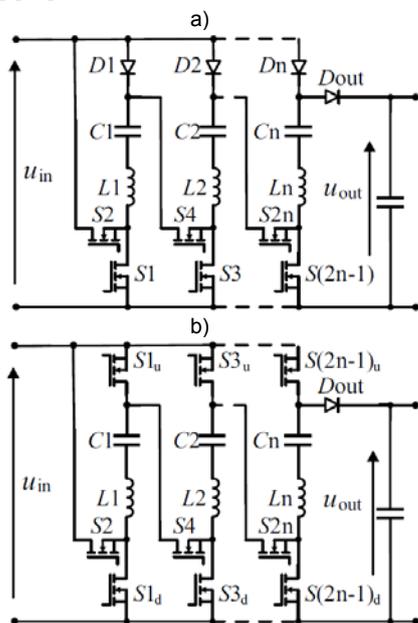


Fig.1. DC-DC converter in the topology of: (a) basic Resonant Switched-Capacitor Voltage Multiplier (SCVM), (b) Synchronous Resonant Switched-Capacitor Voltage Multiplier (SYSCVM) [9]

The SCVM converter (Fig. 1a) is an interesting and attractive topology from the applications standpoint, owing to its relatively simple and modular composition. This converter can create a representative research model for investigations of problems related to SC topologies. High efficiency of the power SC converter is achieved by the application of resonant circuits for charging and discharging of the switched capacitors. However, one of the major

Basics of operation of the SYSCVM

The SYSCVM operates in a similar way as the basic SCVM [9], by charging the switched capacitors from the input source in parallel connection, and discharging them to the output capacitor in a series connection (Fig. 2).

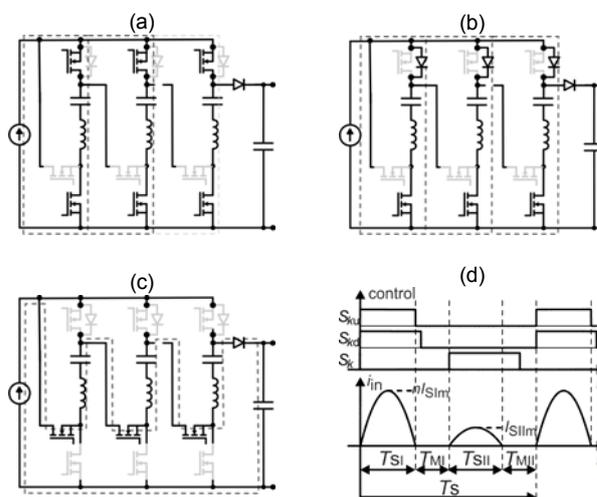


Fig.2. Operating principle of the SYSCVM: (a) charging of the capacitors through the lower and upper MOSFET transistors, (b) charging of the capacitors through the lower transistors and upper diodes, (c) discharging of the capacitors, (d) control of switches and parameters of waveforms

The efficiency increase is achieved by synchronous switching on the lower and upper charging MOSFET transistors (S_{kd} , S_{ku}). When the upper transistor is switched-off, the current can flow through the upper diode or the body diode of the upper transistor (as in the basic SCVM). This

can occur at the end of the charging half-period because the upper transistor can be turned-off before the current crosses zero; however, a negative current flow in the charging circuit is possible.

A detailed analysis of efficiency of the basic SCVM (Fig. 1a), as well as of the SYSCVM, is presented in [9]. According to this reference, the efficiency of the SCVM is the following:

$$(1) \quad \eta = 1 - \frac{n\pi^2 P_{in} r_S T_S}{4(n+1)^2 U_{in}^2 T_{SI}} - \frac{\Delta U_{DS}}{U_{in}} - \frac{\Delta W_{sw} f_S}{P_{in}},$$

where n is the number of cells, U_{in} is the input voltage, P_{in} is the input power, $f_S = 1/T_S$ is the switching frequency, T_{SI} is the current pulse duration, r_S is the total resistance of each cell, including MOSFETs resistances, ΔU_{DS} is the voltage drop across each diode, ΔW_{sw} is the energy lost at turn-on in all the MOSFETs' resistances in a single switching cycle T_S .

In the model of efficiency (1), it is assumed that the values of elements in each cell are the same, both in the circuits of charging and discharging of the cell capacitors, pulse durations T_{SI} and T_{SII} are the same, dead-times T_{MI} and T_{MII} (Fig. 2d) are the same, and the voltage drops across the diodes remain constant in the conducting state.

In the SYSCVM, the conduction power losses in the diodes in the branches of charging the cell capacitors are eliminated, but the overall resistance of these circuits rises k times where r_S is the resistance of each of the MOSFETs paralleling the charging diodes:

$$(2) \quad k = \frac{r_S + r_S'}{r_S}.$$

The efficiency of the SYSCVM is expressed by [9]

$$(3) \quad \eta = 1 - \frac{1}{(n+1)} \left[\frac{n\pi^2 (k+1) r_S' P_{in} T_S}{8(n+1) U_{in}^2 T_{SI}} + \frac{\Delta U_{DS}}{U_{in}} \right] - \frac{\Delta W_{sw} f_S}{P_{in}},$$

where ΔU_{DS} is the voltage drop across diode D_{out} .

An SYSCVM has a higher efficiency than an SCVM of the same parameters if

$$(4) \quad r_S' < \frac{8(n+1) U_{in} T_{SI} \Delta U_{DS}}{\pi^2 P_{in}},$$

where ΔU_{DS} is the voltage drop across each of the diodes (paralleled in SYSCVM by MOSFETs).

From (1) to (4), it follows that the synchronous converter can achieve improvement of efficiency by elimination of conduction power losses in the charging diodes. The efficiency of SYSCVM is higher than that of SCVM for sufficiently low r_S and P_{in} , which is shown in Figure 3. At larger powers, MOSFET switches may not withstand the condition (4), and the SCVM becomes more efficient.

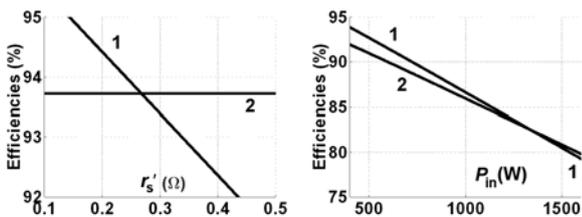


Fig.3. Efficiencies of SYSCVM and SCVM as a function of: (a) r_S' at $P_{in} = 200$ W, (b) P_{in} at $r_S' = 40$ m Ω . 1 - SYSCVM, 2 - SCVM. Common parameters: $n = 3$, $U_{in} = 30$ V, $T_{SI}/T_S = 0.5$ (zero dead-time), $r_S = 100$ m Ω , $U_{DS} = 1.1$ V, $f_S = 109.8$ kHz, $\Delta W_{sw} = 10$ μ J. Calculations based on (1) and (3)

Experimental setup and cost of the converter

To confirm the feasibility and the operation of the converter, as well as its efficiency, an experimental setup of a three-cell SYSCVM was designed (Fig. 4). The parameters of the setup are presented in Table 1.

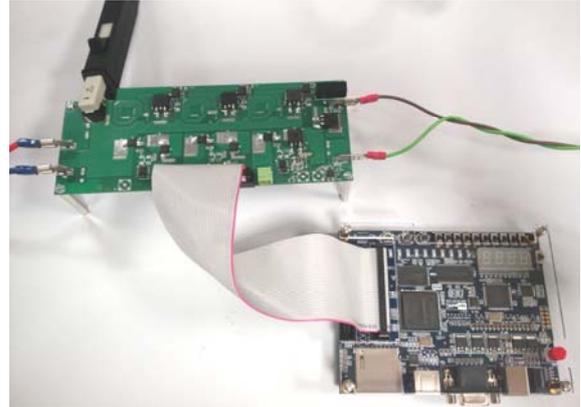


Fig.4. Experimental setup of the SYSCVM with an FPGA-based pulse generator (DE zero board)

Table 1. Parameters of experimental setup of SCVM and SYSCVM

Items	Specification
Number of switching cells	3
Input voltage	30V/40V
Lower MOSFETs S_{kd}	2xSIR872, 1xIRFS4229PbF
Upper MOSFETs S_{ku}	2xIRFS4229PbF 1xIRFS4321PbF
Discharging MOSFETs	2xSIR872 1xIRFS4321PbF
Switched capacitors	2470nF
Resonant inductances	0.85uH
Output diode	STTH3006
Upper diodes in SCVM configuration	STTH3006

The SYSCVM is more complex from the standpoint of gate driver circuits design; however, it can be achieved in an economic way. The lower MOSFETs' drivers have common ground whilst the gate drivers of the discharging MOSFETs can be supplied in bootstrap circuits (Fig. 5). The upper MOSFETs have also common sources; thus, their gate driver system requires a single separated supply voltage (VCC2 in Fig. 5).

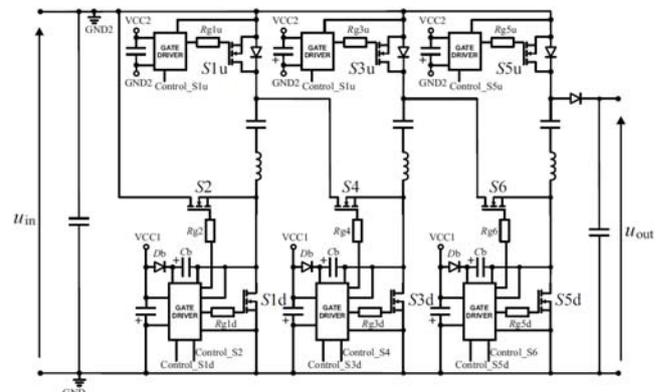


Fig.5. The proposed gate driver system in the SYSCVM

Experimental results

The operation of the SYSCVM is similar to that of the SCVM described in [9] to [12]. In the SYSCVM, the diodes in the charging branches are paralleled by MOSFET transistors. Conduction of these MOSFETs should be synchronized with the lower transistors and should be

adjusted to the time of oscillation of the charging currents. Figure 6 presents the experimental waveforms of the control signals for the transistors in the SYSCVM. It is visible in it that the control signals for the upper charging transistors have a longer high state than the signals for the lower charging transistors. This assures that the body diode of the upper MOSFET does not conduct any current.

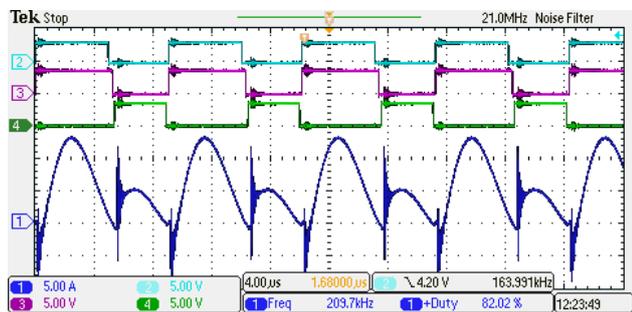


Fig.6. Experimental results of the SYSCVM. Waveforms of the input current (1) and control signals of groups of transistors: lower charging transistors (2), upper charging transistors (3), discharging transistors (4). $U_{in} = 40\text{ V}$, $P_{out} = 200\text{ W}$

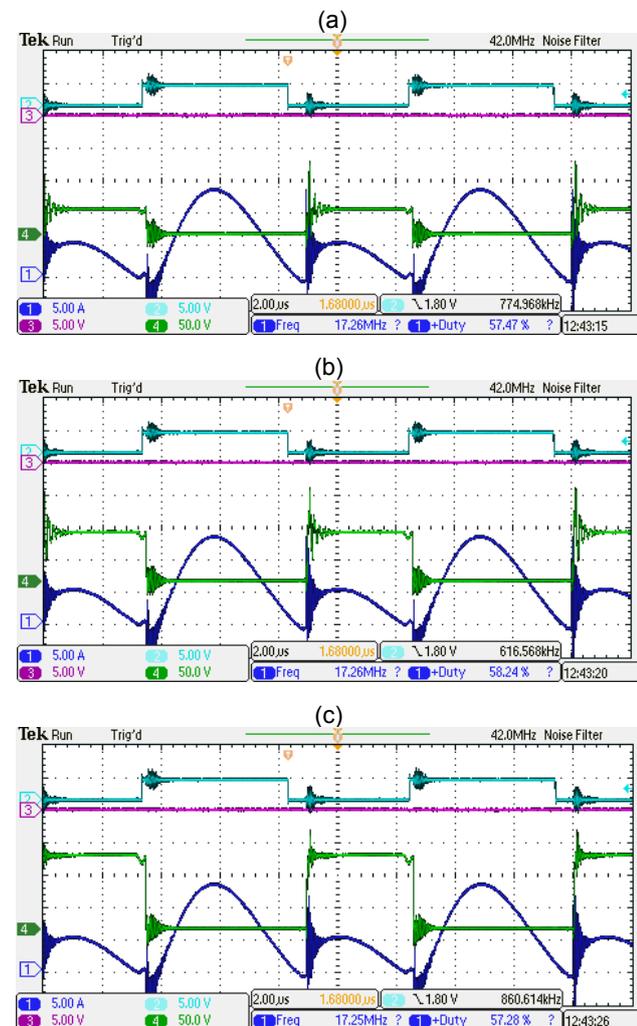


Fig.7. Experimental results of the SYSCVM. Waveforms of the input current (1) and voltage on the upper switch (4): the S_{1u} (a), the S_{2u} (b), the S_{3u} (c). $U_{in} = 40\text{ V}$. Channel (2) displays control signal of lower charging transistors

Figure 7 presents waveforms associated with the problem of the selection of the upper transistors for a practical implementation. From these results, it follows that

the distribution of the voltage on the upper switches is not equal. The highest voltage stress is visible on the switch closest to the output whilst the lowest is on the first switch from the input side.

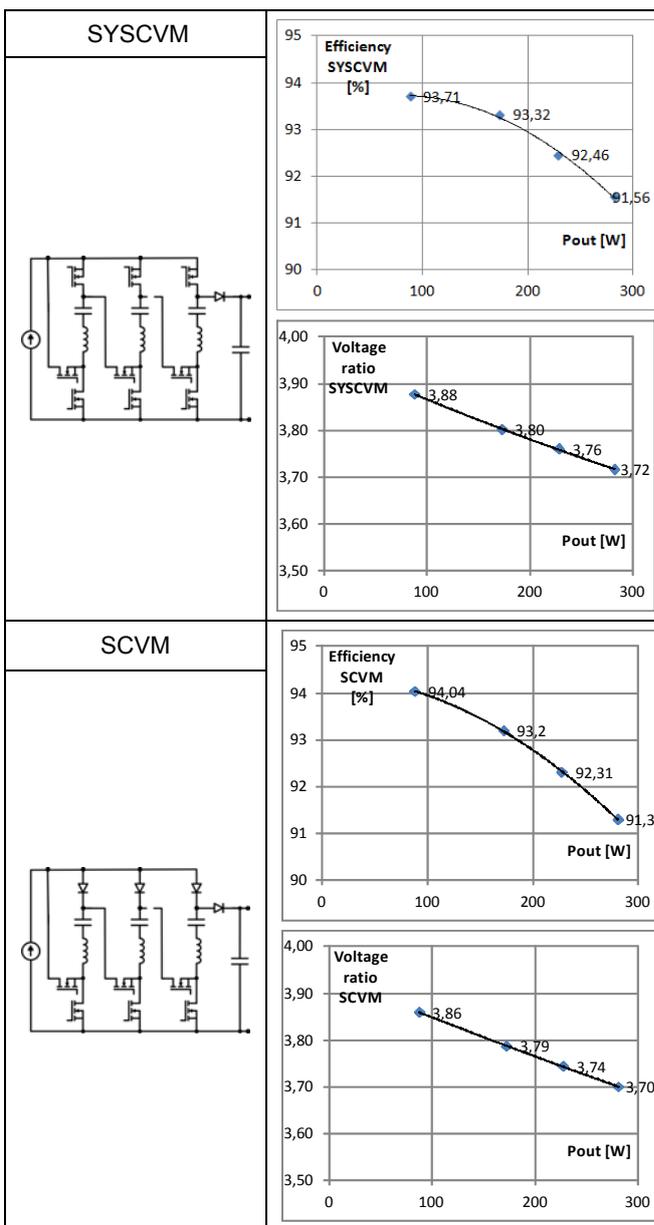


Fig.8. Experimental results of the SYSCVM. Results of measurements of efficiency and the voltage ratio versus power of the SYSCVM and SCVM converters. $U_{in} = 30\text{ V}$

The results presented in Fig. 8 concern the efficiency of the converter. During the tests, two sets of measurements were performed for the SYSCVM as well as for the SCVM converter. From the results, a slight improvement of the efficiency can be seen for higher loads. For load of about 150W, the efficiencies of both solutions are equal. For lower load the SCVM has slightly better efficiency. This is due to the power losses in the MOSFETs' capacitances, which are charged and discharged in each switching cycle. Therefore, the converter does not operate without switching losses (as in ZCS). These power losses are almost independent on the load of the converter; thus, they lower its overall efficiency for low power operation. This issue is not considered in the simplified analysis presented at the beginning of the paper (3). To improve these results, a detailed mathematical model and optimization technique

are needed to find trade-off between switching and conduction losses by careful selection of the frequency and the type of the MOSFETs. A lower voltage drop across the MOSFETs in comparison to that across the diodes results in a slightly higher voltage ratio of the synchronous converter (SYSCVM) against the SCVM for the whole range of the measured power of the load. The benefits of synchronous operation can be definitely bigger in the voltage multipliers where the conduction losses of the diodes dominate over the switching and resistive losses (low frequency systems with low input voltage).

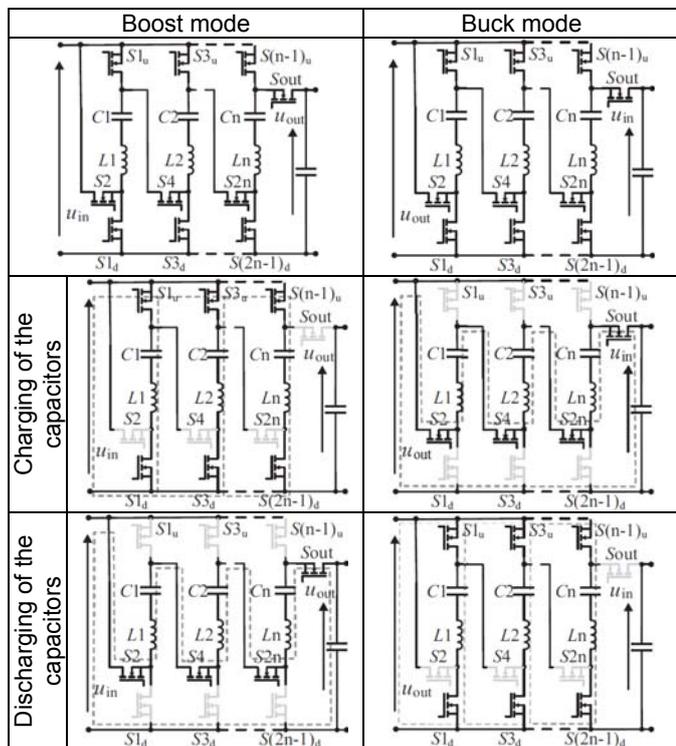


Fig.9. A bi-directional buck-boost converter and its operation modes

Conclusions

The experimental results of the investigation of the synchronous switched-capacitor voltage multiplier (SYSCVM) make it possible to draw the following conclusions:

- The concept of SYSCVM is correct and feasible,
- The design with the additional MOSFET transistors remains not very complicated and not expensive from the gate driver system standpoint,
- Voltage stresses on the additional transistors in the SYSCVM are not equal. The devices closer to the input side have lower voltage stresses; therefore, MOSFET transistors with very low $R_{ds(on)}$ and low cost can be selected in some switching cells,
- In the demonstrated laboratory setup, the SYSCVM achieved a slightly better efficiency and voltage ratio versus the SCVM converter. More significant benefits of the application of the synchronous multiplier are supposed in the systems where conduction losses in the diodes represent an important part of total losses (low frequency systems) and the application of MOSFETs with very low $R_{ds(on)}$ can be possible.

Future works should focus on a detailed mathematical model and on optimization of the SYSCVM's components selection to achieve better performance improvement over the SCVM design.

Future works – bi-directional buck-boost converter

In the future works, the synchronous multiplier (SYSCVM) can be utilized in a bi-directional buck-boost converter (Fig. 9). Apart from the upper MOSFETs, the converter utilizes an output MOSFET.

Authors: dr hab. inż. Robert Stala, E-mail: stala@agh.edu.pl; mgr inż. Adam Kawa, E-mail: adamkawa@agh.edu.pl; dr inż. Adam Penczek, E-mail: penczek@agh.edu.pl; dr inż. Zbigniew Waradzyn, E-mail: waradzyn@agh.edu.pl; dr inż. Andrzej Mondzik, E-mail: mondzik@agh.edu.pl, Akademia Górniczo-Hutnicza im. Stanisława Staszica w Krakowie, Katedra Energoelektroniki i Automatyki Systemów Przekształcania Energii, Al. Mickiewicza 30, 30-059 Kraków.

REFERENCES

- [1] On-Cheong Mak, Yue-Chung Wong, Ioinovici A.: Step-up DC power supply based on a switched-capacitor circuit, *Industrial Electronics, IEEE Transactions on*, vol.42 no.1, 90-97
- [2] Ioinovici A.: Switched-capacitor power electronics circuits, *Circuits and Systems Magazine, IEEE*, vol.1 no.3, 37-42
- [3] Yutian Lei, Pilawa-Podgurski, R.C.N.: A General Method for Analyzing Resonant and Soft-Charging Operation of Switched-Capacitor Converters, *Power Electronics, IEEE Transactions on*, vol.30 no.10, 5650-5664
- [4] Evzelman M., Ben-Yaakov S.: Average-Current-Based Conduction Losses Model of Switched Capacitor Converters, *Power Electronics, IEEE Transactions on*, vol.28 no.7, 3341-3352
- [5] Ben-Yaakov S.: On the Influence of Switch Resistances on Switched-Capacitor Converter Losses, *Industrial Electronics, IEEE Transactions on*, vol.59 no.1, 638-640
- [6] Alam M.K., Khan F.H.: Efficiency Characterization And Impedance Modeling Of A Multilevel Switched Capacitor Converter Using Pulse Dropping Switching Scheme, *Power Electronics, IEEE Transactions on*, vol. 29 no. 6, 3145-3158
- [7] Chun-Kit Cheung, Siew-Chong Tan, Tse C.K., Ioinovici A.: On Energy Efficiency of Switched-Capacitor Converters, *Power Electronics, IEEE Transactions on*, vol.28, no.2, Feb. 2013, 862-876
- [8] Cervera A., Evzelman M., Mordechai Peretz M., Ben-Yaakov S.: A High Efficiency Resonant Switched Capacitor Converter with Continuous Conversion Ratio, *Power Electronics, IEEE Transactions on*, vol. 30 no. 3, 1373-1382
- [9] Waradzyn Z., Stala R., Mondzik A., Penczek A., Skala A. Pirog S.: Efficiency Analysis of MOSFET-Based Air-Choke Resonant DC-DC Step-Up Switched-Capacitor Voltage Multipliers, *Industrial Electronics, IEEE Transactions on*, vol. 64, no. 11, Nov. 2017, 8728-8738
- [10] Waradzyn Z., Stala R., Mondzik A., Pirog S.: Switched Capacitor-Based Power Electronic Converter—Optimization of High Frequency Resonant Circuit Components, *Advanced Control of Electrical Drives and Power Electronic Converters, (Studies in Systems, Decision and Control)*, vol. 75, Cham, Switzerland: Springer, DOI 10.1007/978-3-319-45735-2_15, (2017), 361-378
- [11] Mondzik A., Waradzyn Z., Stala R., Penczek A., High efficiency switched capacitor voltage doubler with planar core-based resonant choke CPE-e 2016, 10th international conference on Compatibility, power electronics and power engineering. Bydgoszcz, Poland, 29 June–01 July, 2016, IEEE, cop. 2016. — Disk Flash. — e-ISBN: 978-1-4673-7292-3, 402–409
- [12] Kawa A., Stala R., Mondzik A., Pirog S., Penczek A.: High power thyristor-based DC-DC switched-capacitor voltage multipliers: Basic concept and novel derived topology with a reduced number of switches. *Power Electronics IEEE Transaction on*, 31(10), doi:10.1109/TPEL.2015.2505906, 6797–6813
- [13] Dong Cao, Fang Zheng Peng.: A family of zero current switching switched-capacitor dc-dc converters, *Applied Power Electronics Conference and Exposition (APEC)*, 2010 Twenty-Fifth Annual IEEE, vol. no. 1365,1372, 21-25
- [14] Ye Y., Cheng K.E., Liu J., Xu C.: A Family of Dual-Phase-Combined Zero-Current Switching Switched-Capacitor Converters, *Power Electronics, IEEE Transactions on*, vol. 29 no. 9, 4209-4218