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doi:10.15199/48.2018.04.06

Single VDCC-Based Electronically Tunable Voltage-Mode Second Order Universal Filter

***Abstract**. A design of second-order multiple-input single-output voltage-mode universal filter is presented in this paper. The proposed filter consists of single voltage differencing current conveyor (VDCC), single resistor and two capacitors. The new circuit provides five filter responses namely, low-pass, high-pass, band-pas, band-reject and all-pass functions. Each output filter response can be selected without the requirement of the matching condition and double gain amplifier for selecting all-pass function. The tuning of natural frequency and quality factor can be electronically done. The proposed circuit only uses single active element, which can be easily implemented as an integrated circuit. The MOS modeling of VDCC and Pspice simulation of proposed filter were carried out on TSMC 0.18 micrometer CMOS technology.*

Streszczenie.** Opisano uniwersalny filtr drugiego rzędu wykorzystujący układ VDCC (voltage differencing current conveyor). Częstotliwość graniczną filtru i jego dobroćmoga być dobierane elektronicznie. Zaproponowany filtr opracowano w technologii CMOS 0.18 mikrometra.* ***Uniwersalny strojony filtr drugiego rzędu wykorzystujący technologię VDCC

Keywords: VDCC; Universal biquad; Analog circuit; Electronic control; Active filter; commercially available IC.
Słowa kluczowe: układ VDCC, filtr, strojenie filtru..

Introduction

It is well-known fact that analog filter are important building blocks for signal processing that have variety of applications in fields of communication, sound system, instrumentation, control system etc [1]. A biquad filter which provides several filter responses in the same circuit topology is well-known as universal or multifunction filter. [2-3]. The number of input and output of the universal filter is used to classify the sort of universal filter. There are single-input multiple-output (SIMO), multiple-input multiple-output (MIMO) and multiple-input single-output (MISO) filter. The MISO filter is one of the universal filter which has been attracted significant research attention [4]. Most of MISO universal filters use digital method to select the output filter response. So, the way to selection of the output filer response should be done without comment matching condition.

The design of electronic circuit in analog signal processing has gone in the use of active building block [5-9]. Especially, the electronically tunable active building blocks have attracted significant research attention since analog circuits using electronically tunable active building block give more fine-tuning than adjusting the value of passive device. The voltage differencing current conveyors (VDCC) [10] is a recently reported versatile active building block used in the realization of analog signal processing circuits. A very significant advantage of using VDCCs in analog circuit design is that it is able electronic controllability.

Literature review shows that, a number of the analog circuits using VDCC as active element have been found for examples, inductance simulator [10-11], capacitance multiplier [12-13], versatile passive element simulator [14-15], square and triangular wave generator [16], sinusoidal oscillator [6, 13, 17-20], first order allpass filter [21], ladder filter [22] etc. The VDCC based universal filters have been proposed in [23-26]. The three-inputs single-output current-mode universal filter with five filter responses was proposed in [23]. It consists of single VDCC, single grounded resister and two grounded capacitors. The natural frequency and quality factor are electronically tuned. The impedance at output current node exhibits high which is convenient to cascade in current-mode circuit without the use of current buffer. However, this filter requires three output w terminals of VDCC. Also, for all-pass response, the double gain amplifier is required. The current-mode reconnection-less reconfigurable filter was proposed in [24]. It consists of single VDCC, single dual output current amplifier, single resister and two grounded capacitors. The natural frequency and quality factor are electronically tuned. The impedance at input current node exhibits low and the impedance at output current node exhibits high which is convenient to cascade in current-mode circuit without the use of current buffer. However, this filter can provide only three filter responses (LP, HP and BP). The single-input four-outputs voltage-mode filter was proposed in [25]. It consists of single VDCC, two resistors and two capacitors. The natural frequency and quality factor are electronically tuned. Moreover, the tune of quality factor can be done without affecting the natural frequency. However, a unity gain difference amplifier is needed to create LP and AP filter responses. The three-inputs single-output (TISO) voltage-mode filter and single-input dual-output (SIDO) voltage-mode filters were presented in [26]. The TISO filter with five filter responses consists of single VDCC, single resistor and two capacitors. The SIDO filters with three filter responses (HP, BP and LP) consist of single VDCC, two resistors and two capacitors. The natural frequency and quality factor for both TISO and SIDO are electronically tuned. Moreover, the tune of quality factor for SIDO filter can be done without affecting the natural frequency.

In this paper, a new structure for realizing second-order voltage-mode three-inputs single-output universal filter using VDCC is proposed. The proposed circuit can realize second-order low-pass, high-pass, band-pass, band-reject and all-pass filter characteristics in the same circuit topology. The use of the VDCC in the circuit as active elements provides electronic tunability. The presented filter does not require component matching conditions and double gain amplifier, which is ideal for digital controllability. The proposed filter was simulated with Pspice program with standard 0.18 μm TSMC CMOS process parameters are given to confirm the theory.

Theory and Principle

Basic Concept of VDCC

The active device called VDCC is used to design the proposed filter. This active building block was proposed in [10]. It gathers the advantages of the operational transconductance amplifier (OTA) and the second

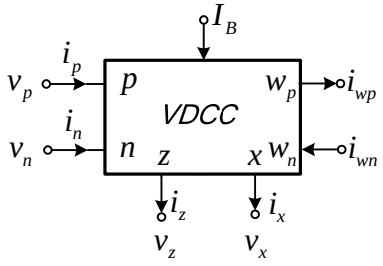
generation current conveyor (CCII) such as: electronic controllability, high input impedance, low output impedance (x terminal), high output impedance (z and w terminals), high accuracy and large bandwidth. The VDCC whose electrical symbol is shown in Figure 1(a) has six terminals. Using standard notation, the terminal relations of the VDCC can be characterized by the following hybrid matrix equation.

$$(1)\qquad \begin{pmatrix} i_n \\ i_p \\ i_z \\ v_x \\ i_{wp} \\ i_{wn} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{pmatrix} \begin{pmatrix} v_p \\ v_n \\ v_z \\ i_x \end{pmatrix}.$$

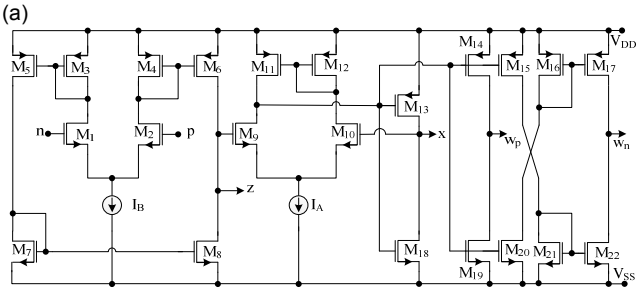
where g_m is the transconductance gain. The VDCC can be constructed from CMOS technology as shown in Figure 1(b). The g_m for this construction is given as

$$(2)\qquad g_m = \sqrt{\mu_n C_{OX} (W/L) I_B}\ .$$

I_B is the input bias current to control gm and is used to control the gm. μ is the effective channel mobility. C_{ox} is the gate oxide capacitance per unit area. W is the channel width and L is the channel length.



(a)



(b)

Fig.1. VDCC (a) Symbol (b) CMOS internal construction

Proposed Voltage-Mode Filter

The proposed filter is illustrated in Fig. 2. It consists of single VDCC, single resistor and two capacitors. There are three input voltages, v_{in1}, v_{in2} and v_{in3}. The single output voltage is v_{out}. Routine analysis of the proposed filter using Eq. (1) yields the following output voltage equation

$$(3)\qquad v_{out} = \frac{s^2 v_{in2} + s\frac{g_m}{C_2} v_{in1} + \frac{g_m}{R} v_{in3}}{s^2 + s\frac{g_m}{C_2} + \frac{g_m}{C_1 C_2 R}}.$$

According to Eq. (3), the natural frequency is given as

$$(4)\qquad \omega_0 = \sqrt{\frac{g_m}{C_1 C_2 R}},$$

Subsequently, the quality factor is given as

$$(5)\qquad Q = \sqrt{\frac{C_2}{C_1 g_m R}}.$$

It is evident from Eqs. (4) and (5) that the control of natural frequency and quality factor can be electronically done via g_m.

From Eq. (3), the derivation of non-inverting five filter responses can be done as follows:

- The high-pass filter response can be obtained by applying the input voltage to node v_{in2} while nodes v_{in1} and v_{in3} are grounded.
- The band-pass filter response can be obtained by applying the input voltage to node v_{in1} while nodes v_{in2} and v_{in3} are grounded.
- The low-pass filter response can be obtained by applying the input voltage to node v_{in3} while nodes v_{in1} and v_{in2} are grounded.
- The band-reject filter response can be obtained by applying the input voltage to nodes v_{in2} and v_{in3} while node v_{in1} is grounded.
- The all-pass filter response can be obtained by applying the input voltage to nodes v_{in2}, v_{in3} and applying the inverting input voltage to node v_{in1}.

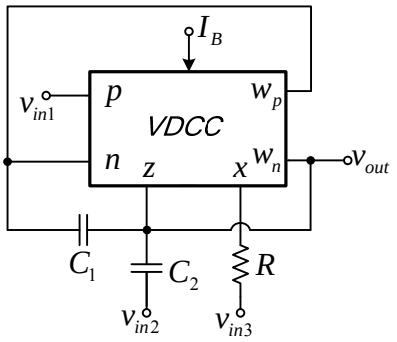


Fig.2. Proposed filter

Non-Ideal Analysis

In practically, the influent of current/voltage tracking errors in VDCC will affect the performances of the proposed filter. For non-ideal case, the relationship of the terminal voltages and currents of VDCC can be rewritten as:

$$(6)\qquad \begin{pmatrix} i_n \\ i_p \\ i_z \\ v_x \\ i_{wp} \\ i_{wn} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 \\ 0 & 0 & \beta & 0 \\ 0 & 0 & 0 & \alpha_p \\ 0 & 0 & 0 & -\alpha_n \end{pmatrix} \begin{pmatrix} v_p \\ v_n \\ v_z \\ i_x \end{pmatrix}.$$

where β is the voltage tracking error from x to z terminal, α_p is the current tracking error from x to w_p terminal and α_n is the current tracking error from x to w_n terminal. Taking the non-ideal parameters into account, the output voltage of the circuit in Fig. 2 is obtained as

$$(7)\qquad v_{out} = \frac{s^2 v_{in2} + s\frac{g_m}{C_2} v_{in1} + \frac{1}{C_1 C_2}\left(\alpha_n s\frac{C_1}{R} - \alpha_p s\frac{C_1}{R} + \alpha_p \frac{g_m}{R}\right) v_{in3}}{s^2 + s\left[\frac{g_m}{C_2} + \frac{\beta}{C_1 C_2 R}(\alpha_n - \alpha_p)\right] + \alpha_p \beta \frac{g_m}{C_1 C_2 R}},$$

From Eq. (7), the natural frequency is given as

$$(8)\quad \omega_0 = \sqrt{\alpha_p \beta \frac{g_m}{C_1 C_2 R}}\,.$$

Subsequently, the quality factor is given as

$$(9)\quad Q = \frac{1}{C_1 g_m + \frac{\beta}{R}\left(\alpha_n - \alpha_p\right)} \sqrt{\alpha_p \beta \frac{C_1 C_2}{g_m R}}\,.$$

Simulation Results

To evaluate the proposed voltage-mode universal filter in Figure 2, the VDCC in Figure 1(b) was designed and simulated using CMOS TSMC 0.18 μm model (level 7) [27]. Table 1 shows the aspect ratios of various transistors of VDCC. The proposed circuit was supplied with symmetrical ±0.9 VDC, the DC bias current was set as I_B = 50μA. The simulated properties of VDCC were g_m=281μA/V, β=0.999, α_p=0.996, and α_n=0.943. The passive component values were chosen as R = 4.7 kΩ and C_1 = C_2 = 40 nF. The total power dissipation was demonstrated to be 0.912 mW. Simulated result for low-pass, high-pass, band-pass and band-reject response built with the filter in Fig. 2 is shown in Fig. 3. The obtained natural frequency and quality factor are 1MHz and 0.851 as compared with the theoretical values of 0.973 MHz and 0.87, respectively, thus giving rise to deviations of 2.7% and 2.18%, respectively. This deviation suffers from the voltage/current tracking error and parasitic elements as analyzed in Eqs. (8) and (9). The simulated gain and phase of AP versus frequency response is shown in Fig. 4. It is found that the phase response changes from 0 to -360 while the magnitude frequency response is constant for all frequencies. The results in Fig. 3 and 4 confirm that the proposed circuit can provide five filter responses with the same circuit topology. The simulated input and output waveform in time domain for band-pass function is illustrated in Fig. 5 when the sinusoidal signal with 1MHz and 200 mVp was applied as input voltage. It is found that the magnitude of output voltage is equal to input voltage. The total harmonic distortion (THD) of the band-pass filter configuration is 0.31%. Fig. 6 shows dynamic range and linearity performance of the low-pass filter configuration. Pretty much increasing of the input voltage makes output characteristic deviate from ideal behavior. THD analysis of the proposed voltage-mode band-pass filter given in Fig. 7 was performed at 1 MHz for various sinusoidal peak input voltages. To demonstrate the proposed filter's center frequency depending on the tolerance of resistor and capacitors, the Monte Carlo analyse of the band-pass filter configuration with 5% Gauss deviation was performed for 200 simulation runs. According to Monte Carlo simulations, the obtained minimum and maximum frequency are 1.095 MHz and 1.234 MHz respectively and standard deviation is 25.230 kHz as illustrated in Fig. 8. It is shown that the proposed filter has low sensitivity to the passive elements.

Table 1. W/L of the MOSFET in the VDCC

Transistor	W (μm)	L (μm)
M1-M4	3.6	1.8
M5-M6	7.2	1.8
M7-M8	2.4	1.8
M9-M10	3.06	0.72
M11-M12	9	0.72
M13-M17	14.4	0.72
M18-M22	0.72	0.72

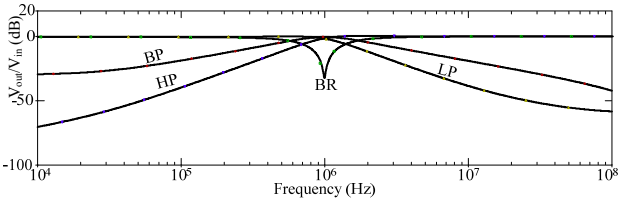


Fig.3. Simulated gain response for low-pass, high-pass, band-pass and band-reject filters.

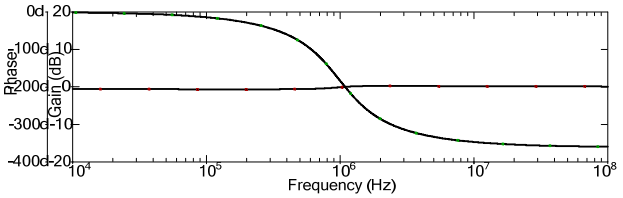


Fig.4. Simulated gain and response for all-pass filter

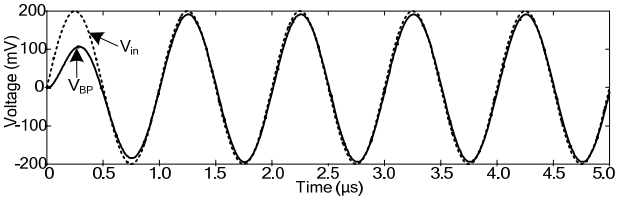


Fig.5. Transient analysis of the band-pass filter for 200 mVp input voltage at 1 MHz

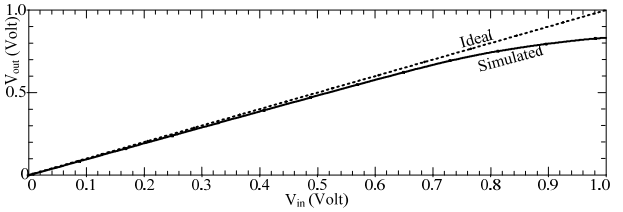


Fig.6. Linearity of the low-pass filter versus input voltage

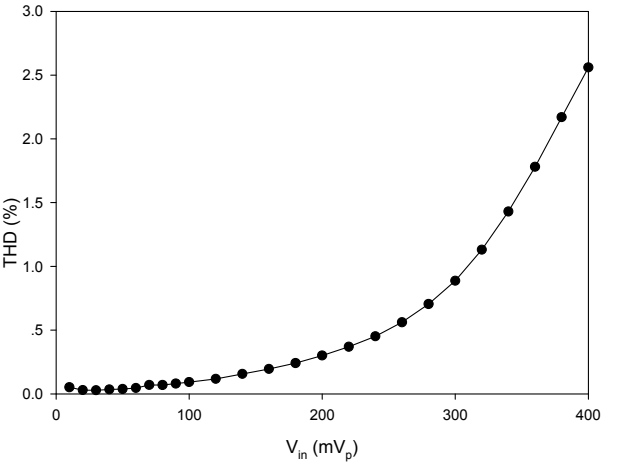


Fig.7. THD against peak value of the applied sinusoidal signal at 1 MHz frequency

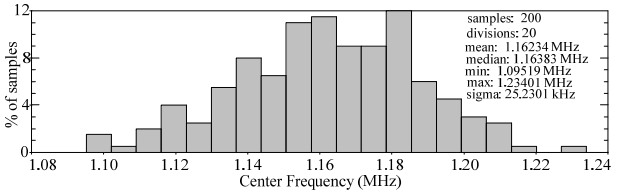


Fig.8. Monte-Carlo histogram for the band-pass filter.

Conclusions

A new electronically tunable filter with three input voltages and single output voltage is proposed in this paper. The core filter designed in Fig. 2 employs only single VDCC

along with single resistor and two capacitors. Therefore, the proposed filter topology has a very simple structure. The proposed filter employing only single active element realizes all the five standard types of biquad functions, namely low-pass, high-pass, band-pass, band-reject and all-pass, filter from the same configuration. The selection of output function responses can be done without any component matching condition and without the requirement of additional double gain amplifier. Pspice simulations have been carried out validating the theoretical predictions. However, the input nodes v_{in2} and v_{in3} are not high impedance and the output node is not low impedance which is required the voltage buffer for cascading.

Acknowledgments. This work is funded by Suan Sunandha Rajabhat University.

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