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Influence of Layer Stackup and Decoupling Capacitors Placement on Power Delivery Network Impedance

Abstract. *This paper discuses frequency properties of power delivery network impedance in multi-layer printed circuit boards. The influence of layer stackup and decoupling capacitors placement are illustrated as result of full-wave analysis performed by means of HyperLynx Power Integrity simulation software.*

Streszczenie. *W artykule analizowano impedancję obwodów zasilania w wielowarstwowych obwodach drukowanych. Omówiono wpływ położenia płaszczyzn odniesienia oraz rozmieszczenia kondensatorów odsprzęgających na przebiegi częstotliwościowe impedancji widzianej na zaciskach układu cyfrowego. Wszystkie symulacje wykonano za pomocą programu HyperLynx PI.(**Analiza wpływu rozmieszczenia płaszczyzn odniesienia i kondensatorów odsprzęgających na impedancję obwodów zasilania wielowarstwowych obwodów drukowanych**).*

Keywords: power delivery network, printed circuit board.
Słowa kluczowe: obwody zasilania, obwody drukowane.

Introduction

Power delivery network (PDN) is nowadays one of the crucial issue of multi-layer printed circuit boards (PCB) design process [1]-[3]. As the operating frequency increases and supply voltages decrease, achieving of very low impedance of PDN in wide frequency band becomes the fundamental aspect of signal integrity and electromagnetic compatibility requirements. Obviously, the most important task of PDN is to keep the voltage across power pins of integrated circuits (IC) stable with possible low level of ripple noise for given IC current fluctuations.

The PDN of typical circuit consists of voltage regulator module (VRM), bulk and decoupling capacitors and all interconnects between VRM and the pads on the IC chips. The impedance of PDN can be relatively easy to control for lower frequencies, where VRM and bulk capacitors dominates the performance of power network. When the frequency increases the PDN properties are determined by both decoupling capacitors (their parameters, placement and mounting techniques) and impedance of the PCB power planes (layer stackup) which makes the PDN impedance variations harder to predict [4]-[6]. For the highest frequencies where self-resonances of PCB cavities appear, the PDN impedance can be effectively simulated by using of full-wave 3D solvers only [1].

The main purpose of this paper is to analyze and discuss frequency variation of PDN impedance for different configurations of PCB stackups and decoupling capacitors placement and mounting techniques. All numerical calculations are performed by commercial software HyperLynx of Mentor Graphics [8]. The purpose of the article is mainly educational. The paper is addressed for those who design of multi-layer printed circuit boards. The results are intended to systematize knowledge and to deal with myths about the influence of decoupling capacitors on impedance of power delivery network.

Impedance of power planes

Contemporary printed circuits are multilayer structures that contain signal layers and power planes, as it is depicted in Fig. 1a. The thickness of applied dielectrics between the layers and the role of the layers is primarily due to the need to meet the electrical requirements – required characteristic impedance on the signal layers and correspondingly low impedance of the power delivery network. The impedance of power planes is affected by their actual shape and dimensions and the thickness and electrical properties of the dielectric. Typical frequency behaviour of the impedance is presented in Fig. 1b for rectangle FR4 laminate with dimensions 20 cm x 15 cm and the planes distance of 5 mils. For the lowest frequencies the planes behaves roughly as parallel-plate capacitor and its impedance decreases with frequency. The spreading inductance of the plates is responsible for series resonances observed in analyzed particular case for frequency about 90 MHz. For higher frequencies the power planes behave as resonance cavity with modal resonant frequencies (*m*,*n*) given as [7]

$$f_{mn} = \frac{c}{2\sqrt{\varepsilon_r}}\sqrt{\left(\frac{m}{a}\right)^2 + \left(\frac{n}{b}\right)^2} \tag{1}$$

where *a* and *b* are power planes dimensions, *m* and *n* are integers (0, 1, 2, 3 etc.) and correspond to the various modes of resonance, whereas ε_r is a relative permittivity of the dielectric.

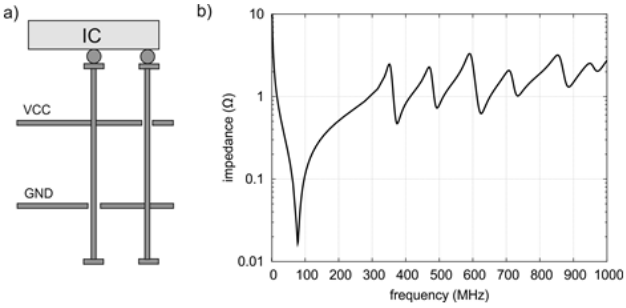

Fig. 1. A 4-layer stackup (a) and frequency behaviour of power planes (b).

Four-layer stackup

As an example, the PDN impedances Z_{PDN} are calculated at power pins of IC placed on top of multi-layer PCBs with dimensions 20 cm x 15 cm. In all analyzed cases, the IC is placed at point *P(5,3.5)* with respect to left bottom corner of the PCB. As a substrate standard FR4 laminate with permittivity of 4.3 is used. The PDN impedance is decreased by using 220 nF decoupling capacitors (C_{dec}) with 0603 size and equivalent series resistance ESR=21 mΩ. In analysis the series RLC equivalent model of capacitor is used where L includes capacitor self-inductance and mounting inductance calculated individually by HyperLynx for each configuration.

A. Influence of capacitor mounting inductance

The first analyzed configuration of stackup with total thickness 55 mils is presented in Fig. 2. The PCB consists of four layers: top and bottom signal layers and two middle layers as power planes for ground and voltage supply. The PDN impedance can be effectively reduced by decoupling capacitors placed near the IC (see Fig. 2). At the beginning it is assumed that the IC and capacitor are placed at top layer and connected to the power planes by through vias. Additionally, the capacitor pads are connected with the vias by traces with length *l* and width *w*. For almost all structures in this paper it is assumed that *l*=8 mils and *w*=10 mils. The structure is analyzed for two configurations of distances between layers: a) h_1=h_3=10 mils, h_2=35 mils; b) h_1=h_3=25 mils, h_2=5 mils. The PDN impedance versus frequency for h_2=35 mils is presented in Fig. 3. The figure shows the results for circuit without de-coupling capacitor and with one capacitor placed at different distances d to the IC. Adequate results for the second configuration (h_2=5 mils) are presented in Fig. 4. As one can observe, the impedance of the power planes can be effectively modelled by a lumped capacitor up to about 80 MHz (see results labelled 'without cap'). Above this frequency the resonant frequencies are observed - the planes form a cavity with modal resonant frequencies depending on dielectric constant of the material in the cavity and dimensions of the board. As expected, location of the resonant frequencies in Fig. 3 and Fig. 4 are the same, however the amplitude of the impedance strongly depends on the power planes separation. It means that Z_{PDN} at higher frequencies (above 100 MHz in this particular case) can be reduced by decreasing distance between pair of power planes. On the other hand, at lower frequencies, Z_{PDN} can be effectively reduced by decoupling capacitors.

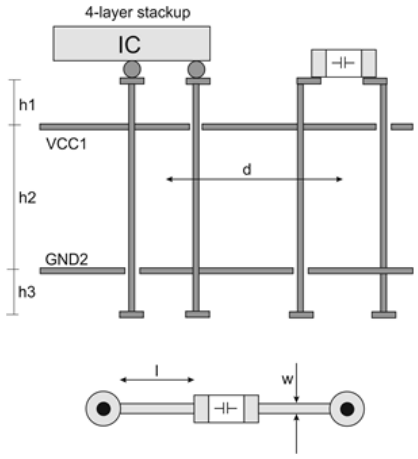

Fig. 2.Exemplary 4-layer stackup.

Increasing the distance between C_{dec} and IC causes rise of mounting inductance of the capacitor. It leads to decreasing the resonance frequency (f_{res}) of the capacitor and to increasing the Z_{PDN} above f_{res}. This effect can be reduced by decreasing distance between pair of power planes (see Fig. 4). For the second configuration (h_2=5 mils) the spreading inductance, i.e. inductance of the cavity, is significantly smaller and as a consequence the distance between C_{dec} and IC has less importance.

Fig. 5 shows the Z_{PDN} for different width (*w*) and length (*l*) of the track between decoupling capacitor pads and vias. The analysis is performed for C_{dec} placed very close to the IC (*d*=0 cm) and four layers stuckup with 35 mils between planes. Results show that *l* has a significant influence on the f_{res} and Z_{PDN} between f_{res} and cavity resonances. The effect of the trace width is less observable, however design rules recommend using traces as short and as wide as possible.

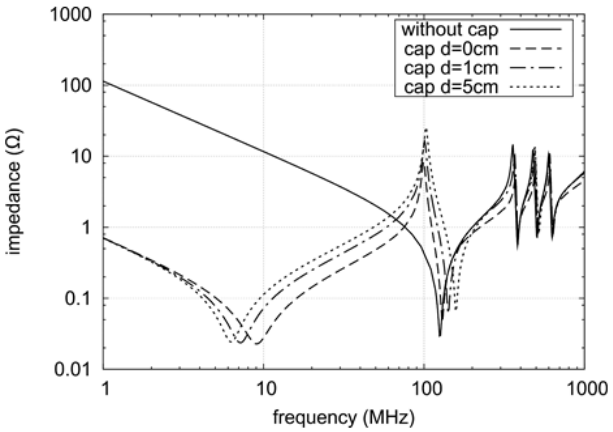

Fig. 3. PDN impedance for different distances between IC and decoupling capacitor (four layers stackup with 35 mils between planes).

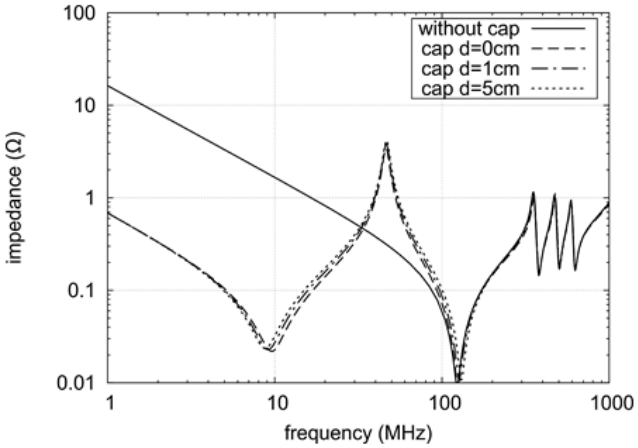

Fig. 4. PDN impedance for different distances between IC and decoupling capacitor (four layers stackup with 5 mils between planes).

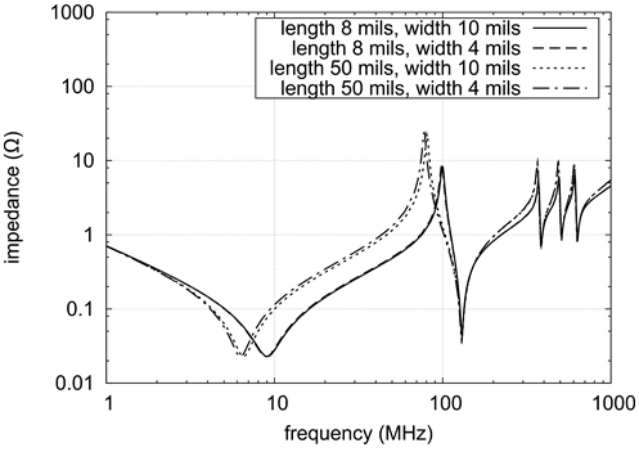

Fig. 5. PDN impedance for different capacitor mounting (capacitor close to the IC, four layers stackup with 35 mils between planes).

B. Increasing the number of capacitors

Fig. 6 shows the Z_{PDN} for 4-layers board with two decoupling capacitors. The first capacitor is placed very close to the IC (*d*=0 cm) and its localization is fixed during the tests. Figures show influence of the distance between second capacitor and IC in the range from 0 cm to 10 cm. It is obvious that adding the another C_{dec} decreases the Z_{PDN} (compare Fig. 6 and Fig. 3). However if the second capacitor is mounted further from IC, it has higher mounting

inductance and lower f_{res}. In this case one can observe an additional parallel resonance located between self-resonances of each C_{dec}. This effect can be reduced again by using stackup with thinner dielectric between power planes.

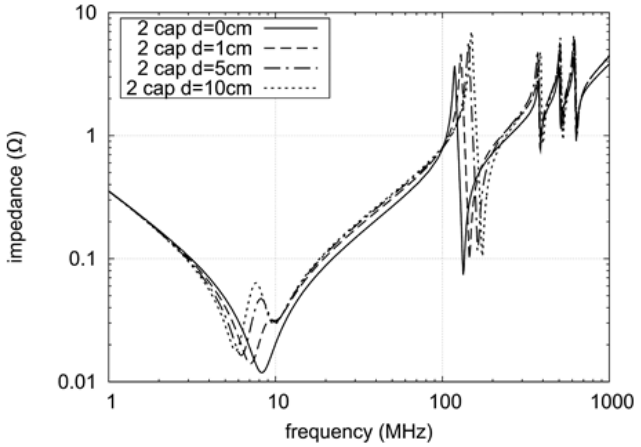

Fig. 6. PDN impedance for different distances between IC and second decoupling capacitor (one capacitor close to the IC, four layers stackup with 35 mils between planes).

Six- and eight-layer stackups

The next analyzed configurations of stackups are presented in Fig. 7. The total thickness of all PCBs is 50 mils. The first 6-layer stackup has only one pair of power planes (VCC1, GND1) placed at distance of 30 mils. The second and third analyzed 8-layer stackups have two pairs of power planes (VCC1-GND1, VCC2-GND1) separated by the distance of 5 mils or 1 mils, respectively. The PDN impedance versus frequency for the stackups is presented in Fig. 8. The results show that stackup significantly affects the impedance at IC power pins. Increasing the number of power planes or decreasing the distance between them enables to reduce of the Z_{PDN} in whole frequency range.

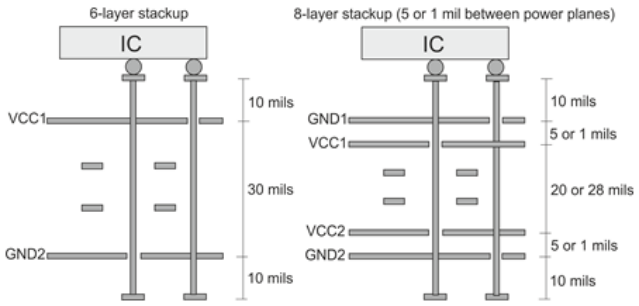

Fig. 7.Exemplary 6-layer and 8-layer stackup).

A. Top and bottom mounted capacitors (six-layer stackup)

The next interesting question is: should the capacitors be placed at the top or bottom side of the PCB for maximum effect? Fig. 9 shows Z_{PDN} for 6-layer stackup and few placements of the C_{dec}. In this structure the distance between power planes is relatively large (30 mils) and it is assumed that the IC is placed at the top layer. For three cases the C_{dec} is also placed at the top but for different distances (d) from IC. The last configuration is for C_{dec} placed at bottom layer directly under IC. It is clear from the Fig. 9, that capacitor mounted very close to IC at the top or bottom layer gives the same effect. Z_{PDN} increases with the distance between IC and C_{dec}. For stackups with a larger spacing between planes, the C_{dec} should be always placed as close as possible to IC. It means that if signal lines routed with a high density at top layer do not allow place the capacitor close to the IC, the capacitor should be placed on the bottom layer under IC.

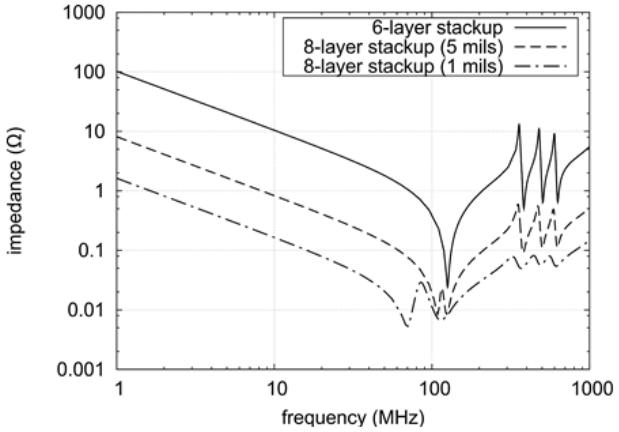

Fig. 8. PDN impedance for the three analyzed layer stackups.

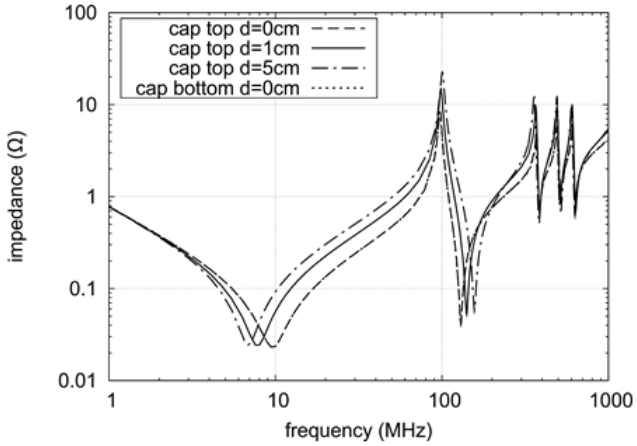

Fig. 9. PDN impedance for different capacitor placement (6-layer stackup).

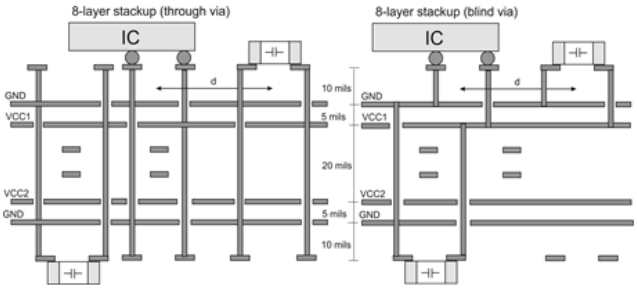

Fig. 10. Capacitor placement for 8-layer stackup.

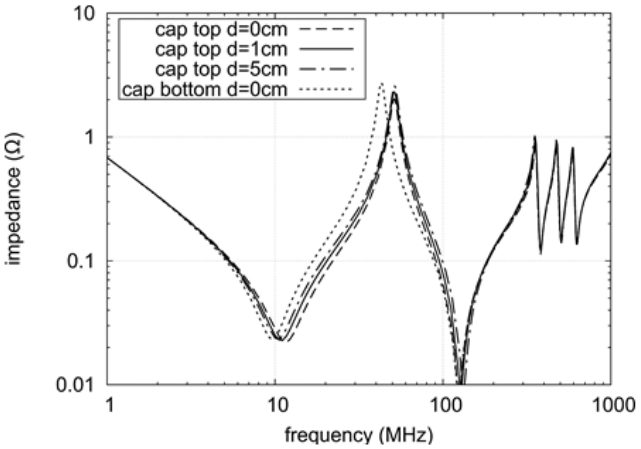

Fig. 11. PDN impedance for different capacitor placement (8-layer stackup, through via).

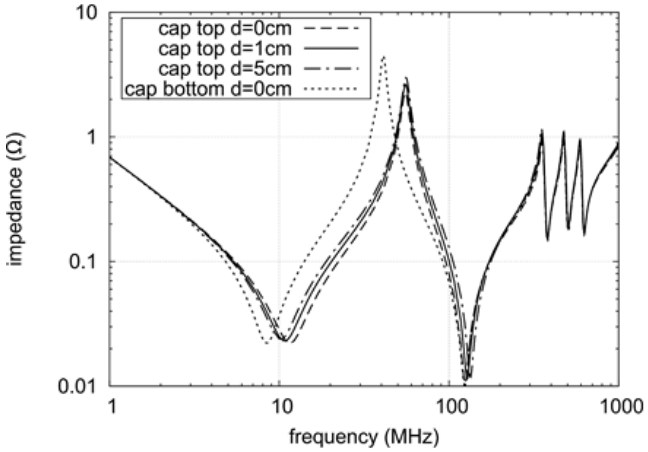

Fig. 12. PDN impedance for different capacitor placement (8-layer stackup, blind via).

B. Top and bottom mounted capacitors (eight-layer stackup)

The last structures under consideration are presented in Fig. 10. The 8-layer stackups with 5 mils spacing between planes are analyzed for different capacitor placement (top or bottom). It is assumed that IC located at the top layer is connected to power plane VCC1 and GND. Fig. 11 and 12 show results for decoupling capacitor connected to power planes by through and blind via, respectively. For these structures (small distance between planes) the C_{dec} should be rather placed at the same layer as IC. When the through via are used the capacitor placed at bottom layer offers similar effect as C_{dec} placed at top. However for blind via, the C_{dec} placed at bottom gives noticeably worse results.

Conclusions

Influence of layer stackup (i.e. distances between layers) and decoupling capacitors placement on PDN impedance is presented in this paper. The exemplary PCBs with four- six- and eight-layer stackups are analyzed by means of HyperLynx Power Integrity simulation software. Generally decoupling capacitor should be placed as close as possible to the IC and traces between C_{dec} pads and vias should be as short and as wide as possible. It is also shown that for stackups with relatively low spacing between power planes the distance between C_{dec} and IC has less importance. For those structures the inductance of vias dominates spreading inductance of power planes. In consequence, IC and C_{dec} should be placed on same layer (top or bottom, whichever is closest to the power planes).

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