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Multiple output second-generation current conveyor utilizing high frequency output stage

Abstract. In this paper a multiple output second-generation current conveyor (MOCCII) is presented. The main advantage of the proposed general circuit architecture over a typical structure, well known in the literature, is the use of a high passband multiple output current amplifier block instead of cascaded current mirrors. It gives similar frequency responses for all the outputs of the current conveyor and also maintains simplicity of the whole circuit. As an example, a detailed design of the MOCCII in 350nm CMOS process is presented. The conveyor consumes only 135μA from 3.3V power supply and exhibits over 120MHz of 3dB passbands for both positive and negative outputs.

*Streszczenie. W artykule przedstawiono koncepcję układową wielowyjściowego konwejora prądowego drugiej generacji (ang. MOCCII). Jej główną zaletą w stosunku do dotychczas prezentowanych w literaturze jest zastosowanie szerokopasmowego wielowyjściowego wzmacniacza prądowego w miejsce kaskadowych luster prądowych. Zastosowanie tego wzmacniacza daje dobre i podobne właściwości częstotliwościowe wszystkich wyjść konwejora zachowując równocześnie prostotę układu. Jako przykład aplikacyjny przedstawiono szczegółowy projekt układu MOCCII w technologii AMS CMOS 350 nm. Finalny konwejor zużywa tylko 135 μA prądu ze źródła zasilania 3,3 V i ma pasmo 3 dB o częstotliwościach ponad 120 MHz zarówno dla wyjść dodatnich jak i ujemnych. (**Wielowyjściowy konwejor prądowy drugiej generacji z wykorzystaniem szerokopasmowego stopnia wyjściowego**).*

Keywords: current conveyor, current amplifier, multiple output second-generation current conveyor.
Słowa kluczowe: konwejor prądowy, wzmacniacz prądowy, wielowyjściowy konwejor prądowy drugiej generacji

Introduction

Since its introduction [1] current conveyors have been widely used in analogue signal processing applications. To date, many variations of current conveyors have been presented, both with positive and negative current gains, of generations identified from I to III and also having multiple outputs [2-6]. In this paper, a multiple output second-generation current conveyor (MOCCII) is presented. It has Y and X inputs and 3 outputs: Z_P, Z_{M1} and Z_{M2}. Output Z_P is the positive one while Z_{M1} and Z_{M2} are two independent negative outputs. The MOCCII graphical symbol and terminals voltages and currents are defined in Fig. 1. A matrix equation describing ideal electrical properties is given in by (1).

$$(1) \quad \begin{bmatrix} i_Y \\ v_X \\ i_{ZP} \\ i_{ZM1} \\ i_{ZM2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_Y \\ i_X \\ i_{ZP} \\ i_{ZM1} \\ i_{ZM2} \end{bmatrix}$$

From (1) it is obvious that MOCCII element is equivalent to 2 negative and 1 positive second-generation current conveyors (CCII) having common Y and X terminals. The main advantage of the below proposed structure over the previously presented one [3-5] is the simultaneous realisation of 3 independent outputs while also all of the outputs exhibit similar and good frequency responses. Such properties are usually not possible using the current mirror cascading technique for the negative output generation.
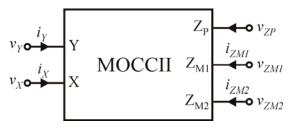

Fig.1. Graphical symbol of proposed multiple output second-generation current conveyor (MOCCII) block

Proposed architecture of the MOCCII

The architecture of the proposed MOCCII is presented in Fig. 2. It consists of an operational amplifier (OA), and as the output stage a current amplifier reported in [7] is employed. Due to the negative feedback loop in the signal path (which starts at X terminal and then goes through OA and inverting M_{N1} device), voltages at Y and X terminals should be of the same value. In a real circuit the equality of voltages at Y and X terminals depends mainly on mismatches of devices in the input stage of OA, and thus, this subcircuit should be designed carefully using relatively big devices and high overdrive voltage [8]. Simultaneously, any current going via X terminal is the input current flowing to the current amplifier stage which is marked in Fig. 2 with a dashed line. That is why any current flowing to X terminal is also amplified and moved to output terminals Z_P, Z_{M1} and Z_{M2}. It should be noted that according to [7], if all M_{N1}-M_{N4} devices have identical dimensions, then, ideally, neglecting resistances of bias current sources I_{BIAS} and $4I_{BIAS}$, current gains to output terminals Z_P, Z_{M1} and Z_{M2} equal -1, 1 and 1, respectively. In a real circuit, which employs cascoded MOS current sources, those current gains absolute values are very close but not exactly equal to 1. It is also worth noticing that according to [7], current gains to all outputs have similar frequency responses.

MOCCII implementation example

As a design example, MOCCII using the architecture from Fig. 2 is presented in Fig. 3. The OA is built using a single pMOS differential pair (devices M_{OA1} - M_{OA2}) with nMOS current mirror as load (devices M_{OA3} - M_{OA4}). Transistor M_{OA5} is the current source for the input differential pair and its dimensions were chosen to get the current of about 4μA. Devices M_{N1} - M_{N4} constitute the core of the current amplifier. Bias current source $4I_{BIAS}$ is built with the use of a low voltage cascode current source formed by devices M_{NB1} - M_{NB4}. The diode connected devices M_{NB5}, M_{PB11} and M_{PB12} generates constant voltage feed to the gates of M_{NB1} and M_{NB3}, which is necessary for the proper operation of the low voltage cascode. Similarly, devices M_{PB1} - M_{PB10}, M_{PB13}, M_{NB6} and M_{NB7} form four low voltage cascode current sources I_{BIAS}. Dimensions of the current sources devices were chosen to obtain bias current I_{BIAS} = 25μA. Together with M_{N1} device from the output

current amplifier, a loop gain above 10k [V/V] is obtained, which is a sufficiently high value to obtain near unity voltage gain seen from Y to X terminals. Capacitor C_{COMP} of value 32fF is necessary to maintain stability of the internal negative feedback loop.
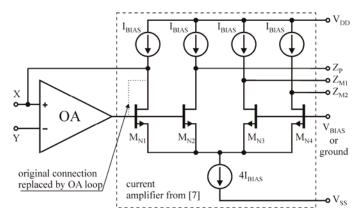

Fig.2. General architecture of the multiple output second-generation current conveyor. Instead of diode connection of the device MN1 (dotted line) operational amplifier (OA) is employed in the negative feedback loop. Dashed line surrounds employed current amplifier presented in [7]
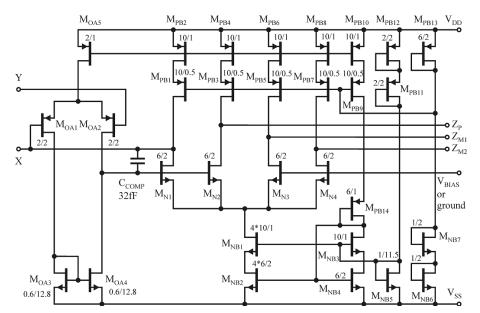

Fig.3. Detailed scheme of MOCCII designed in AMS 350nm CMOS technology. Transistor dimensions are in μm, format is as follows: optional multiplier*width/length

Table 1. Simulated parameters of the MOCCII from Fig. 3 with input voltage applied to Y terminal and resistance $R_X = 100k\Omega$ connected from X to ground. Output currents were tested at shorts to the signal ground

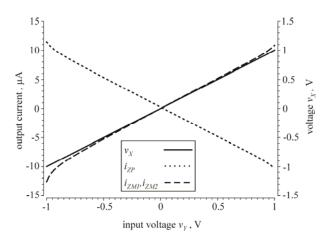| Parameter name	Unit	Value
Power supply voltage $V_{DD} - V_{SS}$	(V)	3.3
Current consumption	(μA)	135
Voltage gain from Y to X	(V/V)	0.999992
3dB passband of Y to X gain	(MHz)	45.9
Transconductance from Y to Z_P @ Rx=100kΩ	(μS)	10.39
3dB passband of Y to Z_P transconductance	(MHz)	136.2
Transconductance from Y to Z_{M1} and Z_{M1} @ Rx=100kΩ	(μS)	-10.13
3dB passband of Y to Z_{M1} and Z_{M2} transconductance	(MHz)	126.2
Resistance of X terminal	(Ω)	58.4
Resistance of Z_P terminal	(MΩ)	2.55
Resistance of Z_{M1} and Z_{M2} terminals	(MΩ)	3.98
Equivalent Y input capacitance	(fF)	4.6
Equivalent Z_P, Z_{M1} and Z_{M2} capacitance	(fF)	17.3
Noise at Z_P output @1MHz	($pA/\sqrt{Hz}$)	2.89
Noise at Z_{PM1} and outputs Z_{PM2} @1MHz	($pA/\sqrt{Hz}$)	4.74

Fig.4. Simulated DC transfer characteristics of the MOCCII from Fig. 3, as input voltage source feed to Y terminal was used, X terminal was connected through 100kΩ resistor to the ground, output currents were tested at shorts to the ground
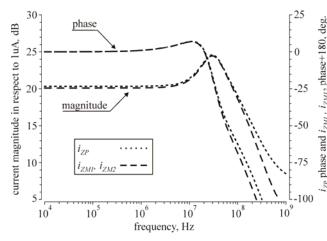

Fig.5. Simulated small signal frequency responses of the MOCCII from Fig. 3, as input voltage source feed to Y terminal was used, X terminal was connected through 100kΩ resistor to the ground, output currents were tested at shorts to the ground

MOCCII circuit was designed and simulated with Cadence Virtuoso IC6.1.5 environment using AMS 350nm CMOS technology kit. Simulated results are given in Table 1, in Fig. 4 and in Fig. 5. Simulations were carried out with the connection of Y terminal to the voltage signal source while X terminal was connected via the resistance of 100kΩ

to the signal ground. Output currents were measured at circuit shorts of ZP, ZM1 and ZM2 terminals to the signal ground.

Conclusion

The multiple output second-generation current conveyor (MOCCII) is presented. The main advantage of the proposed general circuit architecture over the one known in the literature is the use of the high frequency multiple output current amplifier block from [7]. It results in similar frequency responses for all the outputs and also maintains circuit simplicity. As an example a detailed design of the MOCCII in 350nm CMOS AMS process is presented. MOCCII consumes only 135μA from 3.3V power supply and exhibits over 120MHz of 3dB passbands for all positive and negative outputs. The presented MOCCII amplifier can be easily used in signal conditioning and filtering application. Available multiple outputs are also of great value and can considerably simplify a target system [6].

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