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Experimental Research of the Analog Multiplier based on Field-effect Transistors

Abstract. *The article presents the results of mathematical analysis and experimental studies of analog multiplier based on field-effect transistors. It is established that such multiplier has a wider dynamic range of input signals and a low level of output signal combinational components.*

Streszczenie. *Artykuł prezentuje wyniki analizy matematycznej i doświadczeń eksperymentalnych mnożnika analogowego opartego na tranzystorach polowych. Ustalono, że taki mnożnik posiada szerszy zakres dynamicznych sygnałów wejściowych i niski poziom składowych kombinowanych sygnałów wyjściowych. (**Badania eksperymentalne mnożnika analogowego sygnałów na podstawie tranzystorów polowych**)*

Keywords: analog multiplier, field-effect transistor, combinational components.
Słowa kluczowe: wzmacniacz sygnału analogowego, tranzystor polowy, komponenty kombinowane.

Introduction

Analog multipliers is the second most frequently used functional element for processing analog signals after the operational amplifiers. They are important building blocks in many signal processing circuits like correlators, convolvers, adaptive filters, modulation detection, frequency translation, etc. Analog multipliers are the part of quadrature modulators that are used in forming signals with modern types of digital modulation, such as MSK, BPSK, DQPSK or QAM [1-3]. Several techniques of implementing analog multipliers, using field-effect transistors (FET), have been reported. They are the variable transconductance technique [4-6], the voltage-controlled transconductance technique, which employs FET transistors operating in the triode region [7–9], techniques based on square-law characteristics of FET transistors operating in the saturation region, implementing either the quarter-square identity [10–12] or other algebraic identity [13, 14]. For electronic signals' level control, controlled signal is multiplied by a constant voltage with the usage of the multiplier. With the implementation of adaptive filters and noise compensators, it is important to provide high linearity of characteristics when working with small signals, which is provided using analog multipliers. The structure of almost all modern phase-meters includes an analog multiplier. In the multiplying result spectrum of the two sinusoidal signals with the same frequency there is a constant component, which is directly proportional to the cosine of the phase shift. Therefore, the perfection of the analog multipliers and improvement of their characteristics is an important and urgent task.

Formulation of the problem

Balance and ring frequency converters circuits which based on bipolar transistors do not eliminate nonlinearity products of third and higher orders, even using specially selected semiconductor elements [15, 16]. This explains the significant amplitude-phase conversion, high level of nonlinearity products, and as a result, small dynamic range of the various functional units implemented in serial analog multipliers based on bipolar transistors. This fact complicates the use of such analog multipliers in precise measuring tools and relevant functional units of electronic equipment. In this regard, there's an interest in the realization of analog multipliers based on simple structure FETs, which providing nonlinearity no higher than second order. The main goal of this work is analyzing and experimental research of the analog multiplier based on FETs.

The circuit of the multiplier

It is known, that a simple structure FETs provide an insignificant nonlinearity higher than the second order. Special FETs with normalized quadraticity of transfer current-voltage characteristic are produced. For such FETs the manufacturer guarantees the determined attenuation of the third and higher orders combinational components.

Consider Fig. 1, which shows an equivalent circuit of the differential pair with asymmetric inputs based on FETs [15, 16].

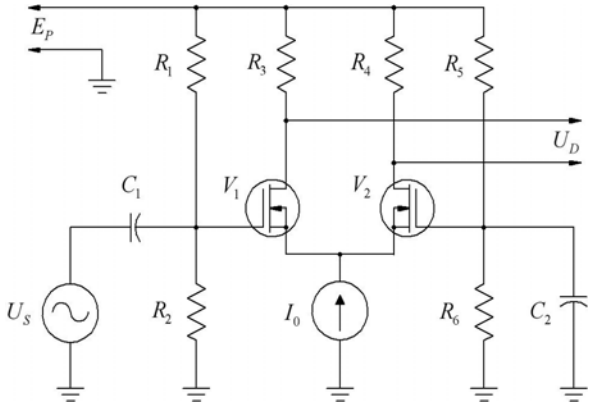

Figure 1 - Equivalent circuit of a differential pair with asymmetric inputs based on FETs

The powering of differential pair is provided by constant voltage E_P. By use of resistors R_1, R_2, R_5, R_6 constant bias on FETs gates is provided. Stable current source I_0 provides the constant currents sum value in sources of transistors V_1 and V_2. Sinusoidal input signal U_S through decoupling capacitor C_1 enters to the gate of the transistor V_1, gate of the transistor V_2 is blocked by capacitor C_2. The output voltage of the differential pair U_D is a symmetrical signal. It is formed on drains of transistors. Resistors R_3 and R_4 are the loading for drains' circuits. According to [15], by the quadratic approximation of transfer current-voltage characteristics of the simple structure FET, drain current is determined by the expression

$$I_D = I_{DC}\left(1 - \frac{U_{GS} - U_{GSC}}{U_P - U_{GSC}}\right)^2, \quad (1)$$

where U_{GS} - voltage between gate and source; U_P - threshold voltage; I_{DC} - classification value of drain current;

U_{GSC} - voltage between gate and source that corresponds to classification value of drain current.

According to [15], the drain currents of differential pair FETs, respectively for transistors V_1 and V_2, are determined by expressions

(2) $$I_{DV1} = \frac{1}{2} I_{DC} \left(\frac{I_0}{I_{DC}} - \frac{U_S}{U_P - U_{GSC}} \sqrt{\frac{2I_0}{I_{DC}} - \left(\frac{U_S}{U_P - U_{GSC}} \right)^2} \right),$$

(3) $$I_{DV1} = \frac{1}{2} I_{DC} \left(\frac{I_0}{I_{DC}} + \frac{U_S}{U_P - U_{GSC}} \sqrt{\frac{2I_0}{I_{DC}} - \left(\frac{U_S}{U_P - U_{GSC}} \right)^2} \right).$$

The operating principle of analog multipliers is based on the nonlinearity of FETs transfer current-voltage characteristics. In this case, the ideal form of characteristic is quadratic dependence [17, 18]. Consider the equivalent circuit of the analog multiplier based on FETs, which is shown in Fig. 2.

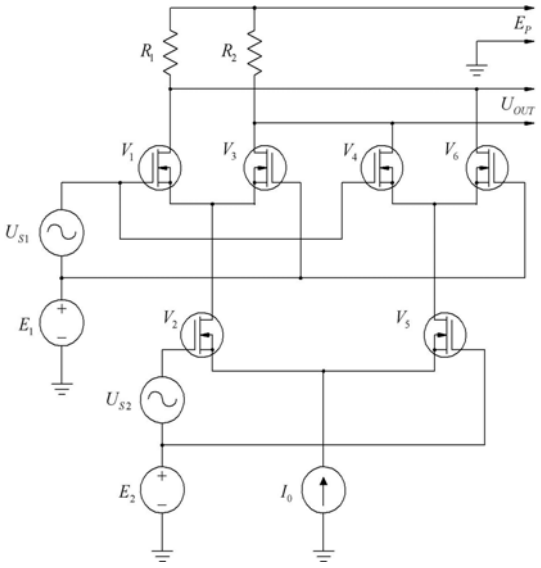

Figure 2 - Equivalent circuit of analog multiplier based on FETs

In this case, the ring circuit is formed by transistors V_1, V_3, V_4 and V_6. Constant bias on their gates is formed by source of constant voltage E_1. The sinusoidal voltage from the signal source U_{S1} on gates of the transistors differential pair V_1 and V_3 and the transistors differential pair V_4 and V_6 is coming in the antiphase. Therefore the relevant components of the output signal U_{OUT}, that are formed on the equal resistors R_1 and R_2, are also in antiphase. Output voltage component, which is formed by transistor V_6 drain current, compensates voltage component that is formed by transistor V_3 drain current. Similarly, there's made the compensation of the output voltage components, which is formed by transistors V_1 and V_4 drain currents. As a result, the voltage from the signal source U_{S1} can't get to the analog multiplier output. The similar situation is with sinusoidal signal U_{S2} - increasing of the transistor V_2 drain current is compensated by decreasing the transistor V_2 drain current, because the gates' voltage of these transistors are in antiphase. The summary current through resistors R_1 and R_2 doesn't change. Therefore the signal U_{S2} is not included to the multiplier output voltage U_{OUT}. Because of transistors transfer current-voltage characteristic quadraticity, components of drain currents through the resistors R_1 and R_2 which proportional to the product $U_{S1} \cdot U_{S2}$ are formed. The above components of the transistors pairs V_1, V_6 and V_3, V_4 drain currents are summed. As a result, the multiplier output voltage is directly proportional to the product $U_{S1} \cdot U_{S2}$. Due to the fact, that is the real transistors characteristics are not identical and transfer transistors current-voltage characteristics are not quadratic, high orders combination components and components with input signals frequency in the output signal are generated.

We assume that all the transistors that make up the analog multiplier have the same value of classification drain current I_{DC}, the same threshold voltage U_P, and the same voltage U_{GSC} between gate and source that matches the classification drain current. Considering that one of the multiplier input signals level is usually set by the user, we believe that a differential pair formed by transistors V_2 and V_5 works in linear section of its amplitude characteristic. Drain currents of its transistors are determined by expressions

(4) $$I_{DV2} = \frac{1}{2} I_{DC} \left(\frac{I_0}{I_{DC}} - \sqrt{\frac{2I_0}{I_{DC}}} \frac{U_{S2}}{U_P - U_{GSC}} \right),$$

(5) $$I_{DV5} = \frac{1}{2} I_{DC} \left(\frac{I_0}{I_{DC}} + \sqrt{\frac{2I_0}{I_{DC}}} \frac{U_{S2}}{U_P - U_{GSC}} \right).$$

Then the drain currents of each of the cross connected transistors V_1, V_6 and V_3, V_4, after expansion in degrees and accounting four members of expansion, are determined by expressions

(6) $$I_{DV1} = \frac{I_{DV2}}{2} - \frac{I_{DC}}{2} \frac{U_{S1} \sqrt{\frac{2I_{DV2}}{I_{DC}}}}{U_P - U_{GSC}} + \frac{I_{DC}}{4\sqrt{\frac{2I_{DV2}}{I_{DC}}}} \left(\frac{U_{S1}}{U_P - U_{GSC}} \right)^3,$$

(7) $$I_{DV6} = \frac{I_{DV5}}{2} + \frac{I_{DC}}{2} \frac{U_{S1} \sqrt{\frac{2I_{DV5}}{I_{DC}}}}{U_P - U_{GSC}} - \frac{I_{DC}}{4\sqrt{\frac{2I_{DV5}}{I_{DC}}}} \left(\frac{U_{S1}}{U_P - U_{GSC}} \right)^3,$$

(8) $$I_{DV3} = \frac{I_{DV2}}{2} + \frac{I_{DC}}{2} \frac{U_{S1} \sqrt{\frac{2I_{DV2}}{I_{DC}}}}{U_P - U_{GSC}} - \frac{I_{DC}}{4\sqrt{\frac{2I_{DV2}}{I_{DC}}}} \left(\frac{U_{S1}}{U_P - U_{GSC}} \right)^3,$$

(9) $$I_{DV4} = \frac{I_{DV5}}{2} - \frac{I_{DC}}{2} \frac{U_{S1} \sqrt{\frac{2I_{DV5}}{I_{DC}}}}{U_P - U_{GSC}} + \frac{I_{DC}}{4\sqrt{\frac{2I_{DV5}}{I_{DC}}}} \left(\frac{U_{S1}}{U_P - U_{GSC}} \right)^3.$$

Output voltage of analog multiplier is determined by the expression

(10) $$U_{OUT} = R\left(I_{DV1} + I_{DV6} - I_{DV3} - I_{DV4}\right),$$

where

(11) $$R = R_1 = R_2 .$$

Substituting (6)-(9) to (10), after transformations we obtain

(12) $$U_{OUT} = R\sqrt{2I_{DC}}\left(\sqrt{I_{DV2}} - \sqrt{I_{DV5}}\right)\frac{U_{S1}}{U_P - U_{GSC}} + \\ + \frac{1}{2}RI_{DC}\sqrt{\frac{I_{DC}}{2}}\left(\frac{1}{\sqrt{I_{DV2}}} - \frac{1}{\sqrt{I_{DV5}}}\right)\left(\frac{U_{S1}}{U_P - U_{GSC}}\right)^3.$$

Components of this expression $\sqrt{I_{DV2}}$, $\sqrt{I_{DV5}}$, $\frac{1}{\sqrt{I_{DV2}}}$ and $\frac{1}{\sqrt{I_{DV5}}}$ are the functions of U_{S2}.

Expanding them on degrees U_{S2} and limiting the three members of expansion, substituting the expressions for (12), after transformations we obtain

(13) $$U_{OUT} = -\frac{4RI_{DC}U_{S1}U_{S2}}{(U_P - U_{GSC})^2} - \frac{2RI_{DC}^2U_{S2}U_{S1}^3}{2\sqrt{2}I_0(U_P - U_{GSC})^4}.$$

For the multiplier operation, drain current of transistors V_2 and V_5 at operating point should be twice larger than the source currents of transistors V_1, V_3, V_4, and V_6 at the same voltage. In the analog multiplier based on FETs practical implementation it is possible to parallel turning on of two identical V_1, V_1, V_4 and V_6 transistors, as is done in [19]. Then we can assume, that in the scheme of Fig. 2, FETs V_2 and V_5 have a transfer current-voltage characteristic transconductance of twice larger than in V_1, V_3, V_4 and V_6.

In analog multiplier practical use in many cases harmonic signals are arriving at both of its inputs, i.e.

(14) $$U_{S1} = U_{m1}\cos\omega_1 t,$$

(15) $$U_{S2} = U_{m2}\cos\omega_2 t,$$

where U_{m1}, U_{m2} - amplitude of harmonic signals; ω_1, ω_2 - cyclic frequency of harmonic signals; t - time.

Substituting (14) and (15) to (13), after transformations we obtain

(16) $$U_{OUT} = -\frac{I_{DC}R\left(3I_{DC}U_{m1}^4 + 16\sqrt{2}I_0(U_p - U_{GSC})^4\right)}{8I_0(U_p - U_{GSC})^6}U_{m1}U_{m2}\cos(\omega_1 + \omega_2)t - \\ -\frac{I_{DC}R\left(3I_{DC}U_{m1}^4 + 16\sqrt{2}I_0(U_p - U_{GSC})^4\right)}{8I_0(U_p - U_{GSC})^6}U_{m1}U_{m2}\cos(\omega_1 - \omega_2)t - \\ -\frac{I_{DC}^2U_{m2}U_{m1}^3R}{8I_0(U_P - U_{GSC})^4}\cos(3\omega_2 + \omega_1)t - \frac{I_{DC}^2U_{m2}U_{m1}^3R}{8I_0(U_P - U_{GSC})^4}\cos(3\omega_2 - \omega_1)t.$$

The output signal components with the frequencies equal to the sum and difference of input signals frequencies is the main product of multiplication. Other components - fourth-order nonlinearity product conditioned by nonlinear dependence of transistors drain currents from the input signal voltage.

From the expression (16) follows that the level of the output signal main product depends linearly from U_{m2} and non-linearly from U_{m1}. This is true at sufficiently low U_{m2} signal level at which the FET's transfer current-voltage characteristics can be considered linear within the change in its level. While receiving the expression (16) we didn't consider the channel current cutoff, though in real terms this dependence is more complicated. The same is with the dependence of fourth-order nonlinearity products level from the input signals level.

The work [19] considers the analog multiplier based on 2П306А transistors with normalized transfer current-voltage characteristic quadraticity. The authors implemented and experimentally investigated analog multiplier on modern element base - transistors MFE120 of Digitron Semiconductors production [20]. To implement two copies of multiplier, twelve transistors are selected on a criterion of equality of threshold voltage and transfer current-voltage characteristic transconductance at the drain currents of 2.5 mA and 5 mA.

Let's present analog multiplier amplitude characteristic as the dependence of output signal spectral component level U_0, which frequency is equal to the sum or difference of input signals frequencies, from input signals levels. Fig. 3 shows the obtained experimentally amplitude characteristics of the researched analog multiplier.

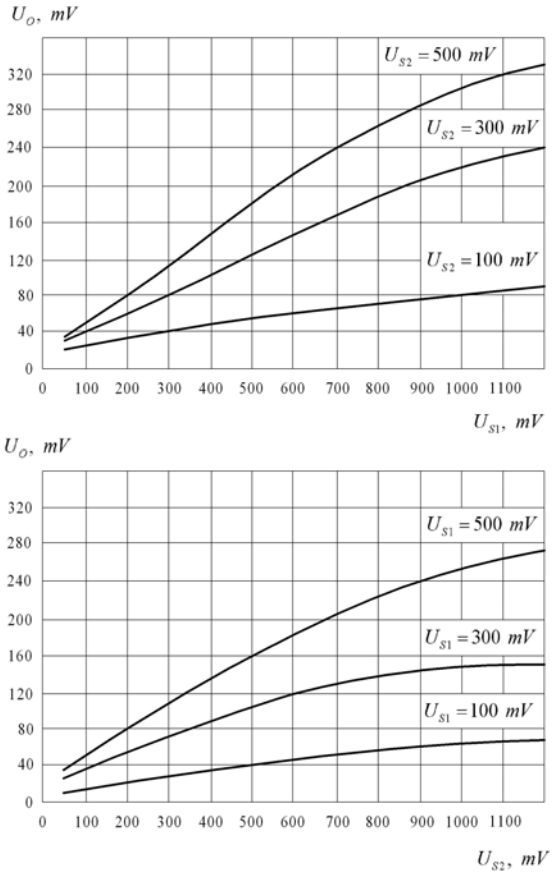

Figure 3 – Experimental amplitude characteristics of analog multiplier based on FETs

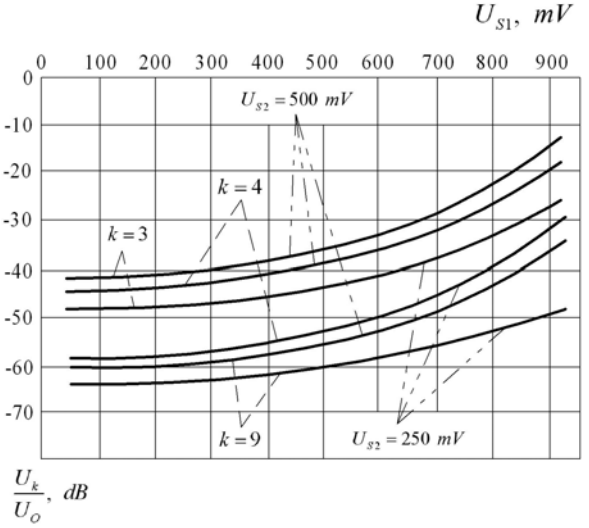

Figure 4 - Experimental dependencies of nonlinearity products levels of 3, 4, and 9 orders in the output signal from the input signals levels; k – order of nonlinearity; U_k – level of combinational component

Researches were carried out by selective microvoltmeter at 1 MHz of input signasl frequency and 1 mA drain current in transistors V_1, V_1, V_4 and V_6. The match of 1 mA current to the middle of transfer current-voltage characteristic quadratic section is proved by the experimental researches. Obtained experimental dependencies of nonlinearity products levels of 3, 4, and 9 orders in the output signal from the input signals levels are shown in Fig. 4.

Conclusions

On the basis of theoretical and experimental research of the analog multiplier based on FETs we can make the following conclusions:

1. The dynamic range of analog multiplier based on FETs input signals upper border is about 700 mV. With a higher level of input signals, the nonlinearity of the amplitude characteristics significantly increases.

2. Level of combinational components of 3, 4, and 9 orders in output signal of analog multiplier does not exceed -30 dB in the range of input signals up to 700 mV.

3. Analog multiplier based on FETs is advisable to perform as an integrated circuit. That improves its linearity, frequency and balance properties.

4. FETs have a higher quadraticity of transfer current-voltage characteristic, than bipolar transistors. There is reason to believe that an analog multiplier based on FETs in integrated design will provide a much lower level of combinational components in the output signal, than a multiplier based on bipolar transistors.

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