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EDA tools for designing ∑Δ modulators working in the current-mode

Abstract. *The article presents original tools for automating designing sigma-delta modulators working in the current mode. The solution makes it possible to optimize any modulator structure, to verify the compliance of the project with technological rules and to automate designing the layout of the circuit. The tools are compatible with popular design environments for CMOS circuits and with languages for describing circuit architectures. The proposed solution offers the designer the freedom of defining parameters expected of the modulator. The final result of the design process is a modulator topography obtained in a fully automated way and ready for fabrication. The effectiveness of the tools is demonstrated with an example of a modulator based on a current-to-frequency converter. The result of the design process was an SNDR coefficient equal to 76dB and the Walden's FoM equal to 616fj/step for 20kHz bandwidth.*

Streszczenie. *W artykule zaprezentowano autorskie narzędzia służące automatyzacji projektowania modulatorów sigma-delta pracujących w trybie prądowym. Przedstawione rozwiązanie umożliwia optymalizację dowolnej struktury modulatora, weryfikację zgodności projektu z regułami technologicznymi oraz automatyzację projektowania layoutu układu. Narzędzia zgodne są z popularnymi środowiskami projektowania układów CMOS oraz językami opisu architektury układów. Zaproponowane rozwiązanie oferuje projektantowi swobodę definiowania oczekiwanych parametrów modulatora, a finalnym rezultatem procesu projektowego jest w pełni automatycznie uzyskana topografia modulatora nadająca się do fabrykacji. Skuteczność narzędzi zademonstrownao na przykładzie modulatora bazującego na przetworniku prąd-częstotliwość. W wyniku procesu projektowego uzyskano współczynnik PSNR równy 76dB oraz Walden's FoM równy 616fj/step dla pasma 20 kHz. (**Narzędzia służące automatyzacji projektowania modulatorów sigma-delta**).*

Keywords: sigma-delta, EDA, design automation, current mode, Hooke-Jeeves.
Słowa kluczowe: sigma-delta, EDA, automatyzacja projektowania, tryb prądowy, Hooke-Jeeves.

Introduction

Nowadays, automating the design process of analog circuits is one of the most developed branches of microelectronics [1]. The popularity of digital circuits, together with competitive parameters of analog solutions inspire to develop complex mixed systems [2]. Due to the analog nature of the world, analog-to-digital converters are integral parts of such systems. Implementing them is not an easy task, as it requires to focus the design process on the demands of the system. The common use of converters and a number of difficulties associated with designing them are the reasons because of which authors of this article decided to propose automation tools for designing ΣΔ modulators. The miniaturization of CMOS technologies, on the other hand, makes it necessary to use the current mode in analog circuits [3]. Therefore the circuit presented in this article is dedicated to modulators working in the current mode. The presented solution makes it possible to automatically design a modulator with a structure selected by the user, and to define requirements in the form of parameters the modulator should have. The tool automates all stages of the design process: optimizing the structure, verification of technological rules and designing circuit topographies. The result of the described tool is a modulator layout ready for fabrication. It's parameters are verified during post-layout simulations.

Chapter 2 introduces original tools for automating the design of modulators at every stage of the process. It covers the possibility of integrating them with the existing design environments and languages for describing CMOS circuits architecture. Chapter 3 presents stages of a sample design process using the developed tools. The chapter begins with an example of a sample structure, which is the starting point. The next sections cover stages of the process and the final results compared with parameters of modulators of similar classes, designed with traditional methods.

Description of the original EDA tools

The tools proposed by the authors are compatible with the Mentor Graphics design environment and the Mathworks mathematical package. The applied design method is based on the approach proposed in literature [4]. In order to improve the effectiveness of the mentioned approach, a modified Hooke-Jeeves optimization algorithm [5] working in multi-core and distributed systems was used [6]. Transistor sizes of the modulator prototype are the variables of the optimization process. The goal of the optimization process is defined by the user.The data flow during the design process when using EDA tools is shown in Fig. 1.

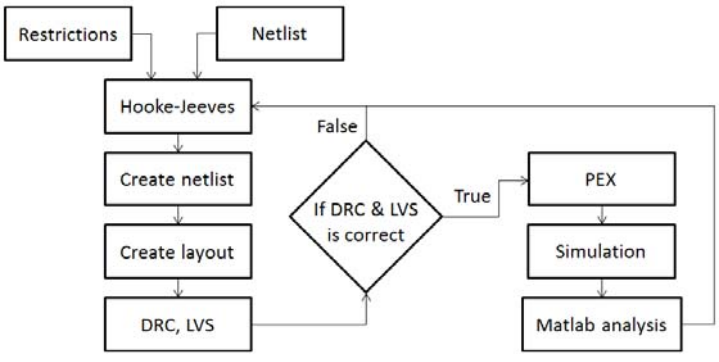

Fig. 1. Data flow of the developed EDA tool

The input data is a netlist described in the SPICE language (**Netlist**) and a set of constraints of the optimization process (**Restrictions**). The result of the optimization using the Hooke-Jeeves algorithm is a netlist with new transistor sizes (**Create Netlist**). The next steps of the algorithm for generating a topography are optional and may be omitted during the design process. Selecting parameters for the modulator prototype can be therefore performed either only at the stage of the schematic, with generating the layout at the end of the optimization process, or at the stage of the layout with generating the topography and a post-layout verification of the progress of the optimization process. When generating a topography (**Create Layout**), the tool makes use of the approach proposed in [7]. The algorithm uses the functionality of the ICStudio environment [8] which automatically generates a modulator layout, based on scripts written in the AMPLE language. The design path requires a full verification of the automated stages. Therefore the developed tools work with the Calibre package of the Mentor Graphics environment and make it possible to verify the compliance of the project with technological rules (**DRC**), as well as to verify the compliance of the topography with the netlist (**LVS**). Errors at this stage indicate the need to improve the parameters and to return to the stage of calculating them (**Hooke-Jeeves**). In case of a successful verification, a modulator netlist containing parasitic resistances and capacitances of the topography (**PEX**) is generated. If **Create layout ÷ PEX** steps are missed at this stage, the algorithm uses the netlist determined in step **Create netlist**. Simulation using the ELDO program, compatible with the SPICE standard, plus determining parameters of the modulator (**MATLAB analysis**) provides information about the progress of the design process. The target function is defined in the MATLAB environment – the user can define which parameters of the modulator will be optimized during the design process. The design process ends after obtaining the required modulator parameters.

The described system is controlled by scripts written in the BASH language and works in the Linux environment. This guarantees its flexibility and the possibility to integrate it with the software used for designing VLSI circuits all over the world. The MATLAB environment in a quick and easy way performs any result analysis resulting from an ELDO simulation. The final result of the described process is a schematic or a topography of a circuit meeting all design and technological requirements, and ready for production.

Example of the design process

This section presents examples of applications of the developed tools to the task of optimizing a ΣΔ modulator structure shown in Fig. 2 and based on the prototype proposed in [9].

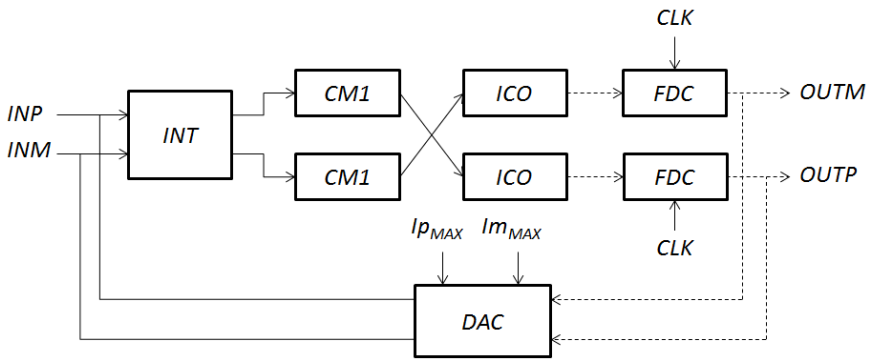

Fig. 2. ∑Δ modulator prototype based on a current-to-frequency converter

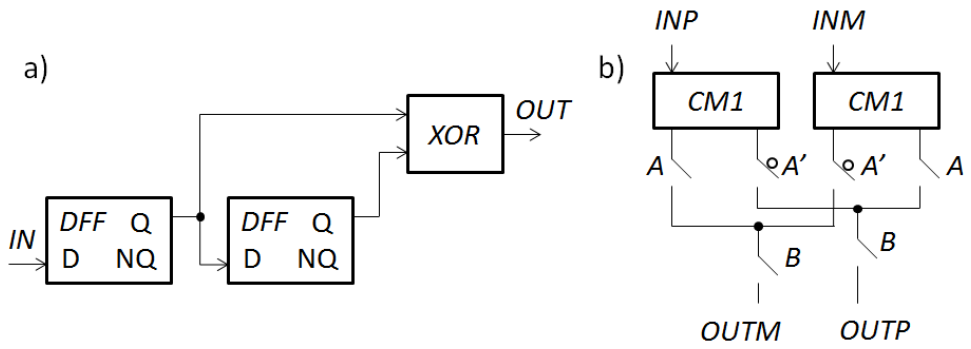

Fig. 3. a) Frequency to Digital Converter, b) DAC converter structure

As a low-pass filter (**INT**) we used an integrator working in the continuous time mode described in [10]. The modulator uses the current-to-frequency converter circuit (**ICO**) [11]. Separating the integrator from the oscillator was done using current mirrors (**CM1**) with a scaling factor of 1. As a quantizer, we use a Frequency to Digital Converter (**FDC**) shown in Fig. 3a) consisting of two DFF flip-flops and a XOR gate. The output of the converter takes the logical state of '1' in case of the detection of a change in the input signal during the sampling period of the modulator. The modulator has a two-bit output which works in the three-state logic. The functionality of the feedback of the modulator is described in equation 1.

$$\begin{cases} D[0] <= OUTP \; xor \; OUTM \\ D[1] <= OUTP' and \; OUTM \end{cases} \quad (1)$$

The DAC converter circuit shown in Fig. 3b) was used as a feedback. Its structure contains two two-output mirrors, reproducing Ip_{MAX} and Im_{MAX} signals, representing the range of input currents the modulator works in. Mirror

outputs are keyed (at digital inputs A and B) with output signals from FDC converters, i.e. OUTP and OUTM. This structure does not contain logic circuits, except of single transistors used as keys. The output of the DAC circuit has the state of [0, 0] when the OUTM signal gets the value of '0'. Otherwise, according to equation 1, outputs have the state of [Ip_{MAX}, Im_{MAX}] or [Im_{MAX}, Ip_{MAX}], depending on the value of the OUTP bit.

Voltage signals are shown as dotted lines in Fig. 2. The modulator has a balanced structure and therefore representations of positive and negative signals appear in the processing track. However, the current-to-frequency converter (**ICO**) works only for input (positive) currents. In order to keep the same direction of currents in the track and to meet requirements of the ICO circuit, we used a current offset at the input of the integrator, equal to three times the range of input signal changes, that is $Ip_{MAX} - Im_{MAX}$. The value of the offset results from the presence of the feedback in the modulator.

In order to provide control over harmonics in the optimization process, we defined a constraint ensuring high linearity of operation of individual modules of the modulator. Transistor sizes were selected in order to ensure the symmetry of positive and negative currents at the outputs of the integrator, mirrors and the DAC circuit. In practice, it means that the input and output nodes of the above circuits have voltage equal to (VDD+VSS)/2 and the voltage differences between the outputs must not be higher than hundredths of a mV, at 1.8V power supply. Improving the SNDR parameter and the Walden's Figure of Merit (FoM) were adopted as the optimization criterium defined in Matlab. The obtained parameters of the modulator are shown in Table 1. FoM was calculated using equation 2, where ENOB is defined as an effective number of bits.

$$\text{FoM} = \frac{\text{Power}}{2 \cdot \text{BW} \cdot 2^{ENOB}} \tag{2}$$

Frequency response for an input function with an amplitude of 2.3uA and a frequency of 3kHz is presented in Fig. 4. The automatically generated layout of the circuit is presented in Fig. 5. As one can see, the row strategy was adopted in the presented tools for generating the topography of a modulator.

Table 1. Parameters of the designed modulator

	Current work	[12]		[13]	[14]	[15]
Technology [nm]	65	180		180	180	130
V_{DD} [V]	1.2	1		0.5	0.5	0.4
Sampling [MHz]	10	2		3.2	10	3.2
Signal Bandwidth [kHz]	20	20		25	78	20
Power [uW]	64	660	860	300	860	140
SNDR [dB]	76	84		74	71	68
FoM [fj/step]	616	1270	1660	1460	1900	1710

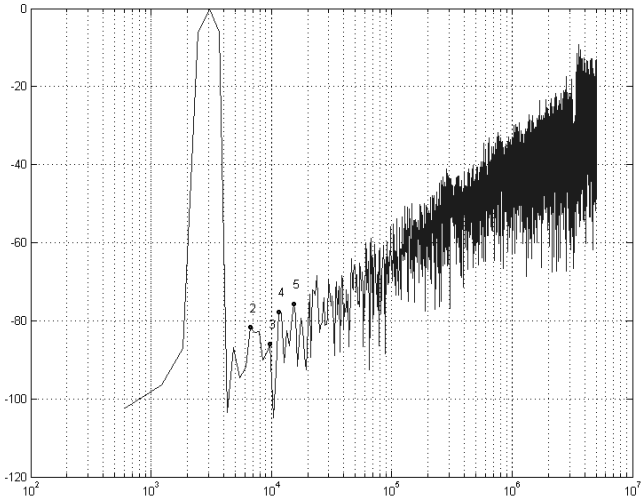

Fig. 4. Output spectrum of the fully automated designed modulator (2^{14} point FFT)

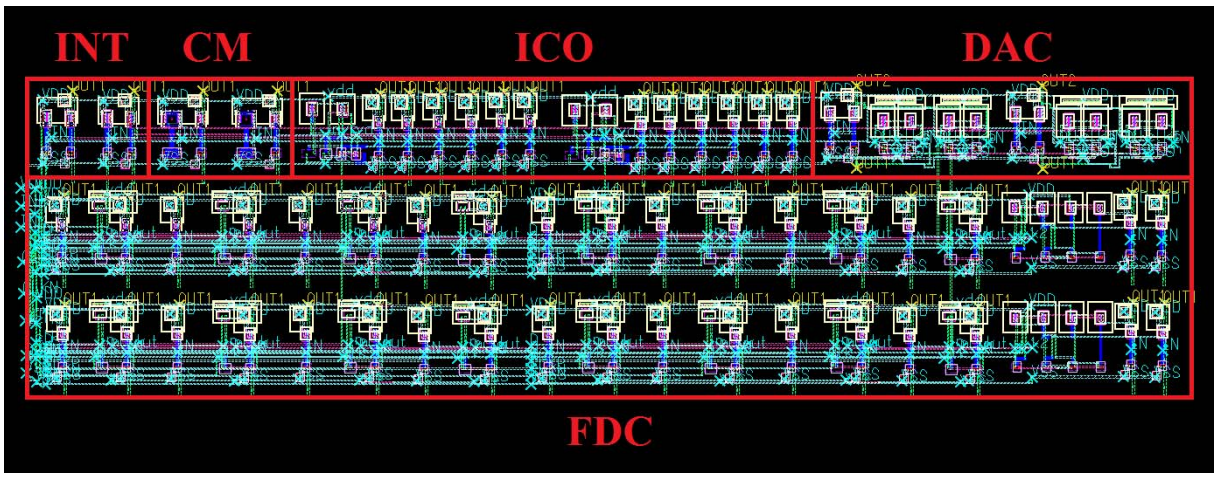

Fig. 5. Modulator layout obtained using the described EDA tools

Summary

The article presents a method for automating designing modulators working in the current mode, according to criteria defined by the designer. The developed EDA tools are compatible with commercial design environments and description standards for electronic circuits. The work of the tools was demonstrated with an example of a modulator with a current-to-frequency converter. The result of the optimization was an SNDR coefficient equal to 76dB and the Walden's Figure of Merit equal to 616fj/step. The environment also makes it possible to generate a topography of a circuit.

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