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Mitigation of Steel Making Plants' Electrical Power Quality Problems Using SVC – A Case Study

***Abstract**. The first part in this paper presents the steps of the design for required Static Var Compensator (SVC) system to eliminate power quality problems. The second part will discuss the dynamic model in the form of differential equation used for the EAF. The EAF model is then integrated with the SVC model to demonstrate network dynamic interactions during different operating conditions. Finally, comparison between design and actual power quality performance figures measured for actual steel making plant substation are shown at the end to validate the design values.*

Streszczenie.** W artykule opisano projekt układu kompensacji mocy biernej w przedsiębiorstwie hutniczym a następnie analizowano właściwości dynamiczne systemu. Porównano dotychczas istniejący system i nowy system z kompensacja mocy biernej. **Problem poprawy jakości energii elektrycznej w przedsiębiorstwie hutniczym – analiza przypadku.

Keywords: Power Quality, SVC, EAF, Harmonics.
Słowa kluczowe: jakość energii elektrycznej, przedsiębiorstwo hutnicze.

Introduction

The main power supply voltage of network under-study is 220 kV at point of common coupling (PCC) "220/66 kV substation.

The steel making substation is supplying all plants with necessary electric energy on 33 kV, 6.6 kV and 400 V levels, the most significant loads are the EAF's and Ladle Furnaces (LF's) which represent 50% of total plants consumption.

CASE STUDY OVERVIEW

Power Network Topology and System Overview

The network with PCC and the single line diagram of electric arc furnaces and ladle furnaces inside the Steel Making Plant (SMP) are as described in table 1 and Fig. 1 respectively:

Table 1 Network Data

PCC (kV)	220/66
Substation incoming feeders installed capacity (MVA)	3x380
Steel Making plant Power Transformers kV	220/33
Steel Making plant Power Transformers MVA	2x125/150 (ONAN/ONAF)
Steel Making plant Power Transformers Z% EAF MVA	21 % 4 X 58 MVA
EAF Rated PF EAF Transformer Impedance at 58 MVA for 721 V	0.78 15.65%
EAF Secondary Impedance EAF Compensation Mvar	2.4 mΩ 4x12 Mvar
Ladle Furnace's (LF's) MVA LF's Compensation Mvar	3x15 MVA 3 x 7.5 Mvar
Short Circuit Capacity Minimum MVA Short Circuit Capacity Maximum MVA	8000 15000
System X/R Ratio	10

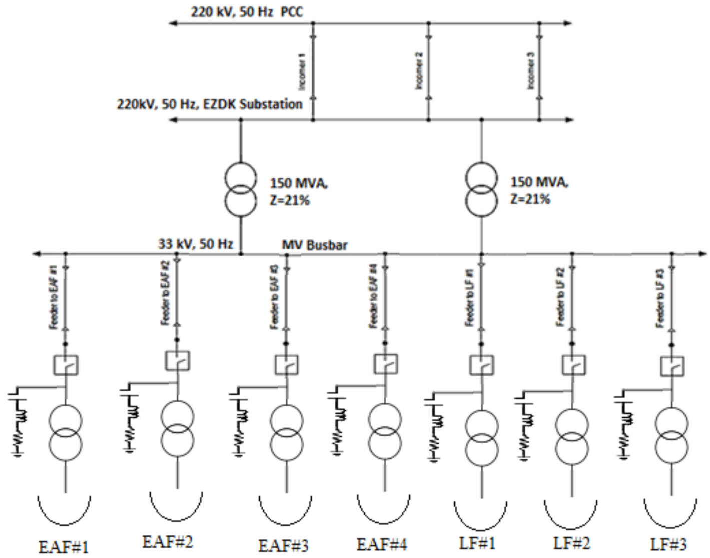

Fig. 1. SLD of power system network under-study

Calculation of Network Parameters

Voltage Drop: The voltage drop, which is caused by the active and reactive power of the electrical loads, consists of the following components:

(1) Q at S_{CCX} (reactive): $\frac{\Delta V}{V} = \frac{\Delta Q}{S_{CCX}}$,

(2) P at S_{CCR} (resistive): $\frac{\Delta V}{V} = \frac{\Delta P}{S_{CCR}}$.

S_{CC} is the short circuit capacity at the furnace bus bar.

For an X/R ratio of 10 for the PCC, a minimum short circuit capacity of 8000 MVA and 2×125 MVA transformers with 21% impedance, the reactive and resistive part of the short circuit capacity at SMP Bus can be calculated at PCC as following noting that from per unit calculations, network source impedance is (1/8000), the 2 parallel step down transformers' equivalent per unit impedance is (0.21/250) and the overall reactive fault level is the base MVA divided by overall equivalent per unit impedance:

(3) $S_{CCX} = \frac{1}{\frac{1}{8000\ \mathrm{MVA}} + \frac{0.21}{250\ \mathrm{MVA}}} = 1036$ Mvar,

$S_{CCR} = 10360$ MW.

For operation with 4 EAF's and 3 L.F's in operation at 0.78 rated PF the voltage drop can be calculated from (1) as follows:

(4) $\frac{\Delta V}{V} = \frac{\sqrt{(58\times4+15\times3)^2-[(58\times4+15\times3)\times0.78]^2}}{1036} = 16.7\%.$

In Case of only compensation filters at plant side in operation the voltage drop can be calculated with the same equation as follows:

(5) $\frac{\Delta V}{V} = \frac{4\times12.5+3\times7.5}{1036} = 6.8\%.$

This makes the voltage variation on network for different load conditions from + 7 % to -17 %, which is a difference of 24 % as shown in Fig. 2 and the approx. calculated voltage droop is 0.1 % / Mvar (1/1036 x 100).

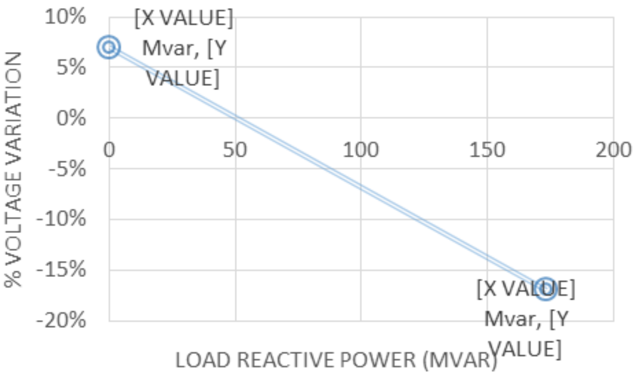

Fig. 2. Voltage drop against load reactive power

Flicker Calculation: According to Union Internationale d'Electrothermie (UIE) [1] the uncompensated flicker level of an AC arc furnace during scrap melting can be calculated as follows:

(6) $P_{st,95\%} = 0.85 \times K_{st} \times \frac{Scc\_furnace}{Scc\_network}.$

0.85 is the empirical ratio between Pst,95% and Pst,99%

Kst is the so-called furnace severity factor describing the furnace characteristics as a flicker generator.

The Kst factor varies from furnace to furnace, a range of 48 ... 85 is reported by the UIE, and is influenced by:

- Furnace operation point (arc power, arc voltage/length, power factor);
- Mechanical furnace data (pitch circle diameter, resonance behavior of electrode arms);
- Electrode control system;
- Furnace temperature (cold or hot furnace);
- Charge mix (quality of scrap, size of scrap, charging of hot metal, Direct Reduced Iron (DRI), etc…);
- Charging (bucket charge or via shaft)

Because of mainly DRI as charge material a Kst factor of 48 can be assumed for further calculations. The furnace short circuit level Sccf for one furnace 58/70 MVA can be derived as follows:

Furnace transformer impedance

(7) $X_{FT} = \frac{0.1565\times 33^2}{58}\ \Omega = 2.94\ \Omega.$

Furnace secondary impedance (voltage tap 721 V):

(8) $X_{FS} = 0.0024 \times \frac{33^2}{0.721^2}\ \Omega = 5.03\ \Omega.$

The total impedance results in

(9) $X_{total} = (2.94 + 5.03)\ \Omega = 7.97\ \Omega.$

The furnace short circuit level is then

(10) $S_{ccf} = \frac{33^2}{7.97}\ \text{MVA} = 137\ \text{MVA}.$

Based on the minimum fault level of Sccn = 8000 MVA the uncompensated flicker is:

(11) $P_{st,99\%} = 48 \times \frac{137}{8000} = 0.822.$

IEC 61000-3-7 2008 [2] introduces equation (12) to obtain the short-term flicker severity index values caused by several fluctuating loads

(12) $P_{st} = \sqrt[m]{\sum_j P_{stj}^m}.$

Where P_{stj} is the contribution of the jth fluctuating load.

m =2 for arc furnaces where coincident fluctuations are probable, for example coincident melts.

The flicker of four furnaces during meltdown can be estimated with the formula:

(13) $P_{st,99\%} = \sqrt[2]{P_{st1}^2 + P_{st2}^2 + P_{st3}^2 + P_{st4}^2}\ ,$

(14) $P_{st,99\%} = \sqrt[2]{0.822^2 + 0.822^2 + 0.822^2 + 0.822^2}\ ,$

(15) $P_{st,99\%} = 1.64,$

(16) $P_{st,95\%} = 0.85 \times 1.64 = 1.39,$

The relation between ΔV10 and P_{st} can be taken as one third according to UIE Publication [3].

(17) ΔV10 = 1.39 / 3 = 0.46.

To keep the flicker values on medium and high voltage levels below the limits stated in European standard EN 50160 [4], appropriate planning levels have been proposed in IEC report IEC 61000-3-7 [2]. As a guideline, P_{st} and P_{lt} should not exceed the planning levels given in table 2 more than 1% of the time (99% probability level) with a minimum assessment period of one week [5].

Table 2 IEC Pst and Plt Recommended Planning Levels

	MV	HV-EHV
Pst	0.9	0.8
Plt	0.7	0.6

SVC System Selection

SVC system consists of a Thyristor Controlled Reactor (TCR, variable inductive power) and System of Filter Circuits (FC, constant capacitive power). A Filter Circuit is a tuned circuit, which consists of capacitor banks (capacitance) and tuned reactor coils (inductance) connected in series, [6]. Filter circuits will reduce the negative influence of the loads like harmonic distortion and poor power factor.

Careful choice of the tuning frequencies of the filter circuits with respect to the generated harmonic frequencies and amplitudes will reduce the harmonic levels [7]. At fundamental frequency filter circuits behave like capacitors and therefore provide power factor improvement.

The TCR consists of thyristor valves in series with reactors directly connected to the medium voltage plant busbar (33 kV).

The TCR will reduce the negative influence of the loads like flicker, voltage fluctuation and voltage unbalance.

The so-called "indirect compensation "is proposed for voltage stabilization. The lagging reactive currents of the TCR are controlled by this method in such a way that for each phase the sum of the load reactive current and the TCR current gives a constant value at any instant. This is compensated by the capacitive current of the filter system.

This results in the following reactive power equilibrium and therefore minimum voltage variation and flicker [8]:

(18) $Q_{load}+Q_{TCR}-Q_{FC}=0$

where Q_{load} is reactive power of EAF / LF (fluctuating with process); Q_{TCR}: reactive power of Thyristor Controlled Reactor (controlled by SVC system); Q_{FC}: reactive power of Filter Circuits (constant).

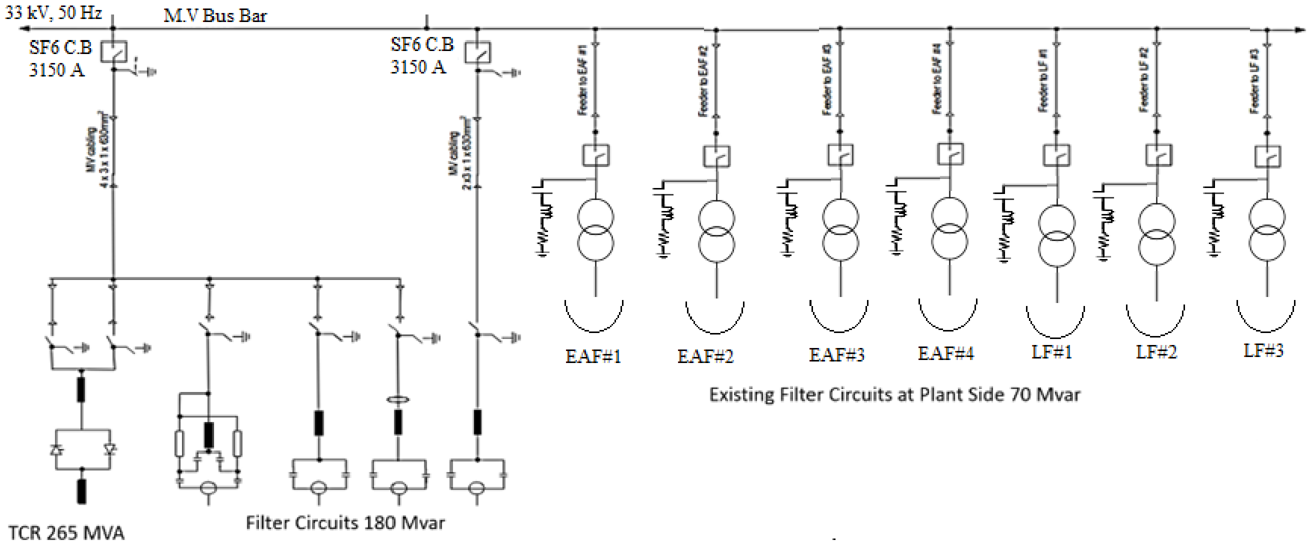

Fig. 3. SLD of power system network understudy with SVC

For stabilizing the bus voltage, the SVC system must be sufficiently rated to compensate the voltage drops, which are caused by the active and the reactive power.

In case of 4 EAF's and 3 LF's in operation at 0.78 rated PF resulting in 277 MVA and 216 Mvar a typical SVC compensation system can be sized as follows [9]:

(19) $S_{svc} = \left(\frac{\text{Pst,99\% (with out SVC)}}{\text{Planned Pst,99\% (with SVC)}} - 1\right) \times 1.3 \times S_{EAF's}$,

Where: $S_{EAF's}$ is the 4 EAF's and 3 LF's MVA, S_{svc} is the required SVC Mvar capacity, 1.3 is a rule of thumb reserve factor from engineering practice for the SVC system application

(20) $S_{svc} = \left(\frac{1.3}{0.8} - 1\right) \times 1.3 \times 277 = 225$ MVA.

Accordingly, a 250 Mvar SVC can be adequate for compensation with power margin for dynamic compensation.

The network reduction factor for such system would be 1036/250 = 4.1 and a flicker reduction factor of approx. 1.625 (1.3/0.8) can be expected, resulting in design flicker level of:

(21) $P_{st99\%} = 1.64 / 1.625 = 1.009$;
(22) $P_{st95\%} = 1.39 / 1.625 = 0.85$;
(23) $\Delta V10 = 0.46 / 1.625 = 0.28$.

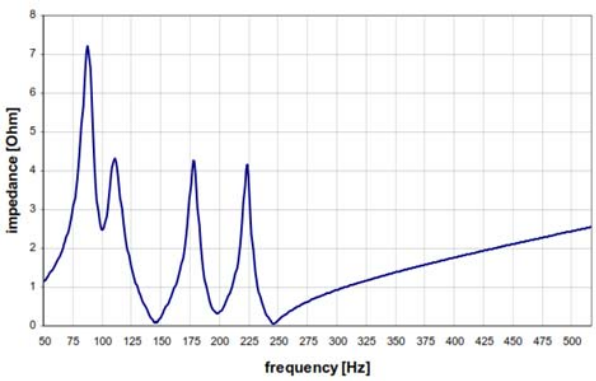

Fig. 4. Resulting frequency response at the 33 kV EAF busbar for a PCC short circuit capacity of 8000 MVA

On the other hand, it should be taken into consideration that from engineering practice point of view, the reduction factor between the compensation system Mvar and network MVA short circuit should not be lower than 3.5, because an overdesigned system for small short circuit capacity networks will result into network instability in case of transients in compensation system.

Fig. 3 shows the SLD of the SVC system for the under study network. The harmonic filters of the SVC compensation are to be tuned to eliminate second, third, fourth and fifth harmonics detected in network as can be shown in the frequency response plot in Fig. 4.

Case Study Simulation

MATLAB Simulink Model of EAF

Some chaos-based models reported in specialized literature have been applied to simulate ac and dc arc furnaces [10]-[11]. The development of general dynamic arc model in the form of a differential equation is based on the principle of conservation of energy. The approach is fundamentally different from those methods where some empirical relation is used to represent the electrical arc, since it has been observed that the electric fluctuations in an arc furnace are chaotic in nature [12]. In the dynamic model such relations which are implicit for steady state conditions are not pre-defined. This makes the models give result for different conditions depending on both frequency and current magnitudes. Here, the arc furnace is modeled in two stages. First dynamic electric arc modeling is done and the obtained arc voltage is then modulated with chaotic signal to produce final arc furnace model.

The power balance equation for the arc can be expressed according to [11] by:

(24) $P_1+P_2=P_3$,

Where: P_1 represents the power transmitted in the form of heat to the external environment; P_2 represents the power, which increases the internal energy in the arc, and which therefore affects its radius; P_3 represents the total power developed in the arc and converted into heat.

The above equation can be represented in the form of differential equation of the arc:

(25) $k_1 r^n + k_2 r \frac{dr}{dt} = \frac{k_3}{r^{m+2}} i^2$,

where: r is the arc radius and is chosen as the state variable instead of taking arc resistance or conductance, k_1, k_2 and k_3 are constants relative to EAF melting conditions, m is the variations of the resistivity with temperature,

n is the conditions of cooling.

The arc voltage is given by:

(26) $v = \frac{i}{g}$,

Where g is defined as arc conductance and is given by equation (27)

(27) $g = \frac{r^{m+2}}{k_3}$.

It is possible to represent the different stages of the arcing process by simply modifying the parameters of m and n. When the environment temperature is relatively high, n=0; when the arc length is relatively long, n=1, while it's short, n=2; the value of m varies among range of 0, 1, 2 when arc radius increases; k_1, k_2, k_3 vary according to practical situations [13]. The complete set of combination of these parameters for different stages of electric arc can be found in [11].

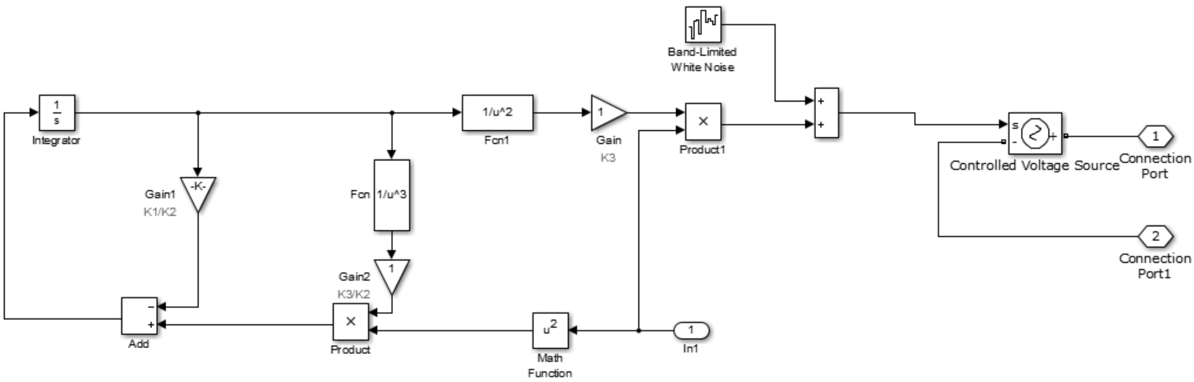

Fig. 5. MATLAB/ Simulink model of electric Arc Furnace

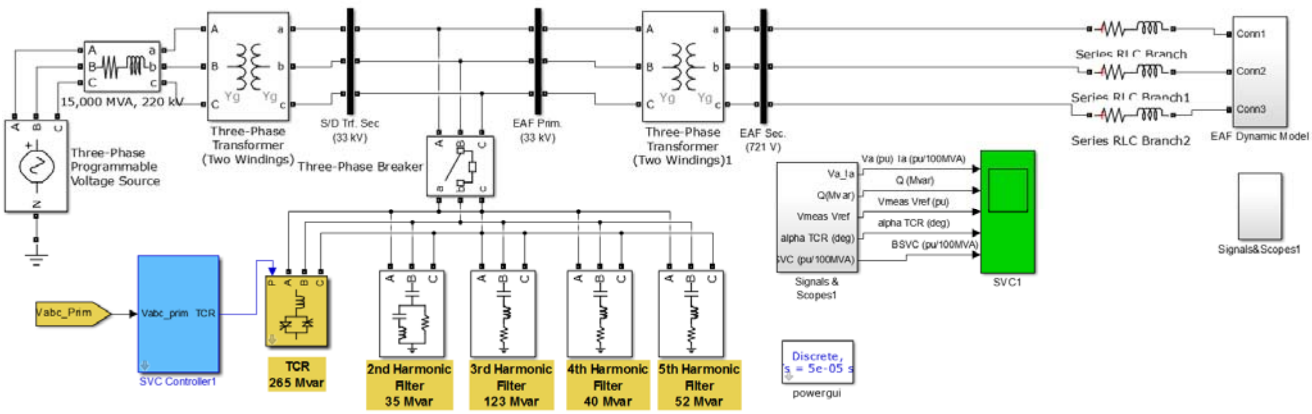

Fig. 6. SVC System Simulation in Matlab Environment

The general arc equation (25) is a first-order nonlinear differential equation. Unfortunately, there are no general analytical methods which allow to solve any nonlinear differential equation, even of the first-order. In that case the general arc equation (25) is not separable neither exact, so there is no simple way to find its solution in a closed form [14]. However, a closed form solution to equation (25) has been developed for some arc parameters in [15].

Taking the parameters K_1= 3000; K_2 = 1; K_3 = 1; n=2; m= 0 to simulate melting stages, equations (25) and (26) would be in this case:

(28) $r^o = \frac{K3}{K2\, r^3} i^2 - \frac{K1}{K2} r$,

(29) $V = i \times \frac{K3}{r^2}$.

Implementing the above equations using numerical approach of Simulink blockset as shown in Fig.5, the EAF model can be combined with the band limit white noise to create the chaotic nature of the arc furnace voltage and current [16]- [17]- [18].

The chaotic-dynamic voltage/current characteristic of the electric arc from the model are illustrated in Fig.6.

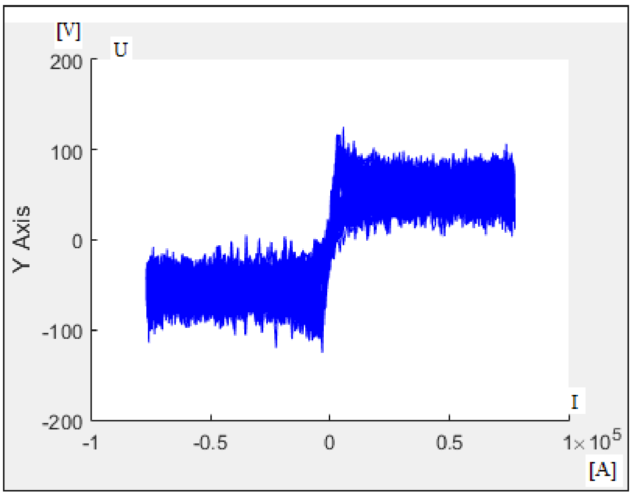

Fig. 7. Dynamic Characteristics of EAF

MATLAB Simulink Model of SVC

Based on the model built in MATLAB environment by [19], the SVC control system can be simulated as shown in Fig. 7 after parametrizing the network data to the discussed network parameters as table 3:

Table 3 Network Data of SVC

Thyristor Controlled Reactors (TCR), MVA	265
2nd Harmonic Filter, Mvar	35
3rd Harmonic Filter, Mvar	123
4th Harmonic Filter, Mvar	40
5th Harmonic Filter, Mvar	52
Total Harmonic Filters, Mvar	250

The SVC reactions to regulate voltage on the system are illustrated in Fig.8.
When system voltage is low the SVC generates reactive power (SVC capacitive). When system voltage is high it absorbs reactive power (SVC inductive).

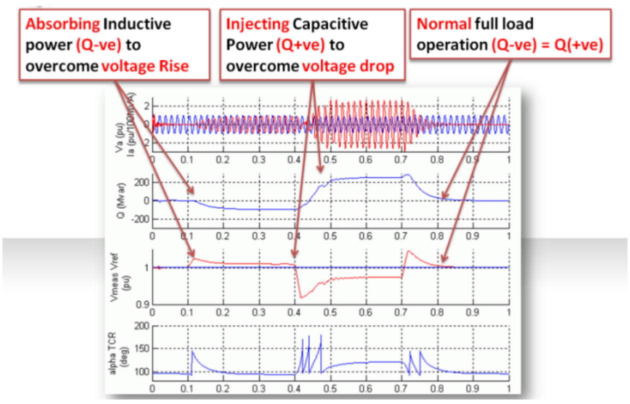

Fig. 8. SVC Interaction with Power Network Dynamics

Comparison between design and actual power quality performance figures

Short Circuit Power at PCC

The actual short circuit capacity of the network is assessed by measuring the voltage drop, due to sudden change of the reactive power on the 220kV (PCC).

This is done starting from no-load conditions with simulation converter reactive power drop in TCR control logic. The actual short circuit capacity Sccn is calculated according to the following formula:

(30) $S_{ccn} = \frac{\Delta Q}{\Delta V/V}$.

Location of measurement: SVC control panel;
Secondary side PT, Ratio 220/0.11 kV;
Measuring device: Power analyzer UMG 605 (Janitza).

Table 4 Short Circuit Readings at PCC

Q1	Q2	V1	V2	Sccn = (Q1-Q2) / (V1-V2) × V1
0 Mvar	30 Mvar	211.64 Mvar	211.24 Mvar	15.87 GVA
0 Mvar	40 Mvar	211.64 Mvar	211.02 Mvar	13.65 GVA

As seen in table 4, the actual short circuit capacity of 220kV line is higher than 8000 MVA, the design condition is fulfilled.

Power Factor

The active (MWh) and reactive (Mvarh) energy readings of substation's meters at the incoming 220kV feeder (primary side of 220/33 kV step down transformer) is used to determine the mean value of the power factor.

(31) $PF = \frac{1}{\sqrt{\left[\frac{W_Q}{W_P}\right]^2 + 1}}$,

Where: W_Q = lagging reactive energy; Design Value: PF ≥ 0.95 lagging; Duration of test: 72 hours.
Location of measurement: INC 1, INC2 and INC 3 in supervisory control panel.
Measuring device:
Incomer 1: AINTRAL-X (ABB);
Incomer 2: AINTRAL-X (ABB);
Incomer 3: AINTRAL (ELSTER);
Duration of measurement: 72 hours.

Table 5 Power Factor Readings at PCC

	Start of Measurement		End of Measurement	
	Act. Energy, MWh	React. Energy Mvarh	Act. Energy, MWh	React. Energy Mvarh
Incomer 1	488036	185053	496757	185880
Incomer 2	399162	176026	407815	176909
Incomer 3	153558	770893	159000	771497
Summary	1040756	1131972	1063572	1134286

Table 6 Total Energy Readings at PCC

Index	Energy Meter Readings		Consumed Energy	
	Act. Energy, MWh	React. Energy Mvarh	Act. Energy, MWh	React. Energy Mvarh
Start	1040756	1131972	-	-
After 72 Hrs	1063572	1134286	22816	2314

Table 7 Total Power Factor Reading at PCC

Description	Design Value	Determined (measured) Value
Power Factor (PCC)	PF ≥ 0.95 lagging	PF = 0.99 lagging

As seen in table 7, the performance figures are fulfilled.

Flicker

Measurement of the voltage flicker is carried out for normal operation of the arc furnaces and ladle furnaces. The design value is fulfilled when 95% of all measured values are below or equal to the following values:

Design values: $\Delta V10 \leq 0.45$ (equivalent to Pst95% ≤ 1.35)

Pst-values shall be 10 minute rolling values as per UIE/IEC.

Measuring point: 220kV PCC

Duration of test: 72 hours

The existing values of voltage flicker measured without the arc furnaces and without SVC in operation are to be deducted from the measured value mentioned below according to the formula:

(32) $P_{st,95\%} = \sqrt{P_{st\_total}^{\ 2} - P_{st\_exist}^{\ 2}}$,

where: $P_{st,95\%}$ is the resulting flicker $P_{st\ total}$ = measured flicker with EAF's, LF's and the SVC P_{st_exist} = measured flicker without EAF's, LF's and SVC' P_{st} is approximate linear to the $\Delta V10$ method, with the empirically determined ratio of $\Delta V10 = (1/3) \times P_{st}$ [3].
Location of measurement: 220kV PCC, SVC control panel.
Secondary side PT, Ratio 220/0.11 kV
Measuring device: Power Quality Analyser PQ-Box 100 (A-Eberle).
Duration of measurement Pst_total: 72 hours

Table 8 Flicker Reading at PCC

Description	Design Value	Measured existing Flicker (Pst exist 95%/ΔV10)	Measured total Flicker (Pst exist 95%/ΔV10)	Measured total Flicker (Pst exist 95%/ΔV10)
Flicker P_{st} 95 %	Pst 95 % ≤ 0.85	N/A	0.68	0.68
ΔV10 = (1/3) × P_{st} 95 %	ΔV10 ≤ 0.28	N/A	0.23	0.23

As seen in table 8, the performance figures are fulfilled.

Table 9 Harmonic Distortion at PCC

Harmonic Order	Design Value	Measured existing Distortion (V_{n}_exist 95%)	Measured total Distortion (V_{n}_total 95%)	Resulting Performance Value (V_n 95%)
Total Harmonic Distortion (PCC)	THVD ≤ 1.5 %	N/A	0.407	0.407
Harm. Voltage (PCC) - 100 Hz	V 100 Hz ≤ 0.5 %	N/A	0.073	0.073
Harm. Voltage (PCC) - 150 Hz	V 150 Hz ≤ 1.0 %	N/A	0.149	0.149
Harm. Voltage (PCC) - 200 Hz	V 200 Hz ≤ 0.5 %	N/A	0.015	0.015
Harm. Voltage (PCC) - 250 Hz	V 250 Hz ≤ 1.0 %	N/A	0.189	0.189
Harm. Voltage (PCC) - 300 Hz	V 300 Hz ≤ 0.5 %	N/A	0.016	0.016
Harm. Voltage (PCC) - 350 Hz	V 350 Hz ≤ 1.0 %	N/A	0.295	0.295
Harm. Voltage (PCC) - 400 Hz	V 400 Hz ≤ 0.5 %	N/A	0.015	0.015
Harm. Voltage (PCC) - 450 Hz	V 450 Hz ≤ 1.0 %	N/A	0.057	0.057
Harm. Voltage (PCC) - 500 Hz	V 500 Hz ≤ 0.5 %	N/A	0.014	0.014
Harm. Voltage (PCC) - 550 Hz	V 550 Hz ≤ 1.0 %	N/A	0.261	0.261
Harm. Voltage (PCC) - 600 Hz	V 600 Hz ≤ 0.5 %	N/A	0.012	0.012
Harm. Voltage (PCC) - 650 Hz	V 650 Hz ≤ 1.0 %	N/A	0.139	0.139
Harm. Voltage (PCC) - 700 Hz	V 700 Hz ≤ 0.5 %	N/A	0.006	0.006

As seen in table 9 and Fig. 9, the performance figures are fulfilled.

Harmonic Voltage Distortion

Measurement of the voltage fluctuation is carried out for normal operation of the arc furnaces / ladle furnaces according to the operation.

The design value is fulfilled when 95% of all measured values are below or equal to the following values:

THVD 95% ≤ 1.5%

where: Individual odd harmonics $V_{odd\ 95\%} \leq 1.0\%$; Individual even harmonics $V_{even\ 95\%} \leq 0.5\%$;

(33) $$\mathrm{THVD}=\sqrt{\sum_{n=2}^{n=25}\left[\frac{V_n}{V_1}\right]^2}\,.$$

Measuring point: 220kV PCC for a 3-second interval

Duration of test: 72 hours

The existing harmonic background level will be deducted geometrically according to the formula:

(34) $$V_n = \sqrt{{V_{n\_total}}^2 - {V_{n\_exist}}^2}\,,$$

where: V_n = resulting harmonic voltage distortion $V_{n\ total}$ = measured harmonic voltage distortion with EAF, LF and SVC, V_{n_exist} = measured harmonic voltage distortion without EAF, LF and SVC.

Location of measurement: 220kV PCC, SVC control panel;

Secondary side PT, Ratio 220/0.11 kV;

Measuring device: Power Quality Analyzer PQ-Box 100 (A-Eberle);

Duration of measurement V_{n_total}:72 hours.

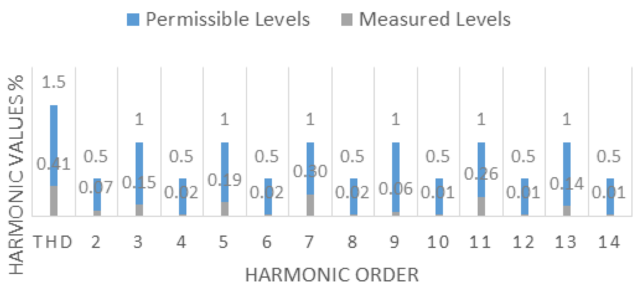

Fig. 9. Permissible and measured harmonics spectrum

Voltage Stabilization at the 33 kV Steel Making Bus

The compensation system is designed so that the following electrical values, caused by specified loads, are kept:

Minimum: +0.5 % (3second average value);

Maximum: +5.0 % (3second average value);

Measuring point: 33kV Steel Making Bus;

Duration of test: 72 hours;

Location of measurement: 33kV, SVC control panel;

Secondary side PT, Ratio 33/0.11 kV;

Measuring device: Power Quality Analyzer PQ-Box 100 (A-Eberle);

Duration of measurement: 72 hours.

The voltage dips taken during electrode short circuit and/or transformer switching, are allowed to be below the minimum value. Taking out those values, the minimum voltage was 33.05kV and the maximum voltage was 34.3kV.

Design value:

Umin = 33kV+0.5% = 33.16 kV;

Umax = 33kV+5% = 34.5 kV;

ΔU = 1.34 kV.

Measured values:

Umin = 33.05 kV;

Umax = 34.3 kV;

ΔU = 1.25 kV.

Conclusion: the voltage gap ΔU (1.25 kV) is smaller than the required gap ΔU (1.34kV), therefore, the voltage stabilization is fulfilled.

Operation Performance

All the measured values recorded above were found to be matching or below the design limits for the above mentioned tests.

The difference in voltage and MW loading profiles of EAF's from substation Scada with and without SVC operation are shown in Fig. 10.

Table 10 shows the actual EAFs' performance with and without SVC for the same operating conditions.

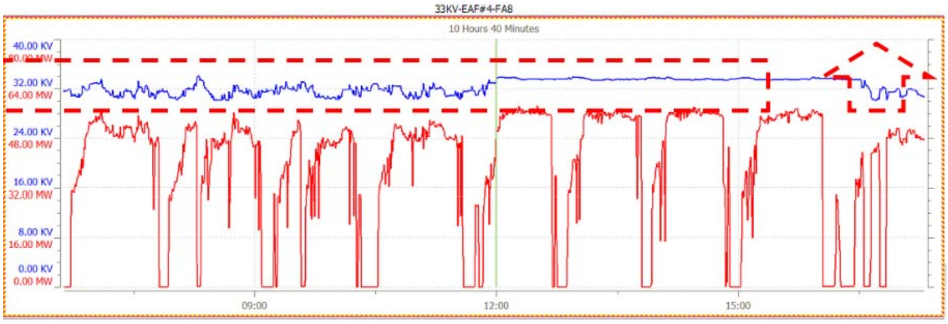

Fig. 10. 33 kV voltage profile with and without SVC operation from Substation SCADA

Table 10 Actual Impact of SVC at same operating Conditions

Comparison Point of View	Planned Figures	Day Without SVC in Operation	Day With SVC in Operation
Tapping Yield %	87.3	86.3	87.3
Availability %	96.5	96.6	96.5
DRI %	70	64.8	65.6
On Tap Time (Min./Heat)	58.56	59.7	54.7
Turn Around Time (Min./Heat)	11.8	12.8	12.7
Delays Time (Min./Heat)	2.6	2.6	3.5
EAF Power KWH/T	565	573.42	562.6
# Heats	77	77	80

Conclusion

This paper showed network analysis for power quality problems' mitigation in steel making plant. Thus the key performance indexes can be easily identified and compared to their standard limits, also other simulation scenarios can be studied in the future based on the same introduced Simulink EAF-SVC models.

The significant operational benefits of SVC application in steel making plants are discussed and compared with actual values. These benefits can be summarized into higher PF reaching 99%, voltage stabilization on the steel making bus with various EAF loading conditions which means increased production and smoother operation and finally lower flickering ($P_{st\ 95\%}$ = 0.68), lower harmonic levels (THVD % = 0.407) which means cleaner bus at PCC.

The financial impact showed that power quality is not only beneficial for utility power grid but also for the plant itself since the operation performance showed decrease in On-Tap time by 5 minutes resulting in increased daily productivity of 3 heats, meaning 1,000 Tons molten steel/year.

Also, the testing results of power quality values were discussed to validate design limits and compare between actual and simulated network reactions for dynamic loading of EAF's during SVC operation.

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