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doi:10.15199/48.2016.06.03

Control of 3-leg 4-wire inverter with passive LC output filter operating with nonlinear unbalanced load

Streszczenie. *Artykuł przedstawia wyniki symulacyjne układu 2 poziomowego, 3 gałęziowego falownika z przewodem neutralnym. Przekształtniki tego typu stosowane są w zasilaczach bezprzerwowych UPS. Zaproponowana struktura sterowania zapewnia stabilizowanie sinusoidalnego napięcia wyjściowego z niską zawartością wyższych harmonicznych przy nieliniowym lub niesymetrycznym obciążeniu. (**Sterowanie 3-gałęziowego 4-przewodowego falownika z filtrem pasywnym LC z nieliniowym lub niesymetrycznym obciążeniem)*

Abstract*. Article presents simulation results of two-level three phase inverter with neutral wire. Such inverters are commonly used in uninterruptible power supplies. The proposed control structure enables sinusoidal output voltage with low THD value under nonlinear or unbalanced load.*

Słowa kluczowe: sterowanie, falownik czteroprzewodowy, UPS, nieliniowe obciążenie, niesymetryczne obciążenie.
Keywords: control, 4-wire inverter, UPS, nonlinear load, nonsymmetrical load.

Introduction

Uninterruptible power supply (UPS) is important part of every system where high reliability and quality of power supply is required. The typical applications of high power UPS (>100kW) are medical equipment, biotechnology, semiconductor manufacturing and data centers. Especially in IT technology, utilization of UPS is getting higher importance. Nowadays, power of the modern data center can easily exceed several MW [1]. Data centers are responsible for handling such sensitive tasks like banking, data storage, online trade etc. It is obvious that in data centers power outage or poor power quality are not acceptable. Even short lack of power may generate massive costs. The task of the UPS is to keep power supply quality at the right level. UPS can operate in different configurations: double conversion, line interactive, standby mode, eco-mode [2]. The most robust method is double conversion configuration, which comprises back-to-back connection of rectifier and inverter and battery storage connected to the DC-link (Fig. 1). In case of grid failure sensitive load is separated from the grid and it is directly, without delay, supplied from the UPS inverter and battery storage. Then, in case of longer failure external diesel generators can start operation and overtake the supply.

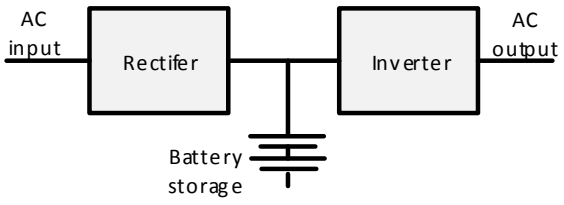

Fig.1. Double conversion UPS configuration

Double-conversion UPS needs to fulfill several requirements which are far more demanding than in motor drives or photovoltaic inverters. First of all, UPS must be able to supply unbalanced loads up 100% (pure single phase load). Secondly, THD of the output voltage should be as low as possible, even with nonlinear loads like diode rectifiers. Moreover, conversion efficiency of modern UPS systems should be far above 95%, which leads to reduced switching frequency and utilization of higher order output AC filters like second-order LC circuit. In order to reduce the size and increase efficiency, modern UPS's has no isolating transformer between load and UPS AC output. For safety reasons galvanic connection of neutral wire between input and output is also required [2].

All of the above issues heavily influents on the inverter topology, control system and utilized modulation technique. To meet all of the requirements 4-wire inverter and high performance control is needed. It should be able to control positive, negative and zero-sequence of the output voltage and deal with higher harmonics in the output current. Moreover, control should be able to minimize circulating current in the neutral wire, which may occur between input and output of the UPS. Recently, control of the UPS inverter stage had been investigated in large number of papers. Both classical and modern control approaches had been analyzed. Papers [3]-[4] propose utilization of repetitive controller which can easily reject periodic distortions, but on contrary has poor performance with aperiodic disturbances. In articles [5]-[6] dead-beat control is investigated. Authors propose modifications of dead-beat in order to deal with system non-idealities, like control delays. In [7] model predictive control is proposed. Algorithm is characterized with good performance, but it bases on the precise model of the system, and it is sensitive to nonlinearities. Further, sliding mode control is investigated in [8]. Unfortunately, paper reports poor performance with asymmetrical loads and complex design of the controller.

The second group of control methods utilizes classic approach with PI regulators and multi-loop control strategy in synchronous reference frame [11]-[12]. In order to maintain low value of THD_U under occurrence of higher harmonics in the output current several modifications are proposed like additional harmonic voltage compensators or decomposition of the three phase signals into positive, negative and zero components. The advantage of the control method is simplicity of tuning PI coefficients and simple implementation of the algorithm in comparison with modern control strategies.

Presented paper concerns control strategy for inverter stage of the high power, three-phase uninterruptible power supply. This work presents UPS inverter topology which enables operation with unbalanced or nonlinear loads. Control system, which is based on PI controllers in synchronous dq0-frame and additional feedforward path is proposed. Moreover simulation results presents influence of output LC filter parameters, like inductance nonlinearity, on the system performance.

System topology

Figure 2 presents topology of the UPS output stage. It comprises voltage balancing circuit, DC-link capacitors, two level inverter and LC star connected output filter. According to figure 1 DC-link is supplied by the UPS rectifier stage with battery storage.

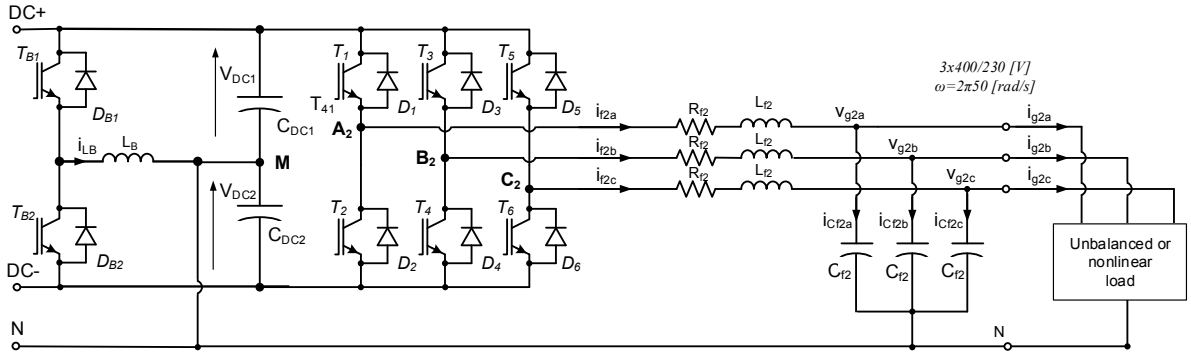

Fig.2. 4-wire UPS inverter stage topology with LC filter

The important part of the output stage is voltage balancing circuit (transistors T_{B1}, T_{B2} and inductor L_B), which is responsible for controlling of the middle of DC-link voltage. Similar balancing circuits are widely analyzed in the four wire systems [13-14]. Transformerless systems are characterized with better efficiency, power density and output voltage quality [15]. However, in such systems proper balancing of the middle point (M) voltage is needed. Voltage balancing circuit operation is similar to buck-boost DC/DC converter. Transistors are switching complementary with dead time. Depending on the duty cycle of switching signal of transistors T_{B1} and T_{B2}, positive or negative average current flows through L_B inductor. In steady state, for 50% duty cycle average current equals zero. Peak-peak ripple value of inductor current equals:

$$\Delta i_{Bp-p} = \frac{U_{DC}}{4 L_B f_{swB}} \tag{1}$$

Where: U_{DC} – DC-link voltage, f_{swB} – switching frequency of the balancing circuit, L_B – balancing inductor value

Balancing circuit operates continuously with constant switching frequency and it is independent from control of rectifier and inverter stage. Circuit enables operation of the inverter with unbalanced and nonlinear three phase loads. Operation of the balancing circuit influences also on the operation of the rectifier stage, but this subject is not the scope of the paper.

The major part of the UPS system is inverter with LC output filter. In comparison with pure L filter, LC enables better THD_u assuming same switching frequency and DC-link voltage. However, filter introduces additional resonance frequency in the system. With a rule of thumb, to omit system stability problems filter parameters need to satisfy equation:

$$10 f_g < \frac{1}{2\pi\sqrt{L_f C_f}} < 0.5 f_{sw} \tag{2}$$

Where: f_{sw} – inverter switching frequency, f_g – grid frequency, L_f – filter inductance, C_f – filter capacitance

Important factor during design of the filter inductance is peak-peak ripple value of the inverter output current:

$$L_f = \frac{U_{DC}}{4 f_{swI} \Delta i_{fp-p}} \tag{3}$$

Where: f_{swI} – inverter switching frequency, Δi_{fp-p} – peak peak value of L_f current ripple

In the model, in order to reduce size of the filter, it was assumed that Δi_{Lf} is equal to very high level: 38% of nominal inverter output current. Value of the filter capacitor can be chosen basing on the maximum voltage ripple of the output voltage under no load conditions:

$$C_f = \frac{1}{\Delta v_{g2p-p}} \left(\frac{\Delta i_{fp-p}}{8 f_{swI}} \right) \tag{4}$$

Where: Δv_{g2p-p}. – ripple peak-peak value of the output phase voltage

In the model it was assumed that voltage ripple will be below 0.5% of nominal peak-peak value of phase voltage.

In the simulations circuit is loaded by the nonlinear load or by linear resistive load. Schematic of the nonlinear load is showed in figure 3. The most demanding part for the control system is a single phase diode rectifier which is strongly unbalanced and generates high-order harmonics in the load current. Similar load is proposed in the IEC norm [2].

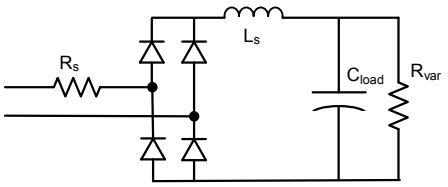

Fig.3. Reference single phase, nonlinear load.

Table 1. Simulation model parameters:

Balancing circuit & DC-link		
f_{swB}	10	[kHz]
L_B	440	[uH]
C_{DC1} / C_{DC2}	12.2	[mF]
U_{DC}	800	[V]
$\Delta i_{B\ p\text{-}p}$	45	[A]
Inverter		
f_{swI}	10	[kHz]
S_n	50	[kVA]
$U_{n\ ph\text{-}ph}$	3x400	[V]
I_n	108	[A]
LC filter		
f_{res}	575	[Hz]
R_f	50	[mΩ]
L_f	170	[uH]
C_f	450	[uF]
$\Delta i_{Lfp\text{-}p}$	117	[A]
$\Delta v_{g2p\text{-}p}$	3.25	[V]
Load parameters		
P_{load}	40/15kW	[kW]
R_s	50	[mΩ]
C_{load}	1	[mF]
R_{var}	7.9	[Ω]
L_s	250	[uH]
R_{linear}	4.4	[Ω]

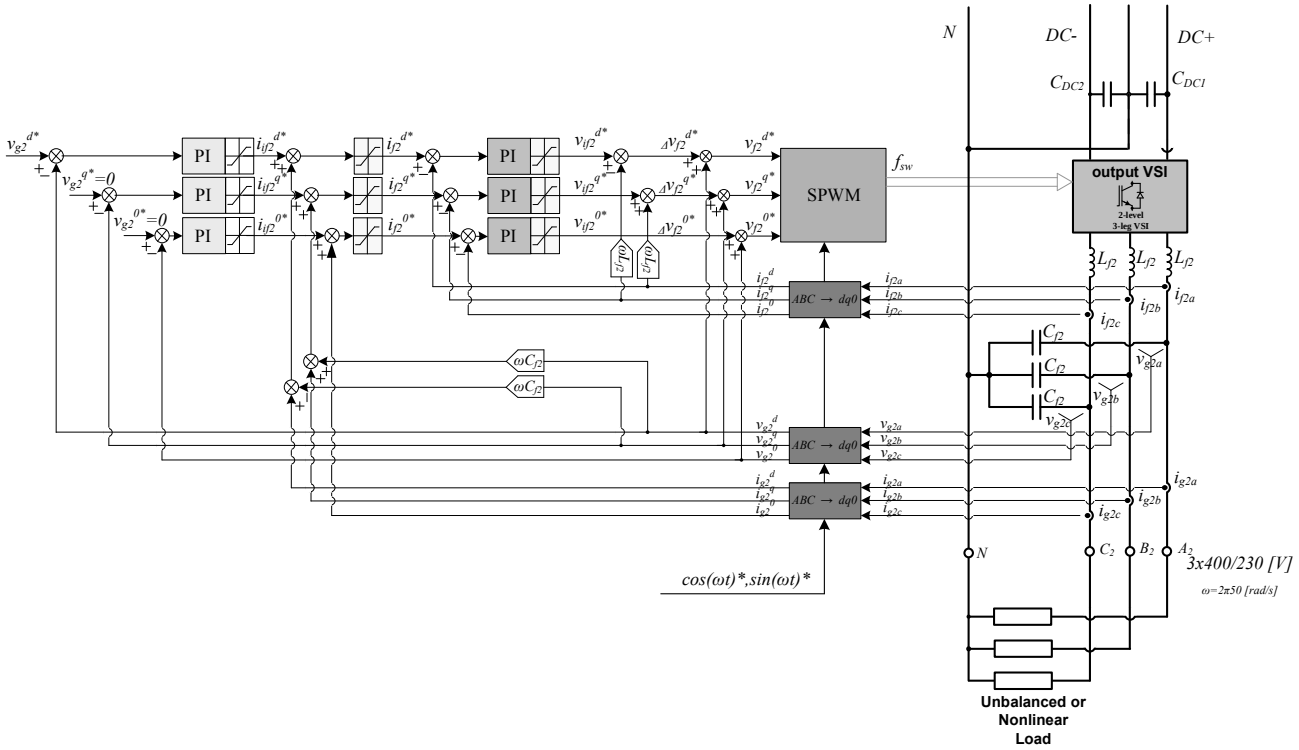

Fig.4. Proposed inverter control structure

Control system description

Figure 4 presents proposed control system of the UPS inverter stage with LC filter. The main aim of the inverter control is to provide three phase sinusoidal voltage with small THD_u even under unbalanced or nonlinear load.

Outer control loop is responsible for tracking of inverter output voltage reference signals (v_{g2}^{dq0*}) and generation of output currents reference signals (i_{f2}^{dq0*}). Faster, inner control loop controls inverter output current. Calculations are made in synchronous dq0-frame. System has four wires, thus zero components of voltage and current signals must be controlled by three PI regulators. Control system uses sinusoidal PWM modulator with zero sequence voltage generation. Inverter output phase voltages cannot be distorted, thus injection of third harmonic component for better utilization of the DC-link voltage is not allowed. Discontinuous PWM techniques for reducing semiconductor switching losses is also not acceptable. UPS inverter needs to handle output currents with content of high order harmonic components. To meet demanding control bandwidth requirements it is proposed to use feed forward control method. Load current (i_{g2abc}) is sampled, transformed into dq0 frame and added to the output of PI regulators. Additionally, basing on the output voltage, LC filter capacitor first order harmonic reactive current is estimated and added to the reference. Finally, the equations for inverter reference output current are equal to:

$$
\begin{aligned}
i_{f2}{}^{d*} &= i_{if2}{}^{d*} + i_{g2}{}^{d} - v_{g2}^{q} \cdot \omega C_{f2} \\
i_{f2}{}^{q*} &= i_{if2}{}^{q*} + i_{g2}{}^{q} + v_{g2}^{d} \cdot \omega C_{f2} \\
i_{f2}{}^{0*} &= i_{if2}{}^{0*} + i_{g2}{}^{0}
\end{aligned}
\tag{5}
$$

The performance of the system with and without feed forward loop will be investigated in the next chapter.

In the current control loop feedforward method is also utilized. Signals which are feed into SPWM modulator are equal to:

$$
\begin{aligned}
v_{f2}{}^{d*} &= v_{if2}{}^{d*} + v_{g2}{}^{d} - i_{f2}^{q} \cdot \omega L_{f2} \\
v_{f2}{}^{q*} &= v_{if2}{}^{q*} + v_{g2}{}^{q} + i_{f2}^{d} \cdot \omega L_{f2} \\
v_{f2}{}^{0*} &= v_{if2}{}^{0*} + v_{g2}{}^{0}
\end{aligned}
\tag{6}
$$

The first term in the equation (v_{if2}^{dq0*}) is output of the PI regulator. Next, feedforward of inverter output voltage is added (v_{g2}^{dq0}). Finally, knowing inverter output current, voltage drop across L_{f2} inductors are compensated.

Figure 5 presents control structure for balancing circuit. It has cascaded structure. External PI controller is responsible for generation of inductor current reference signal. Error signal is obtained by subtracting upper and lower half of the DC link voltage. Faster control loop tracks current reference and generate signal for the comparator. It is possible to simplify control circuit and remove one of internal PI controller, but then control circuit is not acceptable in real implementation, because there is no control of the inductor current and saturation of the core may occur.

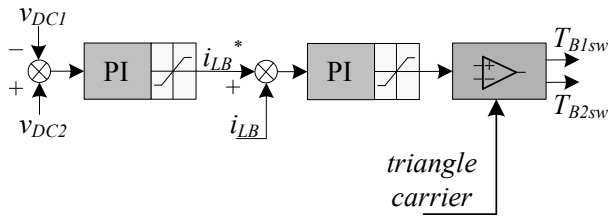

Fig.5. Balancing circuit control structure v_{DC1} – upper half of the DC link voltage, v_{DC2} – lower half of the DC link voltage, I_{LB}^{*} – inductor L_B reference current, I_{LB} – inductor L_B current, T_{B1sw}, T_{B2sw} – transistor switching signals

The last part of the control structure is SPWM modulator, which is shown in Figure 5. In order to improve linearity of the modulator, DC-link variations are compensated by normalization of the reference signals. For dq0->ABC transformation signals from PLL are needed. In

real systems phase lock loop tracks the phase of the input voltage of the UPS system. In the presented model dynamics of the PLL system is not taken into account. Ideal sinusoidal generators are used instead.

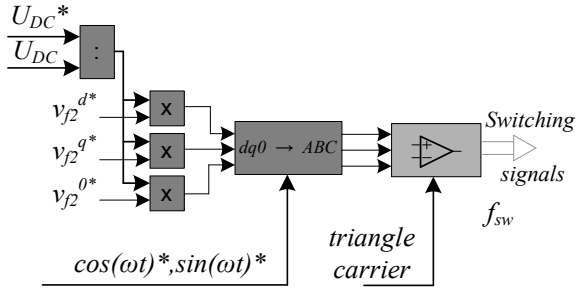

Fig.6. SPWM modulator structure. U_{DC}^{*} – reference DC-link voltage, U_{DC} – measured DC-link voltage, *cos(ωt)*,sin(ωt)** - PLL reference signals

System non-idealities in the simulation model

The common mistake which is encountered in the power electronic simulation models is to not including a system non-idealities. As a consequence, model behaviour is far from experimental results. In order to limit this simulation defects several features are added to the presented model. The most important is PWM delay which strongly limits control system bandwidth. All signals are sampled synchronously at zero and peak of triangle switching carrier (Figure 7). This method is called double-update sampling and provides better performance than updating once per PWM period [16]. However, such method is more demanding for computing unit, which needs to be able to do all the calculations in half of the switching period. In addition to PWM delay, noise and quantization error from analog to digital conversion is also included into the model.

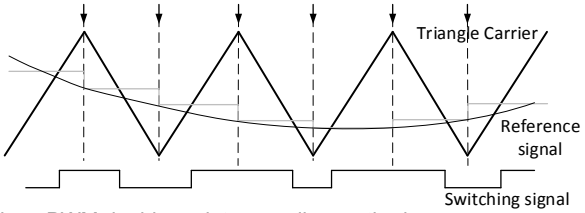

Fig.7. PWM double update sampling method

Second important element which is also taken into account is linearity of the output filter inductor (L_f). To limit weight, size and consequently a cost of the UPS inverter it is necessary to reduce the size of the inductor core. Moreover, highly nonlinear materials like powder cores may be utilized. Figure 8 presents characteristics of two inductors models which were used in the simulations: linear and non-linear with saturable core. Initial inductance for both models is equal 171 [uH]. For high currents inductance of reactor with saturable core is reduced by 35% for 200A. Such behaviour is demanding for control system which should be stable even with very low filter inductance at the output of the inverter. In proposed control system gain of the control loops need to be reduced to provide stable operation under minimal value of inductance. This fact leads to worse performance in comparison with UPS with linear filter.

Finally, transistor switching dead times are also included. In order to properly model dead time distortions it is important to include into the model forward voltage drop and dynamic resistances of semiconductor valves [17].

Parameters of the simulation models are listed in the table 2.

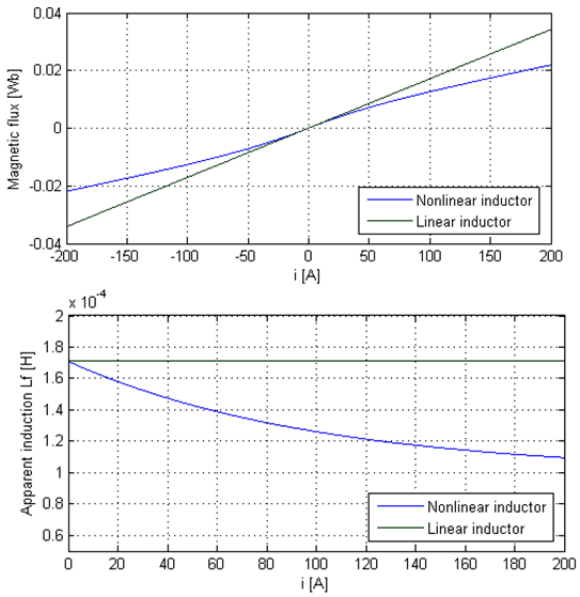

Fig.8. Influence of the nonlinear LC filter on the system performance

Table 2. Simulation model parameters:

ADC parameters		
ADC resolution	12	[bit]
$f_{sampling}$	20	[kHz]
Noise level	2	[bit]
Semiconductor model parameters		
$T_{deadtime}$	3	[us]
$V_{f\ transistor}$	1.7	[V]
$r_{d\ transistor}$	4	[mΩ]
$V_{f\ diode}$	1.1	[V]
$r_{d\ diode}$	3	[mΩ]

Simulation results

This chapter presents results for different configurations of the simulation model. The purpose is to show the performance of the control strategy under different conditions.

Operation under unbalanced or nonlinear loads

Figure 9 presents response of the inverter to step change of the load (0 to 24kW). Inverter is suppling unbalanced resistive load (phase A and B loaded by pure resistor). Control system provides fast settling to reference with only small oscillations at the output voltages.

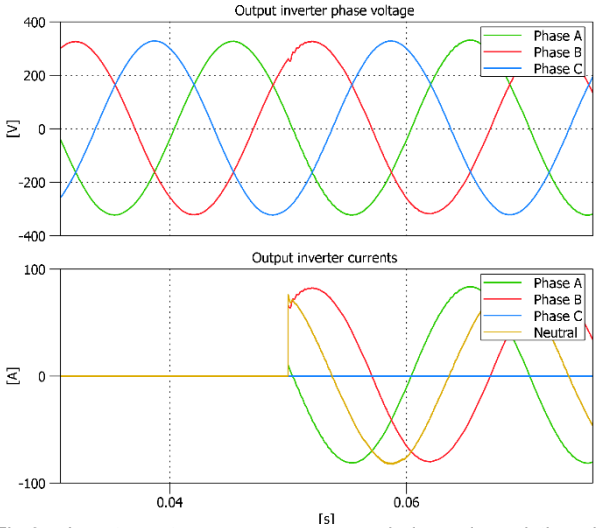

Fig.9. Inverter step response to unbalanced resistive load P=2x12kW, THD_U=1%.

Figure 10 shows inverter output voltage loaded by three phase diode rectifier. Inverter current is discontinuous and its peak value reaches 125A. Even with such demanding load, THD_u of output voltage equals 2%, which fulfills IEC standards [2]

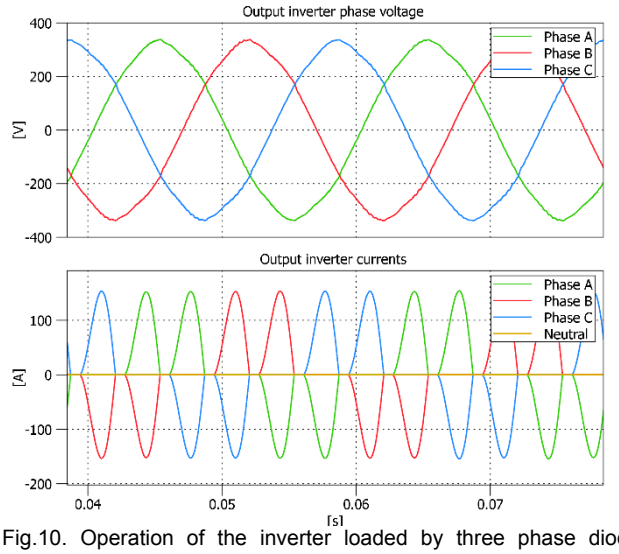

Fig.10. Operation of the inverter loaded by three phase diode rectifier P=40kW, THD_U=2% with current feedforward control loop

Influence of the current feed forward loop on control system performance

Simulation analysis showed that the most important element of control structure which enables regulation of non-sinusoidal inverter output currents is feedforward loop in current controller. (Second terms in equations (5)). With this control strategy it is possible to obtain very fast control with relatively slow switching frequency. The drawback of the method is a need of additional current sensors, which increases cost and complexity of the device.

Figure 11 shows performance of the system with removed feedforward path. Device has same load as in the previous simulation (Fig. 10). It is clearly visible that output voltage is distorted and inverter is not able to track output current. Figures 12 and 13 presents FFT of waveforms showed in figure 10 and 11. Without feedforward loop the 5^{th}, 11^{th} and 13^{th} order voltage harmonic is increased. Respectively those harmonics are reduced in the inverter output current. Peak value of inverter current equals 90A and it is smaller by 28% in comparison with initial results.

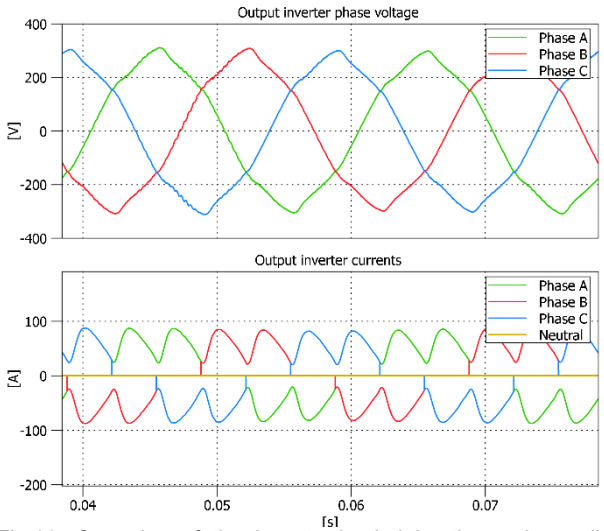

Fig.11. Operation of the inverter loaded by three phase diode rectifier without current feedforward control loop P=40kW, THD_U=5%.

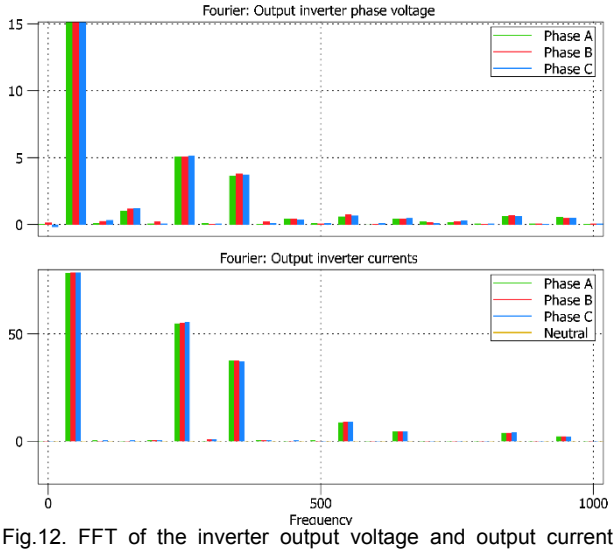

Fig.12. FFT of the inverter output voltage and output current in case when control has current feedforward loop. Inverter loaded by three phase diode rectifier P=40kW

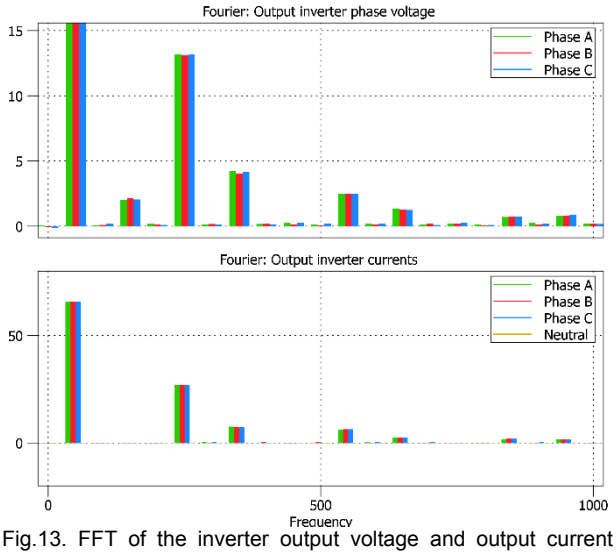

Fig.13. FFT of the inverter output voltage and output current in case when control system without current feedforward control loop. Inverter loaded by three phase diode rectifier P=40kW

Operation of the balancing circuit

Figure 14 presents operation of the balancing circuit. Inverter is loaded by the single phase diode rectifier (Figure 3).

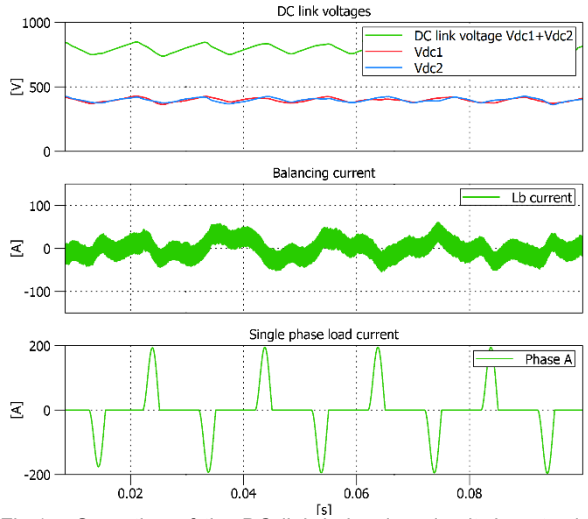

Fig.14. Operation of the DC link balancing circuit. Inverter loaded by single phase diode rectifier.

It is visible that DC-link voltage contains relatively large varying component due to reduced value of DC-link capacitance. Distortions caused by the DC-link ripples are reduced by the normalization of the reference signals in the PWM modulator (Figure 6).

Influence of the inductor nonlinearity on system performance

Figure 15 presents simulation results of the inverter with non-linear AC filter (saturable inductor core – Figure 8). Inverter is loaded by single phase diode rectifier. With increasing output current inductance of the AC filter is significantly reduced. That causes reduction of the stability margin in the control system. In the Figure 15 it is visible that for currents above 150A system is reaching stability border and current start to oscillate with high frequency. To omit this problem gain of the control loop needs to be designed for minimum value of the saturable inductor.

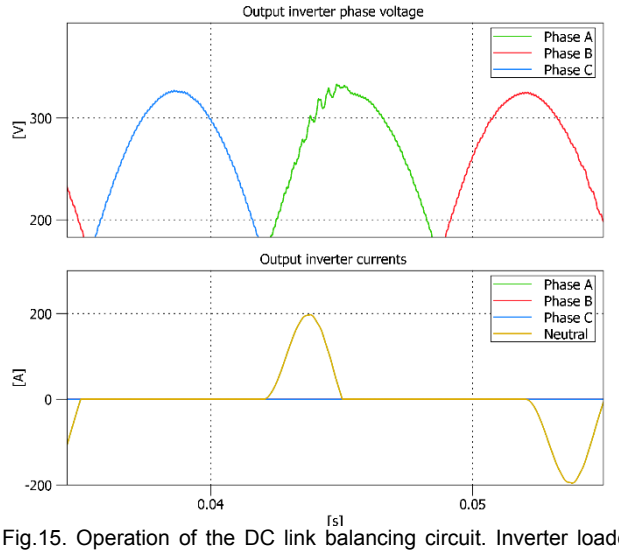

Fig.15. Operation of the DC link balancing circuit. Inverter loaded by single phase diode rectifier.

Summary

Paper presents simulation results of three-phase, four wire UPS inverter stage with unbalanced and nonlinear load. Prepared simulation model took into account computation delays, ADC resolution, sampling synchronization and nonlinearity of the output LC filter. Proposed control strategy, which operates in synchronous dq0 reference frame is able to stabilize sinusoidal output voltage even with diode rectifier. Simulation results confirmed that additional feedforward path improves system performance. Total harmonic distortion of the UPS output voltage with 10 kHz switching frequency is below 3% under most demanding conditions. Results for different loads are listed in table 3.

Table 3. Comparison of output voltage THD_u for different loads.

	Phase A	Phase B	Phase C
No load	0.6%	0.6%	0.6%
Balanced resistive load (P=40kW)	1%	1%	1%
Single phase resistive load (P=15kW, phase A)	1%	0.6%	0.6%
Three phase nonlinear load (P=40kW)	2,0%	2,0%	2,0%
Single phase nonlinear load (Phase A P=15kW)	1.2%	0.6%	0.7%

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REFERENCES

[1] Johnson B., Pike G.E., Thermal considerations in cooling large scale high compute density data centers, The Eighth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, 2002, 767-776

[2] Uninterruptible power systems (UPS) – Part 3: Method of specifying the performance and test requirements, International standard IEC 62040-3, Edition 2.0, 2011

[3] Gnoatto C. L., Scarmin A., Carati E. G., Repetitive Control Techniques Applied to Uninterruptible Power Supplies, *9th* IEEE/IAS International Conference on Industry Applications (INDUSCON), 2010, 1-6

[4] Shuai Jiang, Dong Cao, Fang Z., Peng Yuan Li, Jianfeng Liu: Low THD, Fast Transient, and Cost-Effective Synchronous-Frame Repetitive Controller for Three- Phase UPS Inverters, *IEEE Transactions on Power Electronics,* 27(2012), n.6, 2994-3005

[5] Jun-Seok Cho, Seung-Yo Lee, Hyung-Soo Mok, Gyu-Ha Choe, Analysis and Design of Modified Deadbeat Controller for 3-Phase Uninterruptible Power Supply, Proceedings of the IEEE 1999 International Conference on Power Electronics and Drive Systems, 2 (1999), 1003-1009

[6] Meng WANG, Fangzheng LI, Yadong LIU, Lipei HUANG, Makoto SAKANE, Distributed Parallel Operation of Modified Deadbeat Controlled UPS Inverters, *Power Electronics Specialists Conference,* 2007, 1727-1732

[7] Cortés P., Ortiz G., Yuz J. I., Rodríguez J., Vazquez S. and Franquelo L. G., Model Predictive Control of an Inverter With Output LC Filter for UPS Applications, *IEEE Transactions on Industrial Electronics,* 56(2009), n.6, 1875-1883

[8] Korondi P., Hashimoto H., Park vector based Sliding Mode Control of UPS with unbalanced and nonlinear load, *Lecture Notes in Control and Information Sciences,* 247(1999), 193-209

[11] Mattavelli P., Synchronous-Frame Harmonic Control for High-Performance AC Power Supplies, *IEEE Transactions on Industry Applications,* 37 (2001), n.3, 864-872

[12] Kyung-Hwan KimNam-Joo Park, Dong-Seok Hyun, Advanced Synchronous Reference Frame Controller for three-Phase UPS Powering Unbalanced and Nonlinear Loads, IEEE 36th Power Electronics Specialists Conference, 2005, 1699-1704

[13] Rodriguez P., Luna A., Teodorescu R., Blaabjerg F., Liserre M., Control of a three-phase four-wire shunt-active power filter based on DC-bus energy regulation, 11th International Conference on Optimization of Electrical and Electronic Equipment, 2008, 227-234

[14] Qing-Chang Zhong, T.C. Green, Jun Liang, G. Weiss, H∞ control of the neutral point in 3-phase 4-wire DC-AC converters, IECON 02 Annual Conference of the Industrial Electronics Society, 2002, 520-525

[15] Gunes I., Ustuntepe B., Hava A.M., Modern transformerless uninterruptable power supply (UPS) systems, International Conference on Electrical and Electronics Engineering, 2009, 316-320

[16] Hoffmann N., Fuchs F., Dannehl J., Models and effects of different updating and sampling concepts to the control of grid-connected PWM converters — A study based on discrete time domain analysis, Conference on Power Electronics and Applications (EPE 2011), 2011,1-10

[17] Sikorski A., Korzeniewski M., Ruszczyk A., Identification of Dead-Time Influence on The Output Voltage of the Inverter Controlled by Non-Linear Controllers, The International Conference on "Computer as a Tool" EUROCON, 2007, 1896-1901