

Analysis and design of high efficiency DC/DC buck converter

Abstract. This article presents the project and a practical realisation of a DC/DC buck converter. The measurements of system's functionality were performing in certain operating points (power, switching frequency of the transistor). In addition the analysis of power losses for chosen elements (transistor, inductor) used to build a converter was performed.

Streszczenie. W artykule przedstawiono projekt oraz praktyczną realizację układu przekształtnika obniżającego napięcie DC/DC typu buck. Wykonano pomiary sprawności układu w określonych punktach pracy (moc, częstotliwość pracy tranzystora) oraz przeprowadzono analizę podziału strat mocy dla wybranych elementów (tranzystor, dławik) wykorzystanych do budowy przekształtnika. (Analiza i projektowanie wysokiej sprawności przekształtnika DC/DC typu buck)

Keywords: silicon carbide (SiC), high speed IGBT, buck converter, power losses, efficiency.

Słowa kluczowe: węgiel krzemu (SiC), szybkie tranzystory IGBT, przekształtnik obniżający, straty mocy, sprawność.

Introduction

This paper describes a study of DC/DC buck converter. Main aim of this research was to design the buck converter with high efficiency. This converter is a stage of energy conversion which has to regulate output voltage in a manner that voltage matches to the load requirements. The standard topology of buck converter (Fig. 2) remains unchanged while its components are the subject of optimization. The investigation was focused on two crucial components: semiconductor valve and filtering inductor. The SiC Schottky diode has been chosen as circulating diode (or freewheeling diode) by default. Nowadays this type of diode is commonly considered as the most suitable and efficient solution [1].

Continuously rising demands for high efficiency and recently introduced new materials and components have become the motivation for research described in the paper. The components selection for optimization process is determined by expected power range of converter equal 4 kW ($V_{out} = 550$ V, $I_{out} = 7.3$ A). Whole converter has to work with switching frequency in kilohertz range to minimize size of passive components of output filter.

Based on the figures from components' datasheets [2, 3] the two candidates of semiconductor valve have been selected. The first one is representing the mature technology of transistors manufacturing based on silicon oxide - High speed IGBT (IKW25N120H3). The second one is representing a newly developed technology based on silicon carbide material – SiC Mosfet (C2M0080120D). Both components are promising low switching losses.

Authors decided to investigate two type of chokes as an inductive component made of the material that allows operation with high induction B. It is necessary condition to be able to minimize size of the magnetic core. The first choke has been made on amorphous ribbon with cut discrete air gap – AMCC-250 Metglas [4]. The second one has been made on core with distributed air gap – SuperMSS [5]. Both type of cores are considered as low loss materials suitable for design high efficient power converters.

The process of converter components design can be supported by simulations or analytic calculation only in a limited way [6, 7]. It is because of simplified models of semiconductor components and magnetic materials. Models of transistors used in circuit simulations nicely represent their electric behaviour but losses are purely represented by averaged models. Similar comment also relates to inductive choke where not only magnetic core

modelling is complex but the losses of choke's windings are difficult to predict (because of skin and proximity effects).

Authors are investigating the standard topology of DC/DC buck converter with two types of semiconductor components and two types of inductive components. Initial analytic calculation of average losses in converter are verified by measurement of the laboratory setup. Real measurements are taking into account losses of all parts of converter that normally are neglected in analytic calculation. Measurement has been taken in function of switching frequency in range of 5 to 60 kHz. It allows authors to make the conclusion about optimal switching frequency of buck converter in which the proposed design has minimal losses.

The analysis of a split of losses in the buck converter

The total efficiency of the buck converter is determined by many components. They depend on operation condition (as value of current, voltage or frequency), used electronic devices, a printed circuit manufacturing technology or routing a conducting paths connecting individual devices [8]. However, there is no doubt that the most significant part of total losses ΣP of converter is related to losses in semiconductors (P_{semi}) and the induction losses in a choke (P_{ind}). Therefore total losses can be described with good approximation as $\Sigma P = P_{semi} + P_{ind}$.

The semiconductor losses P_{semi} are the sum of conduction losses P_{con} and switching losses P_{sw} formed during the commutation processes. Therefore the semiconductor losses are represented by sum of conduction and switching losses $P_{semi} = P_{con} + P_{sw}$. The induction losses P_{ind} of a choke are composed of core losses P_{cor} in ferromagnetic core and ohmic losses P_{cu} in choke windings. Therefore the induction losses are represented by sum of core losses and ohmic losses $P_{ind} = P_{cor} + P_{cu}$. The ohmic losses are determined by resistance of windings for direct current (DC), although effective resistance of windings for alternating current (AC) is affected by proximity and skin effect, so ohmic losses for AC current too. The core losses mainly depend on type of used ferromagnetic material. These losses are commonly described as a sum of hysteretic losses, eddy current losses and excess losses. The last one component is insignificantly small, so in practice neglected for first approximation calculation. The eddy current losses are directly proportional to the power function of peak magnetic induction and to the operating frequency [9]. The general schema of power loss division in DC/DC converter is depicted in figure 1.

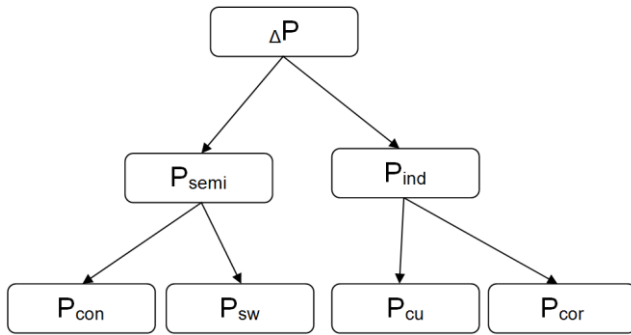


Fig.1. The general schema of power loss division in DC/DC converter

The analytical power loss calculation

The power loss estimation for the particular components of the converter was done based on datasheet information of the examined semiconductor devices [2, 3] and the characteristics of core materials of examined chokes [4, 5] it has been done by use of relations available from literature [9, 10, 11]. For the calculations the steady state point of operation has been taken ($V_{in} = 550$ V, $V_o = 275$ V, $I_o = 3.64$ A, $f_{sw} = 30$ kHz) where two type of transistors – SiC MOSFET and Si IGBT – has been tested. The same silicon carbide (SiC) Schottky diode C4D30120D has been used together with each transistor.

The conduction losses (P_{con}) of semiconductor components can be calculated as follow:

- conduction losses of SiC-MOSFET - C2M0080120D - are calculated for $R_{DSon} = 84.6$ m Ω

$$(1) \quad I_{Drms} = I_o \sqrt{d} = 2.57 \text{ A}$$

where: d – duty cycle coefficient equal 0,5

$$(2) \quad P_{Tcon} = I_{Drms}^2 R_{DSon} = 0.56 \text{ W}$$

- conduction losses of Si-IGBT - IKW25N120H3 - are calculated for $r_{CE} = 27$ m Ω , $V_{CE}(I_{Cav}) = 1.6$ V

$$(3) \quad I_{Cav} = I_o d = 1.82 \text{ A}$$

$$(4) \quad P_{Tcon} = I_{Cav} V_{CE} + I_{Crms}^2 r_{CE} = 3.1 \text{ W}$$

- conduction losses of SiC Schottky diode - C4D30120D - are calculated for $V_F = 0.97$ V, $r_f = 21$ m Ω

$$(5) \quad I_{Dav} = I_o (1-d) = 1.82 \text{ A}$$

$$(6) \quad P_{Tcon} = I_{Dav} V_{CE} + I_{Drms}^2 r_f = 1.9 \text{ W}$$

The switching losses P_{sw} for transistors can be calculated as follow:

- switching losses for SiC-MOSFET - C2M0080120D – are calculated for $E_{on} = 0.45$ mJ, $E_{off} = 0.27$ mJ, $f_{sw} = 30$ kHz, $I_{DN} = 20$ A, $V_{DSN} = 800$ V

$$(7a) \quad P_{sw} = (E_{on} + E_{off}) \frac{I_D}{I_{DN}} \frac{V_{DS}}{V_{DSN}} f_{sw} = 2.7 \text{ W}$$

- switching losses for Si-IGBT - IKW25N120H3 – are calculated for $E_{on} = 0.8$ mJ, $E_{off} = 0.45$ mJ, $f_{sw} = 30$ kHz, $I_{CN} = 25$ A, $V_{CEN} = 600$ V

$$(7b) \quad P_{sw} = (E_{on} + E_{off}) \frac{I_C}{I_{CN}} \frac{V_{CE}}{V_{CEN}} f_{sw} = 5 \text{ W}$$

Switching losses of SiC Schottky diode has been omitted in the switching loss calculation due to negligibly small recombination current I_{rr} of Schottky junction.

The DEMS-55/0.33/25 type choke has been selected as an inductive component with following parameters:

- inductance - $L = 0.33$ mH,
- number of turns - $N = 36$,
- winding resistance - $R_{Cu} = 32$ m Ω ,
- core cross section - $A_e = 4.17$ cm²,
- core volume $V_e = 51.4$ cm³.

The assumed ripples of current are $\Delta I_L = 6.95$ A.

$$(8) \quad I_{LACrms} = \sqrt{\left(\frac{\Delta I_L}{2}\right)^2} / 3 = 2.0 \text{ A}$$

$$(9) \quad I_{Lrms} = \sqrt{I_{LDC}^2 + I_{LACrms}^2} = 4.14 \text{ A}$$

$$(10) \quad P_{Cu} = R_{Cu} \cdot I_{Lrms}^2 = 0.55 \text{ W}$$

Equation (10) gives the value of ohmic losses. However, the R_{Cu} don't consider the resistance change because of temperature rise, proximity effect or skin effect. On the other hand, the winding is wound with litz wire that for relatively low frequency ($f_{sw} \leq 60$ kHz) minimize influence of two last mentioned phenomenons.

The core losses P_{cor} are calculated as follow:

$$(11) \quad \Delta B = \frac{L \cdot \Delta I_L}{N \cdot A_e} = 0.153 \text{ T}$$

Having the value of peak inductance ΔB calculated in equation (11) and based on core material datasheet (SuperMSS, $\mu = 60$) volumetric power loss has been read $P_{cor_spec} = 60$ mW/cm³ for $\Delta B/2$. So, core losses for selected choke are

$$(12) \quad P_{cor1} = P_{cor_spec} \cdot V_e = 3.1 \text{ W}$$

The total required inductance of a L choke is calculated in chapter "Laboratory model of DC/DC buck converter" and has to be about 0.631 mH. For that reason two chokes (DEMS-55/0.33/25) have to be used in series connection to achieve total inductance equal 0.66 mH, which can satisfy output filter in term of output current ripples. Therefore, all losses referred to inductive components taken into account for losses estimation calculation are double. All losses are summarized in table 1.

Table 1. The estimation of power losses in DC/DC buck converter

Transistor	SiC-MOSFET C2M0080120D	Si-IGBT IKW25N120H3
Conduction losses P_{Tcon}	0.56 [W]	3.1 [W]
Switching losses P_{sw}	2.7 [W]	5.0 [W]
Schottky diode		
SiC-Diode C4D30120D		
Conduction losses P_{Dcon}	1.9 [W]	
Choke		
2x DEMS-55/0.33/25		
Ohmic losses P_{Cu}	1.1 [W]	
Core losses P_{cor}	6.2 [W]	
ΣP	12.5 [W]	17.4 [W]

The rough calculation of losses confirms that definitely lower losses should be expected in converter entirely built of silicon carbide components (SiC). However, it should be remembered that a number of simplifications has been

done in presented analytic calculations. Moreover, all calculation presented in table 1 have been done for a single switching frequency f_{sw} . Therefore it is hard to expect that these values could precisely reflect the real picture.

Losses of semiconductor and inductive devices are taking the most significant part in share of total losses. Analytic calculation of losses in semiconductor are a subject of considerable uncertainty because of non-linear behaviour of semiconductor structure in function of temperature, blocked voltage, load current and gate control circuit. A plenty of methods for loss calculation in IGBT [12, 13, 14] and MOSFET [15,16,17,18] can be found in literature.

The calculation of losses for inductive components is even more complicated than for semiconductors. In practice they depend on choke design - including core shape, air gap number and size, type of windings - used materials for core and winding and operating condition like temperature and excitation current – frequency, current shape and DC bias. One can find a lot of attempts to make the calculation of core losses simpler [19] or more complex [20] based on Steinmetz [21] or Preisach model [22] or scaling theory [23, 24]. Regardless of that how advanced model is the analytical calculations can be considered only as preliminary validation.

Laboratory model of DC/DC buck converter

The laboratory setup with DC/DC buck converter has been made for final verification of possible improvements of converter's efficiency. The converter has classic topology of buck converter (Fig. 2) with in series connected transistor T and freewheeling diode D in parallel to the output of LC low-pass filter. Converter can operate in two modes of modulation. The Continuous Current Modulation (CCM) or the Discontinuous Current Modulation (DCM) that depends on character of current conducted by inductance. The analysis of converter operating in CCM mode has only been done in this paper. In CCM mode the voltage control is performed by the change of duty cycle coefficient d according to the equation (13):

$$(13) \quad V_o = d \cdot V_{in}$$

where: d – duty cycle coefficient: $0 \leq d \leq 1$, V_{in} – input voltage, V_o – output voltage.

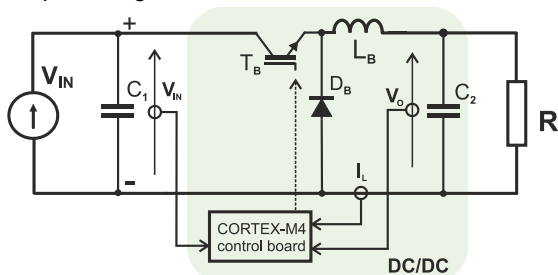


Fig.2. Diagram of DC/DC buck converter

The output filter LC parameters, switching frequency, and load capacity have influence on behaviour of converter. For the steady state it is possible to determine a value of L inductor making an assumption on input and output voltage V_{in} , V_o , switching frequency f_{sw} and allowed current ripples ΔI_L in inductor. Its value can be calculated based on equation (13).

$$(13) \quad L = \frac{V_{in}}{f_{sw} \Delta I_L} d(1-d)$$

The laboratory model of converter for 4 kW power range has been supplied from direct current voltage source equal

$V_{in} = 550$ V. Converter ensured the control of output voltage V_{out} within 50 to 550 V.

The digital control signal for switching transistor T is generated by external board with Cortex-M4 microcontroller. Its frequency can be set from 5 kHz up to 60 kHz. Digital control signal is gained by specialized gate driver integrated circuit (FOD8332 – Fairchild Semiconductor). Gate driver is feeding the gate terminal of switching transistor simultaneously providing required galvanic isolation between control and power circuits. The isolated output side of a gate drive is supplied by DC/DC converter with galvanic isolation located as close as possible to transistor terminals. This can minimize strain inductances in the gate circuit. The tests of converter consider the measurement sequences with two different type of transistors (Si-IGBT and SiC-MOSFET). The supply voltage value at the output side of gate driver chip (FOD8332) was set depending on the type of installed power transistor. This has been done to match their requirements to ensure the optimal switching conditions. SiC-MOSFET transistor requires +20/0 V level while high speed Si-IGBT needs only +15/0 V level. The gate resistor R_G limiting gate charge current of transistor remains the same for both type of transistors. Its value was 10 Ω .

The design of power circuit structure allows for the measurement of the voltage and current at the majority of components. Moreover, the location of power devices (transistor, diode, choke) on the printed circuit board (PCB) allows the user for quick replacement of components. This has been achieved without compromising the converters functionality keeping internal connections as short as possible to minimize parasitic capacitances and strain inductances of the circuit.

The output filter capacitance C is made of two polypropylene foil capacitors MKP1848 connected in series. The single capacitor value was $C = 60 \mu\text{F}/800$ V. The characteristic feature of foil capacitors is their extremely low equivalent series resistance (ESR). These capacitors ensure fast reloads with high currents with impulse character and frequency in range of tens kHz.

The laboratory model of DC/DC buck converter built in accordance to the above description is presented in figure 3. This model has been used for analyses of converter power loss division between different components of converter. The efficiency measurement was done for different switching (modulation) frequencies f_{sw} , different inductances of choke L and different types of transistor. Making the assumption of maximum amplitude of current ripples $\Delta I_L = 2 \times I_o = 7.26$ A, the transistor duty cycle $d = 0.5$ and switching frequency $f_{sw} = 30$ kHz the value of choke inductance $L = 0.631$ mH has been calculated by use of equation (14). The types and values of components used in test are gathered in table 2 for transistors and table 3 for inductances. In each tested configuration the same freewheeling diode has been used (SiC Schottky diode C4D30120D). Value of L_1 inductance is equal to two in series connected chokes type DEMS-55/0.33/25. Value of L_2 inductance is achieved by series connection of three the same chokes DEMS-55/0.33/25. The third inductance L_3 , in contrary to the earlier mentioned, was made on cut amorphous core. Unlike the chokes DEMS-55 where core has low relative magnetic permeability ($\mu = 60$) representing distributed air gap, the amorphous material has very high permeability ($\mu > 45$ k) and air gap has discrete form. It has serious consequences in choke behaviour like fringing flux distribution or linearity of inductance. But in this case the most important is practical verification of choke losses. L_3

inductance has been made on AMCC-250 core. Winding made of litz wire with number of turns $N = 88$. Total inductance of this choke is 4.5 mH. It is about 7 times the required inductance. There are some additional consequences for higher inductance. Negative consequence is oversized an inductor. Positive one are lower current ripples that smoothen inductor's current and output voltage. The advantage of smaller current ripples is that they have the positive influence on the induction peak ΔB which should result on the other hand with lower losses in the core for the same switching frequency. Winding resistance is comparable to resistance of L_1 and L_2 chokes. For detail please look into table 3.

Table 2. Main parameters of semiconductor components

Type	Current [A]	Breakdown voltage [V]	Voltage drop ON-resistance
SiC-MOSFET C2M0080120D	$I_D = 24$ A ($T_c = 100^\circ\text{C}$)	1200	$R_{DSon} = 80$ m Ω
Si-IGBT IKW25N120H3	$I_C = 25$ A ($T_c = 80^\circ\text{C}$)		$V_{CEsat} = 2.05$ V
SiC Diode C4D30120D	$I_F = 43$ A ($T_c = 135^\circ\text{C}$)		$V_F = 1.8$ V

Table 3. Main parameters of inductors

Name	Inductance [mH]	Core type	Winding resistance
L_1	0.66 mH	EMS-0552825-060 by Micrometals	64 m Ω
L_2	0.99 mH		96 m Ω
L_3	4.5 mH	AMCC-250 Metglas by Hitachi	70 m Ω

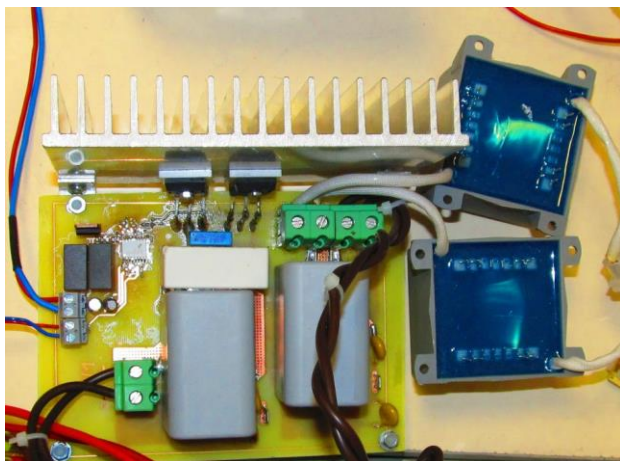


Fig.3. The laboratory test setup of DC/DC buck converter - (top view)

Results of laboratory measurements

The total loss ΣP measurement of buck converter has been done for operating set point (constant value of V_{in} , V_o , I_o). The Yokogawa WT1600 power analyser connected with measured circuit - as shown in figure 4 - was used for total power measurement. The measurement of buck converter with L_1 and L_2 choke has been done for 10 kHz to 60 kHz frequency range. The same measurements with L_3 choke has been done for extended frequency (5 kHz to 60 kHz) due to the higher inductance of L_3 choke and smaller current ripples ΔI_L . For L_3 choke converter was able to operate in CCM with 5 kHz while for choke L_1 and L_2 the limit for CCM was about 10 Hz. Results of total power loss ΣP measured in function of switching frequency for different type of chokes and different transistor's technologies are presented in (Fig. 5, 6, 7).

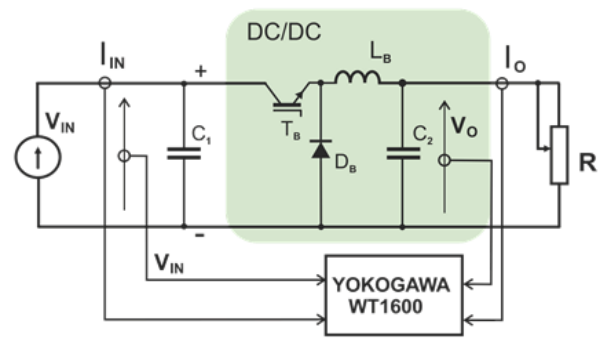


Fig.4. Buck converter and power analyzer connection diagram

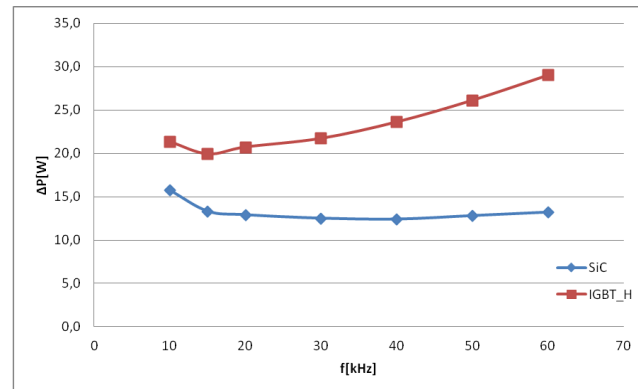


Fig.5. The buck converter total power loss in function of switching frequency $\Sigma P = f(f_{sw})$. Converter with installed inductance $L_1 = 0.66$ mH.

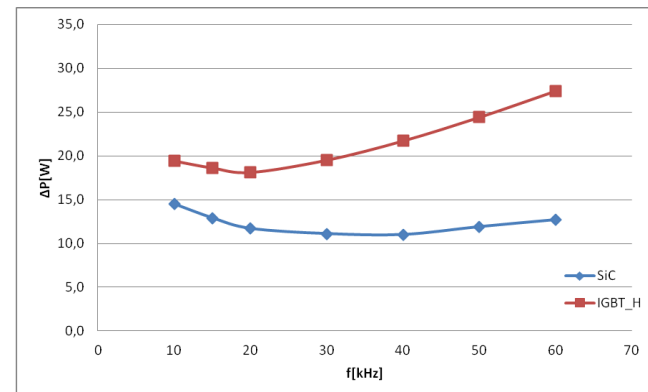


Fig. 6. The buck converter total power loss in function of switching frequency $\Sigma P = f(f_{sw})$. Converter with installed inductance $L_2 = 0.99$ mH.

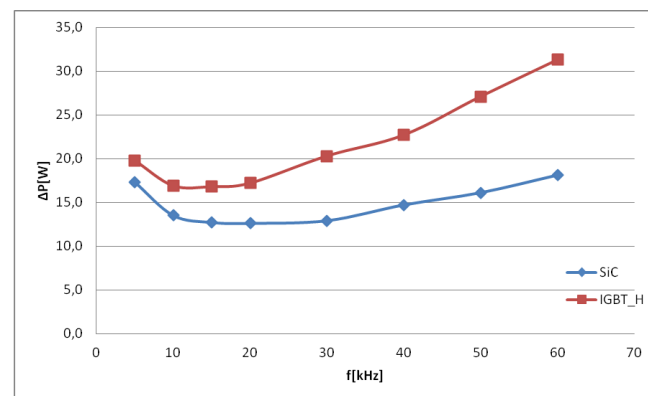


Fig.7. The buck converter total power loss in function of switching frequency $\Sigma P = f(f_{sw})$. Converter with installed inductance $L_3 = 4.5$ mH.

As can be observed the total losses for converter with SiC-MOSFET transistor are significantly lower compare to converter with High-Speed Si-IGBT transistor. It is independent to used inductor and switching frequency. This difference is coming out from lower conduction losses in SiC-MOSFET than in Si-IGBT. The conducted measures confirm higher switching losses P_{sw} in Si-IGBT too. This result confirms the analytical estimations done in chapter above.

The Si-IGBT technology is characterized by higher loss energy - E_{on} and E_{off} - during commutation process. Therefore the difference in total losses for converter built on SiC-MOSFET and Si-IGBT is growing with switching frequency (Fig. 5, 6, 7). At maximum switching frequency $f_{sw} = 60$ kHz the total losses in converter with Si-IGBT compare to SiC-MOSFET are almost double (Fig. 5, 6, 7). The comparison of total losses in buck-converter with L_1 choke shows that the losses calculated analytically (Tab. 1) for switching frequency $f_{sw} = 30$ kHz are lower than this measured in laboratory setup (Fig.5). Losses for SiC-MOSFET are almost the same as analytically calculated (12.5 W), but losses for Si-IGBT are significantly higher (22 W compare to 17.4 W). This difference is coming out from major simplification assumptions. One of them is neglecting the influence of temperature rise on power losses. The contribution of conduction losses P_{con} is higher than switching losses P_{sw} in the total losses for lower switching frequency $f_{sw} = 5$ kHz (Fig. 7).

In two figures bellow the comparison of total losses for the converter with three different chokes (L_1 , L_2 , L_3) has been presented. This is made for converter with SiC-MOSFET transistor in (Fig. 8) and with Si-IGBT in (Fig. 9).

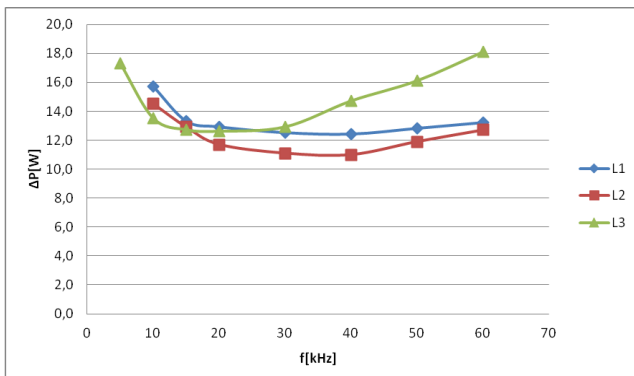


Fig.8. The total losses $\Sigma P = f(f_{sw})$ in buck-converter for different type of choke (L_1 , L_2 , L_3). The buck-converter operates with SiC-MOSFET transistor

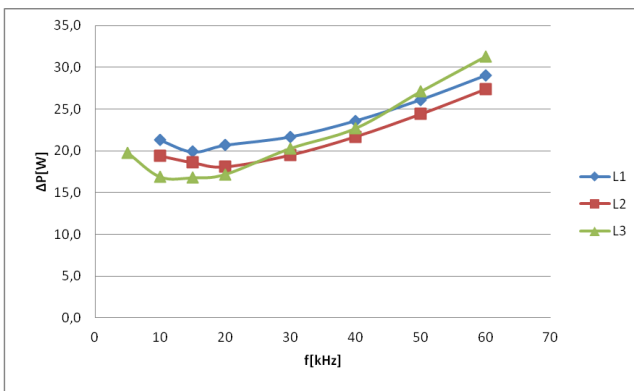


Fig.9. The total losses $\Sigma P = f(f_{sw})$ in buck-converter for different type of choke (L_1 , L_2 , L_3). The buck-converter operates with Si-IGBT High Speed transistor

The choke core losses are described by Steinmetz equation frequently [21] :

$$(14) \quad P_{cor} = kf^\alpha B_{pk}^\beta$$

where: k , α , β – Steinmetz equ. coefficients

It is simplified equation valid for single harmonic sinusoidal excitation without DC bias. When excitation signal is different from sinusoidal (e.g. triangular) with DC bias the more sophisticated equation can be used [20].

According to the equation (14) the core losses are function of excitation signal frequency (switching frequency f_{sw}) and magnitude of induction ripples B_{pk} . Coefficients k , α and β are specific for certain core material and shape. The equation (14) shows that a change of frequency is affecting on core losses. On the other hand the change of frequency is changing the induction peak value B_{pk} .

From analysis of characteristics presented in figure 8 and figure 9 one can observe that each curve has its own minimum for specific switching frequency f_{sw} .

In case of buck-converter with choke $L_1 = 0.66$ mH (2x DEMS-55/0.33/25) or $L_2 = 0.99$ mH (3x DEMS-55/0.33/25) the switching frequency where a minimum of losses is observed is in the range of $f_{sw} <30..40>$ kHz. Operation of buck-converter with switching frequency below 30 kHz will cause the increase of power losses due to a rise of core losses associated with increase of induction ripples ΔB ($\Delta B \sim \Delta I_L$). On the other hand the operation of buck-converter with switching frequency above 40 kHz will cause the increase of power losses due to significant increase of transistor switching losses and eddy current core losses.

In the buck-converter with choke $L_3 = 4.5$ mH (AMCC-250 Metglas core) the switching frequency where a minimum of losses is observed is in a range of $f_{sw} <10..20>$ kHz. Generally, Metglas amorphous cores are dedicated for operation with lower frequencies compare to Sendust based cores.

The operating points for the lowest measured losses for particular components setups are listed in table 4.

Table 4. The operating points where the lowest losses has been measured

SiC-MOSFET C2M0080120D			
	ΣP [W]	η [%]	f_{sw} [kHz]
L_1	12.6	98.8	40
L_2	11.0	98.9	40
L_3	12.7	98.7	20
Si-IGBT IKW25N120H3			
L_1	19.9	98.0	15
L_2	18.1	98.2	20
L_3	16.8	98.3	15

Conclusion

The results of comparison of buck converter efficiency are presented in this paper. The measures were made in the fixed operation point. The best results have been achieved in setup with L_2 choke and SiC-MOSFET transistor operating with switching frequency $f_{sw} = 40$ kHz where total losses are equal 11 W. Slightly worse result was achieved with L_1 and L_3 inductances. From economical point of view, considering the size of whole device, the worst configuration is a case with choke L_3 . The buck-converter with L_1 choke, although with slightly higher losses, looks the best option taking into account the size and cost of whole device. Buck converter setup with IGBT transistor

and L_3 choke had the lowest total losses equal 16.8 W for switching frequency $f_{sw} = 15$ kHz. One can say that the total losses in this case are higher by about 53% comparing to the best case with SiC-MOSFET transistor (results bolded in Table 4). In this configuration the majority of losses are dispersed in IGBT transistor. It is visible as higher temperature of transistor's heatsink.

Received results are pointing out that there is certain switching frequency for each selected combination of used components, for which power losses are the lowest. The change of switching frequency from optimum efficiency point causes the increase of losses due to the higher switching losses for high frequency or higher core losses for low frequency. Presented results confirm that SiC-MOSFET transistor is characterized with lower conduction and switching losses. Its use allows for higher switching frequency operation. Therefore, for converter design, chokes with lower inductances can be used (L_1, L_2). These chokes have smaller dimensions in comparison to choke L_3 . Lower transistor losses have impact on lower operation temperature of semiconductor components located on common heatsink. It allows to minimize the size of radiator and thus the size of whole converter or for resignation from the cooling fan and thus improved reliability of converter.

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REFERENCES

- [1] Krupa, A., Tomaszuk A., Comparison of power losses in hard switched applications using silicon carbide power semiconductors, *Poznan University of Technology Academic Journals. Electrical Engineering*, (2012), 35-38
- [2] Infineon, IKW25N120H3 Rev. 1.2 2010-02-10 - manufacturer datasheet (available, July 2015), source: <http://www.infineon.com/>
- [3] Cree, C2M0080120D Rev B - manufacturer datasheet (available July 2015), source: <http://www.cree.com/>
- [4] Hitachi, - manufacturer datasheet (available July 2015), source: <http://www.hitachimetals.com/product/amorphous/powerliteinductorcores/>
- [5] Micrometals, - manufacturer datasheet (available July 2015), source: <http://www.micrometals.com/>
- [6] Ho C.N.-m., Breuninger H., Pettersson S., Escobar G., Serpa L. A., Coccia A., Practical Design and Implementation Procedure of an Interleaved Boost Converter Using SiC Diodes for PV Applications, *IEEE Trans. on Power Electronics*, 27 (2012), n.6, 2835 – 2845
- [7] Pettersson S., Kicin S., Holm T., Bianda E., Canales F., Full Silicon Carbide Boost Chopper Module for High Frequency and High Temperature Operation, Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE-ASIA), (2014) International, 18- (21 May 2014), 3432 - 3439
- [8] Rąbowski J., Zdanowski M., Barlik R., Sterowniki bramkowe dla tranzystorów z węgla krzemu (SiC)-przebieg rozwiązań, *Przebieg Elektrotechniczny*, 88 (2012), nr.4b, 187192
- [9] Zakrzewski K.: The effects of flux density and frequency on power losses in magnetic laminations, Proc. of XXI Symp. EPNC'10, 17-18
- [10] Valchev, V.C., Van den Bossche A., Inductors and Transformers for Power Electronics, (2005)
- [11] Barlik R., Nowak M., *Energoelektronika, Oficyna Wydawnicza Politechniki Warszawskiej, Warszawa, (2014)*
- [12] Drofenik U., W. Kolar J.: A General Scheme for Calculating Switching- and Conduction- Losses of Power Semiconductors in Numerical Circuit Simulations of Power Electronic Systems, *Power Electronic Systems Laboratory (PES), Zurich, Switzerland, (2005)*
- [13] Feix G., Dieckerhoff S., Allmeling J., Schonberger J., Simple methods to calculate IGBT and diode conduction and switching losses, 13th European Conference on Power Electronics and Applications, Barcelona (2009). EPE '09, 1-8
- [14] Graovac D., Pürschel M., IGBT Power losses calculation using the datasheet parameters, *Infineon Application Note*, ver. 1.1, (2009)
- [15] Hsin-Ju Chen, Power losses of silicon carbide MOSFET in HVDC application., *University of Pittsburgh*, 2012, 29-34
- [16] Mößlacher Ch., Guillemand O., Improving Efficiency of Synchronous Rectification by Analysis of the MOSFET Power Loss Mechanism, *Infineon Application Note*, AN 2012-03 ver.2.1, (2012)
- [17] Graovac D., Pürschel M., Kiep A., MOSFET Power losses calculation using the datasheet parameters, *Infineon Application Note*, ver.1.1, (July 2006)
- [18] Application Considerations for SiC MOSFETs, *CPWR-AN08*, CREE Inc.
- [19] Eichhorn T., Estimate Inductor Losses Easily in Power Supply Designs, *Power Electronics Technology*, (2005), 14-24
- [20] Muhlethaler J., Biela J., Kolar J. W., Ecklebe A., Improved Core-Loss Calculation for Magnetic Components Employed in Power Electronic Systems, *IEEE Trans. on Power Electronics*, 27 (2012), n.2, 964-973
- [21] Steinmetz Ch. P., On the law of hysteresis, reprint, *Proc IEEE*, 72(2), 2 (1984), 196-221,
- [22] Bertotti, G., Fiorillo F., Pasquale, M., Measurement and prediction of dynamic loop shapes and power losses in soft magnetic materials, *IEEE Transactions on Magnetics*, 29 (1993), n.6, 3496 - 3498
- [23] Ruszczyk A., Sokalski K., Scaling in Modeling of Core Losses in Soft Magnetic Materials Exposed to Nonsinusoidal Flux Waveforms and DC Bias, arXiv:1309.0022v1
- [24] Ruszczyk A., Sokalski K., Unified model of temperature dependence of core losses in soft magnetic materials exposed to non-sinusoidal flux waveforms and DC bias condition, *COMPEL: The International Journal for Computation and Mathematics in Electrical and Electronic Engineering*, 34 (2015) n.1, 371 – 379