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Unique Micro System Stimulator with High Data Rate and Efficient Power Recovery Circuit

Abstract. This paper present an efficient micro-system stimulator to transfer data and power in biomedical implanted device by using Amplitude shift keying (ASK) modulation technique. The proposed system operates with low frequency 6.78MHz accordance to the industrial-scientific-medical (ISM) bands to avoid the biological tissue damage. The system design include new ASK modulator, class-E power amplifier, half wave rectifier, voltage regulator (LDO) and new ASK demodulator structure without passive elements to transfer 500Kb/s of data with modulation index 12.5%. The efficient inductive coupling link with 74.47% of efficiency is driven by class-E power amplifier with high efficiency up to 94.5%. Adequate and stable 1.8V DC are generated by the modified rectifier and voltage regulator to power the implanted electronics which occupies small area and does not have a thermal protection circuit or passive elements. The proposed ASK demodulator structure is developed to collect a synchronised demodulated signal that has minimum error without using delay-locked loops (DLL) circuits and clock recovery circuit. This system designed by using OrCAD Pspice 16.6 software, which employed 0.35 µm CMOS technology as a basis.

Streszczenie. W artykule opisano mikrosystem używany w stymulatorach biomedycznych przeznaczony dpo transferu danych i zasilania. System wykorzystuje kodowanie ASK z częstiotliwością 6.78 MHz. System składa się z modulatora ASK, wzmacniacza mocy klasy E, prostownika, regulatora napięcia LDO I dempodulatora ASK. Mikrosystem sty,mulatora biomedycznego o dużej szybkości przesyłu danych i skutecznym układzie zasilania.

Introduction

The implanted micro-system stimulator falls under the bio-implantable device classification. It is employed towards stimulating the nerves and muscles when disorders happen because a neural action potential is absent or when there is damage in the neural signal conduction pathway. The inductive coupling link is an appropriate method of wireless power transmission for powering the implanted micro-systems [1]. The ASK modulation technique has low cost, low-power consumption and a simple architecture. For these reasons its widespread using in near field telemetry system [2]. The implanted micro-system stimulator consist of two parts: the external one is fixed outside the body and inductively transfers data and power to the internal one, which is sited inside the body [3]. Most of biomedical implanted device powered inductively Due to the large size, chemical side effect and limited lifetime of battery [4]. For biomedical implants, the selecting carrier frequencies is playing a role important, which should to be lower than 20 MHz [1] depend on industrial scientific medical (ISM) bands to avoid over heated tissue and damage. The ASK demodulator was presented powered by 1.8 DC V towards achieving 1Mb/s data rate [5]. It was necessary for the structure to have clock recovery digital circuits for the synchronisation of the output data and the large size is still an issue. An ASK demodulator powered with 2.5-2.8 DC V was designed for the reduction of the power consumption in medical implanted devices [6]. However, no passive elements were used and the structure is made up of a rectifier, a digital shaper, an envelope detector, and a load driver for the transfer of 1MHz of data with 13.56 MHz. This structure has sensitivity to the modulation index and carrier frequency. Towards avoiding this drawback, a new circuit was designed based on comparator in an ASK demodulator. The new comparator was operated with 10 MHz and powered with 3.3 DC V towards transferring 1Mb/s of data, which includes a full wave rectifier, a signal formatter circuit, and a small capacitor and a voltage reference for filtering the high-frequency components. The demodulated signal output requires clock recovery circuits to enable correct data reading [7]. Also proposed was a low-power, non-coherent ASK demodulator that is1.8 DC V-powered and operated at 2 MHz frequency [8]. Based on clock recovery and comparator circuits, this structure is designed towards achieving a 1 Mb/s of data rate. Its large size, however, is the major problem. Based on the above-stated review, the researchers utilised a clock recovery circuit (e.g. latch flip-flop or decoder circuits) towards extracting the demodulated ASK signal. They additionally employed full wave rectifier and buffers, which occupied a large area and resulted in an increase in power consumption. Lastly, the implanted micro system's structural design operated at 13.56 MHz and with 1.8DC of voltage. This was used for powering a non-coherent ASK demodulator, which has self-data synchronisation and no clock recovery circuit to enable a (1-1.25) Mb/s transfer [9]. This structure utilised two comparators and one buffer for the extraction of the data that led to an increase in power consumption and towards an enlargement in size.

This paper constitutes an attempt to develop a fully integrated high data rate and low power for the implantable micro-system device with new structure of self-recovery ASK demodulator to collect data-information. The developed micro-system operates with ISM band 6.78 MHz with a low modulation index about 12.5%. The design aims at increasing the transmitted data rate up to 500 Kb/s, decrease power consumption with power efficiency 74.47%, minimize size and achieve feasibility.

System Design and Methodology

In general, the wireless power transfer system has two parts, external part touch the skin from outside and internal part implanted under the skin. The external part for proposed system contain from ASK modulator to modulate the data, class-E power amplifier to drive the external coil presented as transmitter. Implanted part consist of secondary coil presented as receiver, voltage rectifier to rectify the signal from AC to DC, low drop out (LDO) voltage regulator to get 1.8VDC to turn on the ASK demodulator to collect data with minimum error as shown in Figure (1). To enhance the efficiency for power transmission, the external and implant coils are tuned by series and shunt capacitors, respectively [10]. The implanted part divided into two paths, data recovery path and power recovery path which shown the details in Figure (2).
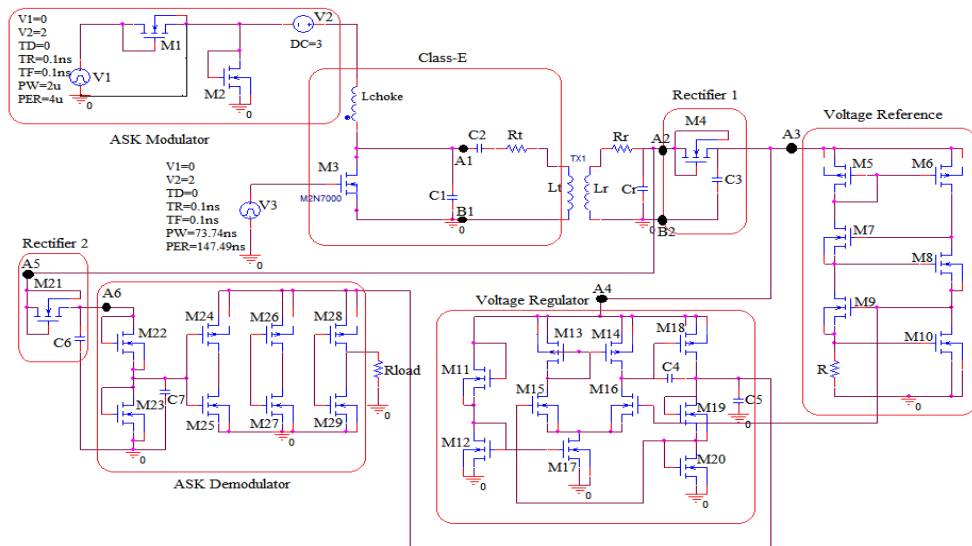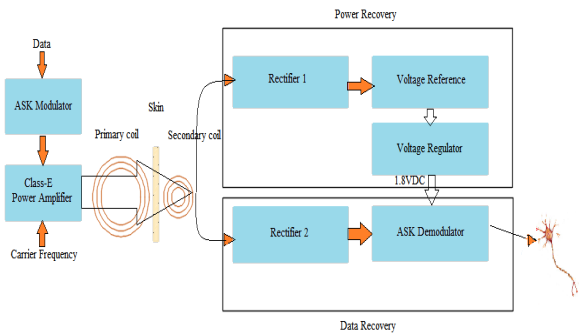
Fig.1. Proposed system architecture

Fig.2. The block diagram for micro-system stimulator

ASK Modulator Structure

The proposed block diagram of the developed ASK modulator is demonstrated in Figure (3). The data generator produces a Pseudo-random Noise (PN) or a fixed binary sequence. The modulation index is determined by two MOSFET (M1,M2) act as the voltage divider resistance form and voltage source V_2, which estimates the high and low voltage levels V_H and V_L respectively for powering the class-E power amplifier.
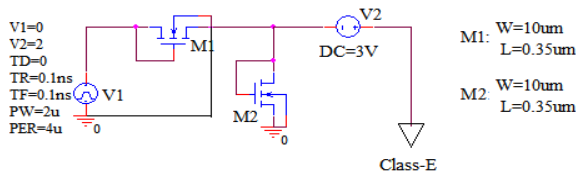

Fig.3. Architecture of proposed ASK modulator

The operation principle of the proposed ASK modulator is as follows: The voltage sources V_1 is used to generate fixed binary states 0 or 1 of the data with T_{bit} =2 μs. The voltage divider which present as MOSFET resistors (M1 and M2) control the ASK signal by adjusting the resistors and the voltage source V_2 that varies the relation between the high and low amplitude levels, V_H and V_L as given in (1).

$$(1) \qquad Modulation\,index = \frac{V_H - V_L}{V_H + V_L}$$

Class-E Power Amplifier Model at 6.78 MHz

Class-E power amplifier operated by frequency 6.78MHz ISM band is more suitable to be used for the biomedical applications and bio-telemetry systems in the near field region due to its high efficiency and simplest [11-13]. The proposed class-E as show in figure (4) is simple and achieves high efficiency reach to 94,5%. It's consist of inductor choke (L_{choke}) to provide fixed current and reduce the ripple from the power supply V_{DD}, one pole MOSFET switch is selected type (3TEN - 2N7000) to minimize switching losses in transistor [11], and one shunt capacitor (C_1) to ensure zero-voltage switching and remove harmonics of the non-ideal MOSFET switch.
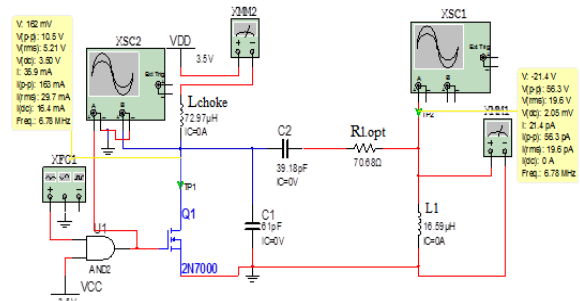

Fig.4. Class-E power amplifier structure

To tuned a certain frequency 6,78 MHz, these parts connected with series load network (C_2, R_{load} and L_1) which behaves as a transmitting antenna and convert the digital input signal into a stable sinusoidal output and satisfy constant current from the supply source. The inductor L_1 acts as a physical coil to transmit power and data to the implantable device. To find the values of the optimum load resistance and others passive elements, the delivered power to the implanted device should be known. The mathematical model is presented and as follow: Because of the proposed design is for bio-implantable devices, and to avoid the tissue damage due to the transmitted power is limited. where the power should be as small as possible and measured in mW [14, 15]. Therefore, the delivered power to the implanted devices (Pout) is assumed 100 mW (20dBm), operated frequency is 6,78 MHz and V_{DD} is 3,5V and the switch with 50% of duty cycle. To find the optimum power delivered by class-E power amplifier, the optimum resistances $R_{l.opt}$ for the amplifier should be introduce as a known value and can be calculate as given in (2) [16].

$$(2) \qquad R_{l.opt} = \frac{2}{1+\frac{\pi^2}{4}} \cdot \frac{V_{DD}^2}{P_{out}}$$

The inductor choke (L_{choke}) calculated as given in (3) [17].

$$(3) \qquad L_{choke} = 2\left(\frac{\pi^2}{4}+1\right)\frac{R_{l.opt}}{f} = \frac{7R_{l.opt}}{f}$$

The shunt capacitor (C_1) and the series capacitor (C_2) calculated by equation (4) and (5), respectively.

$$(4) \quad C_1 = \frac{1}{\omega_0 R_{l.opt}\left[\frac{\pi^2}{4}+1\right]\left[\frac{\pi^2}{2}\right]} = \frac{1}{\omega_0\left(5.447 R_{l.opt}\right)}$$

$$(5) \qquad C_2 \equiv C_1\left[\frac{5.447}{Q}\right]\left[1+\frac{1.42}{Q-2.08}\right]$$

For maximum class-E efficiency and constant sinusoidal wave, the quality factor (Q) should be consistent with the bandwidth and having value more than 5 [18]. The quality factor for the proposed Class-E amplifier is (9.99) as given in (6) and (7), respectively.

$$(6) \qquad \omega = 2\pi f$$

$$(7) \qquad Q \le \frac{\omega L_1}{R_{l.opt}},$$

The transmitted coil L_1 calculated as given in (8)

$$(8) \qquad L_1 = \frac{Q R_{l.opt}}{\omega_0}$$

Inductive Coupling Link Design

The inductive coupling link was designed to transfer the power and data from the external part to the implant part. Generally, the inductive coupling link is containing from secondary and primary coils. The primary side is tuned in series resonance to provide a low impedance load for driving the transmitter coil, whereas the secondary side is almost invariably parallel, and uses LC circuit for better driving of a nonlinear rectifier load [19]. The optimum resistance $R_{L.opt}$ which is calculated in equation (2) still large and it is not suitable to be used for subcutaneous applications which need very low impedance called parasitic resistance R_t [20]. This parasitic resistance having low impedance depending of the coils dimensions such as total length, thickness, permeability constant and relative permeability of the conductor and depth of skin [21, 22]. Figure (5) shows the passives component for the proposed series to parallel (SP) inductive link design. The values for the inductive coupling link are demonstrated in table 1.
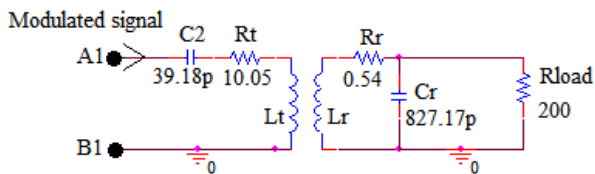

Fig.5. Design of inductive coupling link

Table 1. The values of the proposed system

Description	Symbol	Value
Primary inductance	Lt	16,59 µH
Secondary inductance	Lr	0,654 µH
Optimum resistance load	Rlopt	70.68 Ω
Primary resistance	Rt	10.05 Ω
Secondary resistance	Rr	0,54 Ω
Primary capacitance	C2	39,18 PF
Secondary capacitance	Cr	827,17 PF
Quality factor (Class-E)	Q	9,99
Quality factor (transmitter)	Qt	70.28
Quality factor (receiver)	Qr	51.56
Resonant frequency	f_0	6,78 MHz
Coupling coefficient	K	0,105
Class-E efficiency	ηamplifier	94,5%
Transmitted coil efficiency	ηt	84.76%
Received coil efficiency	ηr	87.77%
Total coupling efficiency	ηtotal	68,77-74.47%
Efficiency at 200Ω	η	74.47%
Modulation index	-	12,5%
Modulation rate	-	7,37%

The coefficient of coupling (K) must be 0 < K < 1 [23] and calculated as given in (9).

$$(9) \qquad K = \frac{M}{\sqrt{L_t L_r}}$$

The primary capacitance (C_2) is calculated in equation (5), and the secondary capacitance (C_r) is calculated by equation (10).

$$(10) \qquad C_r = \frac{R_{load} + \sqrt{R_{load}^2 - 4\omega_0^2 L_r^2}}{2\omega_0^2 R_{load} L_r},$$

Where R_{load} is presenting the implanted resistance and should be $R_{load} > 2\omega L_r$ [14], hence $R_{load} \ge 55.69$. Therefore, the values of Rload assumed from 100Ω to 400Ω. Where 100Ω is the worst case and 400Ω is an optimum case.

The quality factor for the transmit and received coil Q_t and Q_r are based on resonance frequency, coil inductance and parasitic resistance and calculated as given in (11) and (12), respectively.

$$(11) \qquad Q_t = \frac{\omega_0 L_t}{R_t}$$

$$(12) \qquad Q_r = \frac{\omega_0 L_r}{R_r}$$

Where the R_t, R_r presents the transmit and received coils parasitic resistance, respectively. Consider by using reflected impedance concept analysis [19]. The efficiency for the transmitter and receiver coils given in equations (13) and (14), the total coupling efficiency for the link calculated as given in (15).

$$(13) \qquad \eta_T = \frac{k^2 L_T R_{load}}{k^2 L_T R_{load} + L_R R_T}$$

$$(14) \qquad \eta_R = \frac{\omega_0^2 L_R^2}{\omega_0^2 L_R^2 + R_R R_{load}}$$

$$(15) \qquad \eta_{Total} = \eta_T \times \eta_R = \frac{k^2 \omega_0^2 L_T L_R^2 R_{load}}{k^2 \omega_0^2 L_T L_R^2 R_{load} + k^2 L_T R_R R_{load}^2 + \omega_0^2 L_R^3 R_T + L_R R_T R_R R_{load}}$$

Voltage Rectifier Design

The rectifier is a voltage conversion component, which converts AC to DC voltage in the implantable devices. The efficiency improvement of the rectifier is the most challenging part, especially in low power [24]. To improve the RF-DC MOSFET rectifies efficiency, the switching loss transistor (channel size) must be considered [9]. In the proposed embedded system, a half wave rectifier utilizing low-drop voltage with low-leakage CMOS diodes is developed by utilizing one NMOST and one capacitor. the relationship between voltage drops and also the transistor channel size can be rearranged to solve for (W/L) from equation (16) [25].

$$(16) \qquad V_{drop} = |V_{th}| + \sqrt{K\left(\frac{W}{L}\right)}$$

Where (K) is the trans-conductance parameter equal to (C_{ox} x μ_0). C_{ox} represents the gate-oxide capacitance per unit area. μ_0 is the low field mobility.

To prevent disturb the envelope data, the rectifier using in two positions, the first one is to rectify ASK signal in power recovery part as shown in figure (6-a) and the second one is to envelope signal in data recovery part with small capacitor as shown in Figure (6-b).
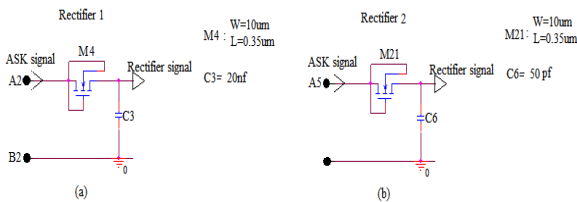

Fig.6. Half Wave Rectifier Structures

Proposed Voltage Reference for LDO regulator

An efficient voltage regulator in bio- implanted device requires voltage reference to generate a steady regulated voltage. The human bodies temperature has a limited variation and the implanted device with surrounding tissue has constant temperature due to the flowing blood in self-surrounding tissue lead to dispense from using a band gap circuit [9]. The multiple independent voltage reference circuit is a good choice in bio-implantable device [26, 27]. The development on the circuit is produced to provide multiple independent voltage reference. The value of reference voltage (2) is 900mV, which is the half value that's need in the output of voltage regulator. This value obtains by adjusting the size of the MOSFET M9 and M10 and the value of the resistor R as shown in Figure (7).
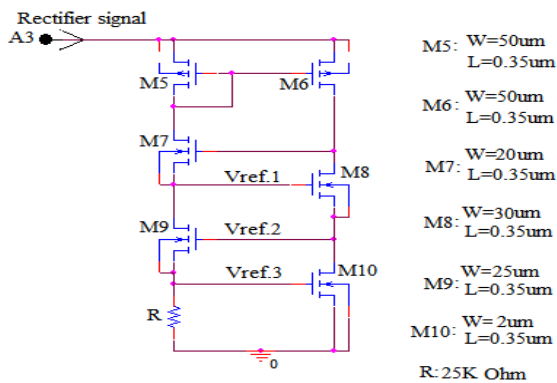

Fig. 7. Multiple supply independent voltage reference

Proposed Voltage Regulator (Low Drop-output Regulator (LDO))

The low drop out (LDO) regulator is considered a crucial block in implantable devices. They generally contain an errors amplifier with a negative feedback wherever their stability against numerous load conditions is of top notch concern. The propose LDO voltage regulator which is modified from [28] by replacing the passive element with NMOS transistor as a resistor, lead to decrease the size and to generate 1.8 DC output voltage.

An LDO voltage regulator consists of an error amplifier as one-stage high gain differential amplifier consists of (M11 to M17) transistors, pass power transistor PMOS (M18), a resistive voltage divider (M19 to M20) and small feedback capacitor (C4) 3 pf connected between the series-pass transistor gate and the drain to ensure and increase the system stability. The goal is towards designing an LDO limited by the following constraints:
• The output voltage is to be set at 1.8 V utilising an unregulated supply voltage of 5.7 V. Figure (8) presents the proposed regulator's general structure.
• The pass transistor must have a very large width. This is to enable the transistor to source currents that have large loads with a reasonable gate-source voltage.
• The length is kept at the minimum value towards keeping the threshold voltage low.
• Instead of using voltage divider resistors, (NMOS) transistors are employed at regulator output. This is towards feeding a fraction of the output voltage back towards the input; in doing so, the feedback path's power consumption is minimized since very little current passes through them.
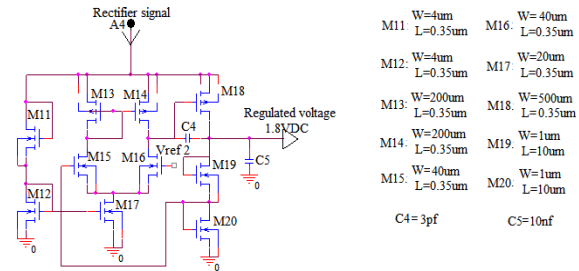

Fig.8. The basic LDO voltage regulator structure

ASK Demodulator Design

One of the simplest digital modulations techniques is the amplitude shift keying (ASK) or On/Off keying (OOK); these are commonly employed in wireless communication and biomedical device applications. In accordance with the references [2, 5-7, 29, 30]. The proposed ASK demodulator design is devised, which will be used in the developed implanted micro-system stimulator. The normal ASK demodulators contain from two important building blocks; envelope detector and comparator [9, 31, 32]. These architectures suffer from large process, temperature and voltage variation especially when comparator replaced by Schmitt trigger circuit and occupied a large area. The proposed ASK demodulator structure is powered with V_{DD} = 1.8 DC voltage and operated with ISM low-band frequency 6.78 MHz to extract 500Kb/s without using clock recovery circuits as shown in Figure (9).

The proposed ASK demodulator is designed based on two main parts: envelope detector and cascaded inverters. The first step is the envelope detector which receives the ASK signal at the rectifier output to step down by voltage divider resistance into maximized amplitude level that can be recognized by only digital inverter. Small capacitor set between the voltage divider and the inverter to suppress the

unwanted signal. The second part is using cascaded inverter following the envelope signal to increase the signal driving capability and to be standard logic levels. The ASK demodulator designed without using any comparator or a clock recovery circuit such as latch flip flop or decoder circuits, That's Lead to less power consumptions and smaller size.
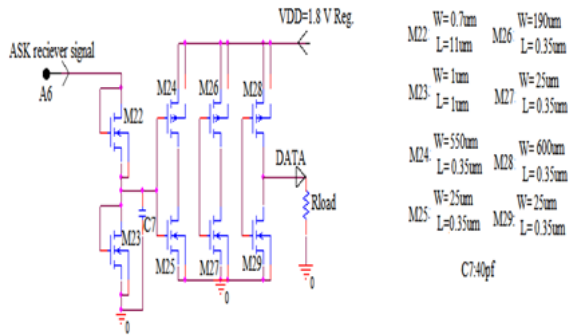

Fig.9. The proposed structure of ASK demodulator

Results and Discussions

This paper introduces a simple and efficient transcutaneous system which used to power and transmits data to the subcutaneous system. The proposed transcutaneous system involves two parts, external and internal part. The external part consists of pulse data generator, new ASK modulator and class-E, power amplifier operated at 6,78 MHz and transmitted coil to transmit the power and data to the implantable devices. Whereas, the internal part consist of received (implanted) coil, rectifier to convert AC to DC voltage, LDO voltage regulator to produce stable DC voltage, and ASK demodulator as shown in Figure (1). The data generator generates fixed binary sequence which controlled adjusting the resistors and the voltage source V_2. In this paper a new ASK modulator without passive elements as shown in Figure (2) is developed to modulate the input data and powered the Class-E power amplifier with 3- 4 V (DC) as shown in Figure (10).
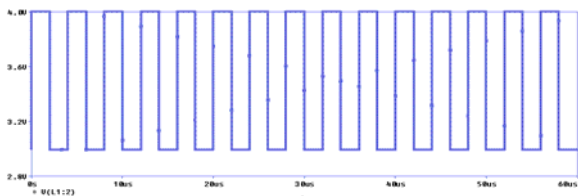

Fig. 10. The ASK generated power output to supply the Class-E power amplifier
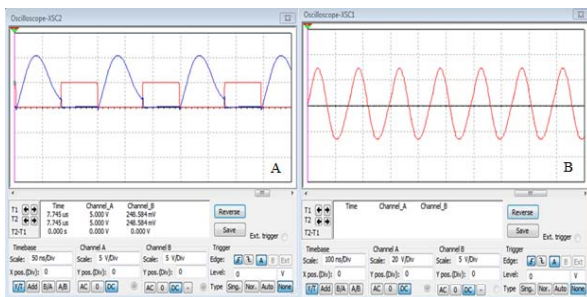

Fig.11. (A)The Class-E switching activity, (B) The stable class-E amplifier output sinusoidal waveform

The class-E switch (M3) operation is as follows: the Drain to Source voltage is equal (0) when the switch is active state (1) and Gate to Source voltage is (1) when the

switch in the state (0), and produce a stable sinusoidal wave signal to the transmitted coil as shown in Figure (11-a) and (11-b), respectively.

The Class-E efficiency is performed from the simulation where V_{rms} =19,6 V, I_{dc}=16,4 mA.

$$(17) \qquad P_{outavg} = \frac{V_{rms}^2}{R_{Lopt}}$$

The class-E efficiency can be calculated as given in (18).

$$(18) \qquad \eta_{class-E} = \frac{P_{outavg}}{P_{in} + P_{dc}}$$

The input power (Pin) is very small compare with dc power (P_{dc}) [11], so will be neglect. Therefore, the efficiency for class-E with optimum resistance is 94,5%. To design efficient inductive coupling link, several factors should be taken into account, these factors include: link efficiency, link voltage gain, communication bandwidth and coils size. Because of the proposed design is based on coupling not geometry, therefore, the "voltage in-voltage out" link is an approach which can control the output gain. The power efficiency link for inductive coupling is up to 74.47% according to equation (15). The coupling factor (K) is 0.105 as shown in Figure (12).Referring to the Figure (5), the transmitted coil L_1 presents the external coil for the inductive link and act as an antenna to transmit the modulated ASK signal with V_H=27 V and V_L=21 V with modulation index 12,5% as shown in Figure (13-a), and table (1) shows the values of the proposed system. The received coil L2 in the internal part presents the implanted coil and receive the ASK signal inductively with V_H=6 and V_L=4,65 V with modulation index 12,5% as shown in Figure (13-b). Both transmit and receive coils have the same modulation index and this contribute to reduce the system power consumption.
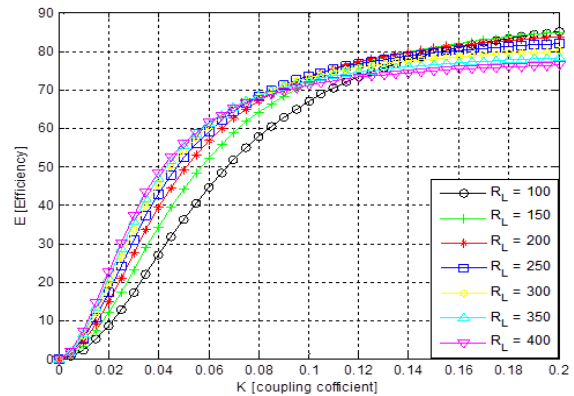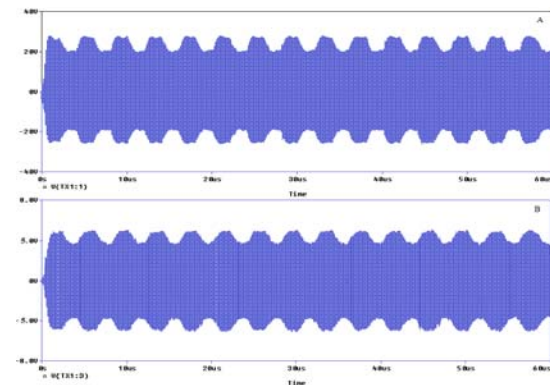

Fig.12. Power efficiency links

Fig.13. (A) The transmitted ASK signal with modulation index 12.5%, (B) The received ASK signal with modulation index 12.5%

To get better link efficiency, both primary and secondary RLC circuits for the inductive link tuned at the same resonance frequency with bandwidth approximately 500 KHz, which it is chosen operated frequency 6,78 MHz as shown in Figure (14).
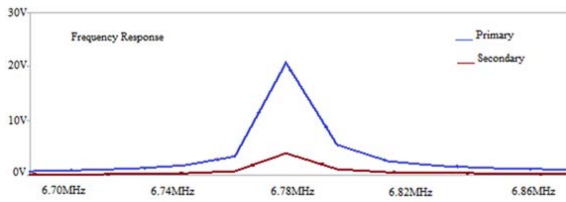

Fig.14. The external and internal coils at same resonance frequency 6.78MHz

The processing for extracting data and power divided in two parts, the first one is power recovery path and the second one is data recovery path. For the power recovery path, it is consist of voltage rectifier, voltage reference and voltage regulator. The proposed rectifier provide a rectified ASK signal smoothed by stabilizer capacitor 20 nf to get a non-regulate DC signal as shown in Figure (15-a). The non-regulated DC voltage must be constant. Therefore, The voltage reference for power recovery is designed to generate a level voltage VREF is (900mV), which it is half of the needed value on the output voltage regulator with a very stable DC voltage as shown in Figure (15-b). the proposed voltage regulator generate very stable and smooth 1.8 V as shown in Figures (15-c).
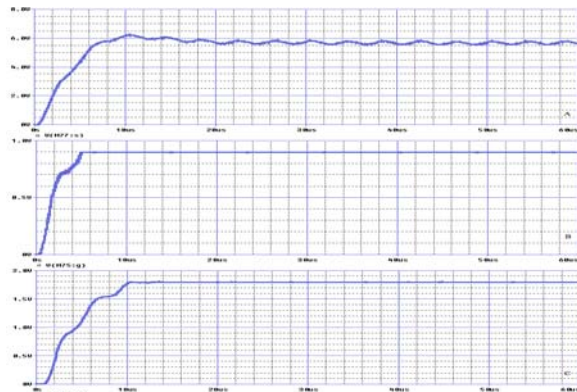

Fig.15. (A) The smoothed rectified ASK signal, (B) Reference voltage output signal, (c) The regulated VDD voltage output signal
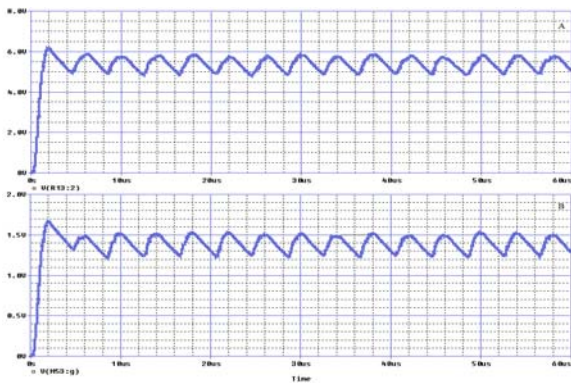

Fig.16. (A) rectifier signal for data path recovery, (B) step down voltage divider signal

For data recovery path which consist of rectifier, voltage divider, one small capacitor, and cascade inverter. The output signal from rectifier has V_{max} (5.7V) and V_{min}(4.8V) as shown in Figure (16-a). These values are still high to be compared with the V_{DD} regulated voltage, and the V_{MAX} should be maximize amplitude level that can be recognized by only digital inverter which turn on with $V_{DD}=1.8$ V. Thus, in order to achieve that, the voltage divider is used to stepped down the ASK rectified signal to the desired value as shown in Figure (16-b).

The ASK demodulator has envelope detector and two cascade inverters to extract the data. To envelope data signal, a small capacitor used to suppress the high of the modulated ASK signal and remove the unwanted harmonic signal as shown in Figure (17-a) with one sensitive digital inverter. The output of the envelope signal shown in Figure (17-b).
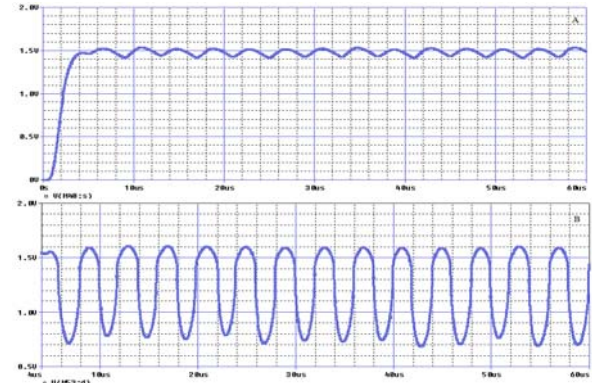

Fig.17. (A) Output signal after small capacitor, (B) Output envelope signal

The final part in ASK demodulator is a buffer composed of cascaded inverter to increase the signal driving capability and used to collect the synchronize data with value (1.7V) without using any comparator or a clock recovery circuit, That's Lead to less power consumptions and smaller size. Figure (18) shows the output demodulator data signal.
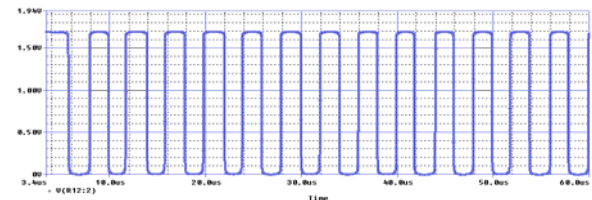

Fig.18. The output demodulated signal

The demodulated signal with data rate 500Kb/s synchronized with the input ASK modulated signal was achieved with high performance and without using any clock recovery circuits as demonstrated in Figure (19).
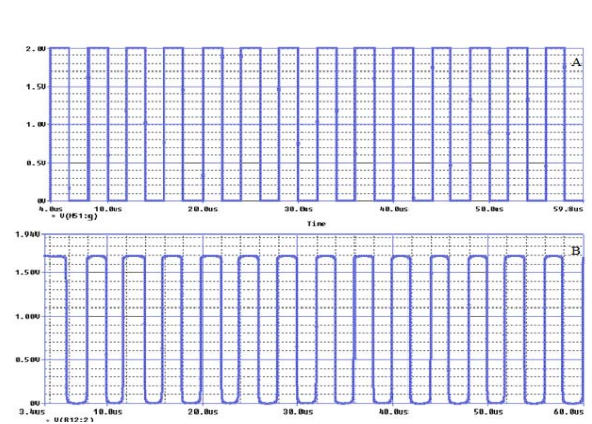

Fig.19. the synchronize input (a)and output(b) data

To validate the propose system, the comparison of the system with other prior works is summarized in Table (2). The results point to the better performance of the developed system: the implanted circuits are powered by low power supply at 1.8 DC V; higher data rate transmission; lower power consumption; and lowest figures of merit (FOM), as indicated in Equation (19).

$$(19) \quad FOM = \frac{DataRate}{CarrierFrequency \times Modulationindex}$$

Table 2. The system performance compare with other works

CMOS(μm)	Mod. Index (%)	Mod. Rate (%)	Car. Freq. (MHz)	Data Rate (kb/s)	Power Sup. (V)	Power Cons. (mw)	FOM	References
1.2	N/A	N/A	6.78	200	N/A	N/A	N/A	[33]
1.2	7.14	5	1-10	50-500	N/A	N/A	N/A	[34]
0.5	10	2	10	200	3.3	N/A	2	[35]
0.35	10.34-17.24	1	2	20	3.3	10.23	0.58-0.967	[28]
0.35	18.25	7.37	13.56	1000	3.3	N/A	N/A	[14]
0.35	N/A	N/A	10	2000	3.3	0.84	N/A	[36]
0.35	10	28.5	2	570	3.3	N/A	N/A	[37]
0.18	5.25	50	2	1000	1.8	0.336	95.05	[5]
0.35	20	N/A	10	1000	3.3	N/A	N/A	[7]
0.18	2.86-38.64	50	2	1000	1.8	0.396	1.29-1.748	[8]
0.35	13	7.3-11	13.56	1000-1250	1.8	0.25	0.985-1.277	[15]
0.35	12.5	7.37	6.78	500	1.8	0.19	0.589	Proposed

Conclusion

This paper produced a modified design for biomedical implanted micro-system device utilised towards stimulating muscles and nerves. the operated carrier frequency is used at 6.78MHz ISM band, the propose system has a 12.5% modulation index and a 7.37% modulation rate for achieving a 500Kb/s data rate, which depends on the generated binary data $T_{bit}=2$ μs. The modified half wave rectifier was employed. The voltage regulator underwent improvement towards producing a stable 1.8 DC voltage. This was for powering up a new ASK demodulator structure, which is depend on simple envelope circuit, and cascade inverter. Therefore, the proposed ASK demodulator did not necessitate the use of any circuit for synchronising data. Dissimilar to others, some of the designs employed decoders, or flip–flops, towards getting rid of the shifting problem. The design accomplished the following four objectives: small size, low power consumptions, feasibility and high data rate. So cannot cause tissue damage. The proposed design is very suitable to use in wireless biomedical implants and also other portable wireless communication systems. The system Compared with 11 previous works, the results of this study's showed better performance.

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