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The design approach to the single-phase Z-Source inverter

Abstract. *The impedance networks increment the input DC voltage of the voltage source inverters. Their advantage is lack of the additional switches – they use only inverter bridge switches. However they cause some side effects in the inverter operation. Up today the tips how to design Z-Source impedance network keeping it in the Current Continuous Mode are rare in the literature. The paper present problem of additional distortions of the Z-Source inverter output voltage caused by "shoot through" states. The influence of the impedance network on the dynamic properties of the inverter can be the other problem. The properties of the magnetic materials in the used coils cores affect on the Z-Source inverter properties. The paper will show the approach to the design of the single-phase Z-Source inverter, the measurements of its control function Bode plots. The ZSI small signal model (required for the microprocessor based control) calculated using measurements will be presented.*

Streszczenie. *Sieci impedancyjne są stosowane do zwiększenia stałego napięcia wejściowego falowników. Ich zaletą jest brak dodatkowych przełączników – wykorzystują tylko przełączniki z mostka falownika. Jednak powodują one efekty uboczne w pracy falownika. Aktualnie trudno znaleźć w literaturze wskazówki jak projektować sieć impedancyjną typu Z-Source. Artykuł przedstawia problem powstawania dodatkowych zniekształceń napięcia wyjściowego falownika powodowanych stanami „shoot through". Innym problemem może być wpływ sieci impedancyjnych na własności dynamiczne falownika. Własności materiałów magnetycznych rdzeni dławików wpływają na własności falownika z siecią Z-Source. Artykuł przedstawia podejście do projektowania jednofazowego falownika z siecią Z-Source, pomiary charakterystyk częstotliwościowych jego funkcji sterowania. Zostanie zaprezentowany małosygnałowy model układu ZSI (niezbędny do sterowania mikroprocesorowego), obliczony na podstawie pomiarów. (**Projektowanie jednofazowych falowników z siecią impedancyjną typu Z-Source**).*

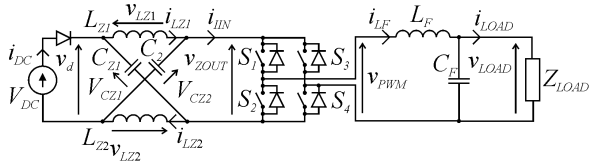
Keywords: impedance network, Z-Source, Bode plots, voltage source inverter, small signal model.
Słowa kluczowe: sieć impedancyjna, Z-Source, model małosygnałowy.

Introduction

The Z-Source impedance network [1, 2] is a kind of DC/DC converter that does not need any additional switches. The energy is stored in its inductances during "shoot through" time T_{st}=$d_Z T_c$ in zero states of the H-bridge voltage source inverter (VSI). The restricted modulation depth (M<1-d_Z) of PWM – the "shoot through" pulses should be placed between inverter pulses what decreases the maximum modulation depth, is the disadvantage of the Z-Source is. "Shoot through" pulses have influence on the inverter bridge output voltage. The integration of the Z-Source impedance network and the VSI is called Z-Source Inverter (ZSI). Z-Source in some degree changes dynamic properties of the inverter in the low frequency range [3, 4]. It is caused by the Z-Source high equivalent output impedance, because the values of coils inductances are multiplied by the square of the voltage increasing factor. The "shoot through" action during zero states of the inverter increases the voltage drop on the switches during discharging the energy from the filter inductor L_F. The "shoot through" current cause the characteristic for ZSI distortions of the inverter output voltage (it is "skewed") and implements the additional damping in the Bode plots of the control transfer function of the inverter. These problems were not discussed in the literature – even they can be seen for all the impedance networks structures (e.g., Fig. 3d in [4], Fig. 10b in [8]). The discontinuous input pulse current (Fig. 3a) is a disadvantage of the Z-Source. The impedance network architecture was modified to the voltage fed quasi ZSI (qZSI) [5, 6] with the continuous input current. The Switched Inductor ZSI (SLZSI) [7, 8] grants the higher increase of the DC voltage. There are other mixed structures of ZSI and SLZSI [9], modified qZSI [5], transformer coupled inductor-capacitor-capacitor-transformer networks: LCCT-ZSI and LCCT-qZSI [10, 11]. The impedance networks topology is presented widely in the review paper [12]. In chapter 2 the PWM scheme useful for ZSI driving will be described, in the chapter 3 the inverter output filter will be calculated, in chapter 4 the values of the Z-Source inductors and the capacitor will be estimated to keep Continuous Current Mode, in chapter 5 the problem of additional output voltage distortions will be focused, in chapter 6 the measured Bode plots of the Z-Source inverter will be presented focusing impedance network influence on them, and the discrete small-signal model based on the measured Bode plots will be described.

The PWM scheme useful for ZSI driving

a)



b)

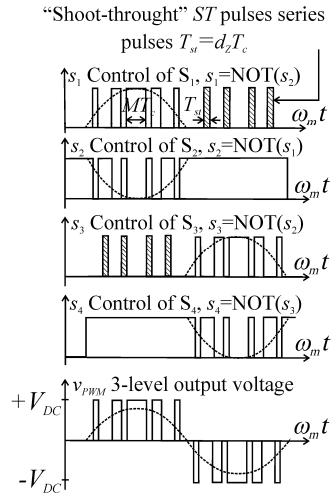


Fig. 1. a) The standard ZSI structure description, b) the modified "third PWM scheme" used in ZSI

The standard designed ZSI structure is presented in Fig. 1a. "Shoot through" states are possible only in zero states of the inverter (the falling down current of the L_F inductor flows through two switches S_2 and S_4). Three PWM schemes for the double-edge, 3-level PWM were presented in [13, 14, 15]. The modified (with the additional "shoot through" pulses) third PWM scheme (1) - realised by means of ARM7 LPC2148 microprocessor - is the best for the Z-

Source driving (Fig. 1b). *ST* is the series of shoot through pulses $d_Z T_c$. It is crucial that they should be centred with the end of the T_c periods (the PWM pulses are centred with the middle of T_c periods).

(1) $For\ k = 1...(f_c / f_m)$:

$$S_1 : T_{ON}(k) / T_c = M \sin(2\pi k f_m / f_c)\ for\ \omega_m t < \pi ,$$

$$S_1 = ST\ for\ \omega_m t \geq \pi ,$$

$$S_2 = NOT(S_1)\ for\ \omega_m t < \pi ,\ S_2 = ON\ for\ \omega_m t \geq \pi ,$$

$$S_3 = ST\ for\ \omega_m t < \pi ,$$

$$S_3 : T_{ON}(k) / T_c = -M \sin(2\pi k f_m / f_c)\ for\ \omega_m t \geq \pi ,$$

$$S_4 = ON\ for\ \omega_m t < \pi ,\ S_4 = NOT(S_3)\ for\ \omega_m t > \pi$$

The design of the output $L_F C_F$ filter of the voltage source inverter

The value of the product of $L_F C_F$ is calculated [14] from the limited value of the output voltage ripple amplitude (below 3% in accordance with IEEE Standard 519-1992). The inductance L_F is calculated looking for the minimum (2) of the cost function which is the sum of absolute values of reactive powers P_{RLF} and P_{RCF} in the filter components where C_F is presented as function of $L_F C_F$ product and L_F: $C_F=(L_F C_F)/L_F$.

$$(2) \qquad \partial(P_{RLF} + P_{RCF}(C_F = (L_F C_F)/L_F))/\partial L_F = 0$$

The L_F and C_F values [13, 14, 16] depend on the load ($V_{LOADrms}$, $I_{LOADrms}$ – the VSI output rms voltage and current) and the switching frequency f_c. The values of the filter components for the double edge, 3-level, single phase VSI are calculated (3).

$$(3) \qquad L_F \approx \frac{1}{f_c}\frac{V_{IOUTrms}}{I_{IOUTrms}},\ C_F \approx \frac{1}{f_c}\frac{1}{V_{IOUTrms}/I_{IOUTrms}}$$

The design of the Z-Source impedance network

When power efficiency coefficient is $\eta=P_{LOAD}/P_{DCIN}$, the DC voltage amplification coefficient k_{VZ} of the ZSI (4) was calculated in [4] on the base of [17]

$$(4) \qquad k_{VZ} = \frac{V_{IOUT\max}}{V_{DC}} = \eta\frac{M}{1-2d_Z}$$

The assigned coefficient d_Z ($d_{Zmin} \leq d_Z < 0.5$) cannot be lowered below d_{Zmin} because the Continuous Current Mode (CCM) of i_{LZ} inductors should be provided and M cannot increase over $1\text{-}d_Z$. The two average values of the inductor current (Fig. 2b) should be taken into account – the current averaged in the switching period T_c (i_{LZavTc}) and the current averaged in the fundamental period T_m (i_{LZavTm}).
In [5] the average value $I_{DCav}=I_{LZavTm}$ (Figs 2a, 2b).

$$P_{DCIN} = V_{DC} i_{DCav} = V_{DC} I_{LZavTm},$$

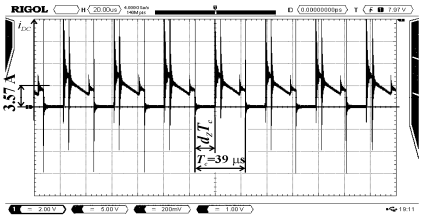
$$(5)\ P_{LOAD} = \eta P_{DCIN} = V_{LOADrms} I_{LOADrms}$$

$$I_{LZavTm} = \frac{1}{\eta}\frac{V_{LOADrms}}{V_{DC}} I_{IOUTrms} =$$

$$(6)\qquad \frac{1}{\eta}\frac{1}{\sqrt{2}}\frac{\eta M}{1-2d_Z} I_{LOADrms} = \frac{1}{\sqrt{2}}\frac{M}{1-2d_Z} I_{LOADrms}$$

$$(7) \qquad I_{LZavTm} = \eta\frac{1}{2}\left(\frac{M}{1-2d_Z}\right)^2 \frac{V_{DC}}{R_{LOAD}}$$

a)



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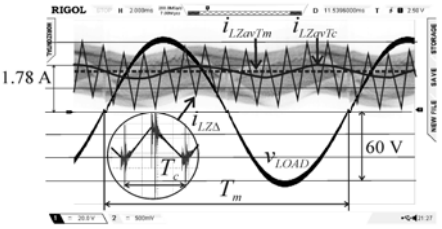

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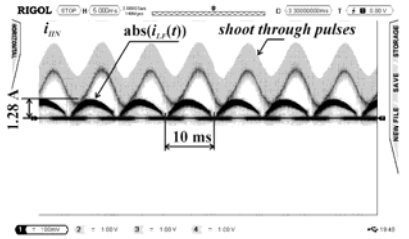


Fig. 2. a) The output DC source current i_{DC}, b) components of the Z-Source choke current i_{LZ}, c) H-bridge input current i_{IIN}

The inductor $i_{LZavTc}(t)$ current is approximately the sum of the constant I_{LZavTm} current and the sinusoidal $h_1(i_{LZavTc}(t))$ current that has twice the fundamental f_m frequency and it is approximately the first harmonic $h_1(\text{abs}(i_{LF}))$ of the "rectified" sinusoidal inverter input current $i_{IIN}(2\pi f_m t)$ (Fig. 2c) because of the inverter H-bridge action.

$$i_{LZavTc}(t) = I_{LZavTm} + h_1(abs(i_{LF}(t))) =$$

$$(8)\ \frac{1}{2}\frac{\eta M}{1-2d_Z}\frac{V_{DC}}{R_O}\left[\frac{M}{1-2d_Z} + \frac{8}{3\pi}\cos(4\pi f_m t)\right]$$

$$(9)\ I_{LZavTc\min} = \frac{1}{2}\frac{\eta M}{1-2d_Z}\frac{V_{DC}}{R_O}\left(\frac{M}{1-2d_Z} - 0.85\right)$$

To ensure the CCM of the i_{LZ}(t) current, the Δi_{LZ}(t) ripple component waveform symmetrical around $i_{LZavTc}(t)$ should fulfil (10).

$$(10) \qquad I_{LZavTc\min} - \frac{1}{2}\Delta I_{LZ} > 0$$

We can assume that the voltage ripple ΔV_{CZ} on the C_Z capacitor is small (e.g., 3%V_{CZav}) and $V_{CZmin} \approx V_{CZmax} \approx V_{CZav}$ can be approximated.

$$(11) \qquad \Delta I_{LZ}(t_{st}) = \frac{V_{CZav}}{L_Z} d_Z T_c = \frac{1-d_Z}{1-2d_Z}\frac{V_{DC}}{L_Z} d_Z T_c$$

From (10) and (11) the minimum value of L_Z (12) can be calculated.

$$(12) \qquad L_{Z\min} = \frac{(1-d_Z)(1-2d_Z)d_Z}{\eta M(M - 0.85(1-2d_Z))} T_c R_{LOADborder} \qquad \text{for}$$

$$M > 0.85(1-2d_Z)$$

The value of $R_{LOADborder}$ should be initially assigned for the sufficient border of the CCM. Always for higher value of the load resistance there will be Discontinuous Current Mode (DCM). The high value of L_Z increases the influence of the impedance network on the dynamic properties of the ZSI. That is why (13) was further used.

(13) $$L_Z = L_{Z\min}$$

To calculate the minimum value of C_Z we should know the admissible capacitor voltage change ΔV_{CZ} during shoot through time. At the begin of the "shoot through" time T_{st} the $i_{LZ}(t)$ coil current is the lowest inside single T_c.

(14)
$$\Delta V_{CZ\max}(t) = \frac{\max(I_{LZ\min})}{C_Z} T_{st} = [\max(i_{LZavTc}(t)) - \frac{1}{2}\Delta I_{LZ}]\frac{d_Z T_c}{C_Z}$$

(15) $$I_{LZavTc\max} = \frac{1}{2}\frac{\eta M}{1-d_Z}\frac{V_{CZav}}{R_{LOAD}}(\frac{M}{1-2d_Z} + 0.85)$$

(16) $$\Delta I_{LZ}(t_{st}) = \frac{V_{CZav}}{L_Z} d_Z T_c$$

We can calculate the minimum value of the capacitor C_Z for the assigned value $\Delta V_{CZmax}/V_{CZav}$.

(17) $$C_{Z\min} = \frac{1.7}{2}\frac{\eta M d_Z}{(1-d_Z)}\frac{T_c}{R_{LOAD\min}}\frac{1}{\Delta V_{CZ\max}/V_{CZav}}$$

In all the DC/DC converters, the calculated minimum value of output capacitance is oversized (18) with multiplying by e.g., 10.

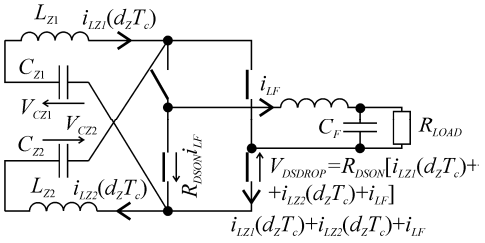
(18) $$C_Z = 10 C_{Z\min}$$

The calculated values (13) and (18) can be compared with the results of [18]. The example of the experimental inverter is: d_Z=0.4, M=0.5, T_c=1/25600 s, η=90%, $R_{LOADborder}$=94 Ω, $R_{LOADmin}$=47 Ω, $\Delta V_{CZmax}/V_{CZav}$=3%. The results are: C_Z=71 μF, C_Z=100 μF was used, L_Z=1.2 mH, the choke L_Z=1.1 mH was used with Super -MSS™ core [19]. This type of the alloy-powder material guarantees that coil inductance will be equal to the nominal in the wide magnetizing current amplitude and frequency range [20]. The output filter was L_F=2.2 mH (economic iron-powder Material 26 core), C_F=1 μF.

The additional distortions of the output ZSI voltage

The additional voltage drop (Figs 3a, 3b) on the switch $R_{DSON}(i_{LZ1}+i_{LZ2})$ during $T_{st}=d_Z T_c$ "shoot through" state causes that the condition of approximately the same current increase and decrease in the L_F coil in a single switching period T_c forces the additional increase of the output voltage. The R_{DSON} resistance of channel of the switched on power MOSFET can be equal to hundreds of mΩ. Finally this voltage drop causes the faster increase of the VSI output voltage and slower output voltage decrease during fundamental period (Fig. 3c).

a)



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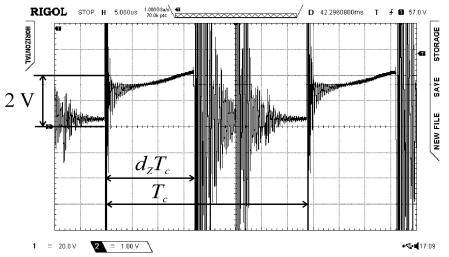

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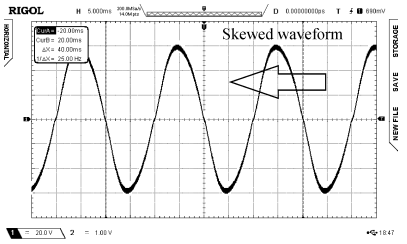
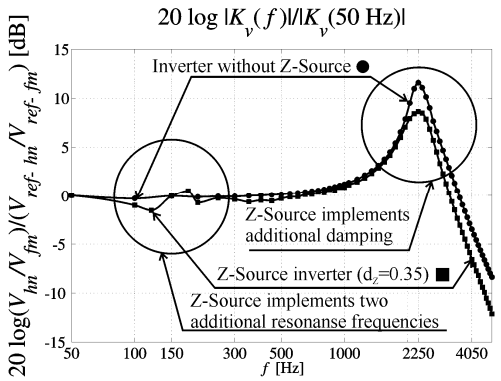


Fig. 3. a) Current flow in ZSI during "shoot through" time in one half of the fundamental period, b) the voltage drop V_{DSDROP} on the low switch S_4 - IRFP 360 Power MOSFET in the inverter bridge for d_Z=0.45, V_{LOAD}=60 V, R_{LOAD}=47 Ω, c) the distortions of the ZSI output voltage caused by the additional voltage drops on the switches during "shoot through" states

The influence of the Z-Source on the small-signal model of the inverter

a)



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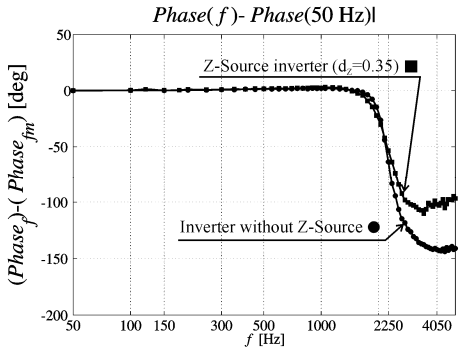

Fig. 4. The exemplary influence of the Z-Source on the control transfer function of the inverter (d_Z=0.35, L_Z=1.1 mH – Super-MSS, C_Z=100 μF, L_{Fnom}=2.2 mH – Mat. 26, C_F=1 μF), a) magnitude, b) phase

The Z-Source implements two additional resonant frequencies in low frequency range [3, 4] in the control transfer function and additional damping in the neighbourhood of the filter resonant frequency (Figs 4a,

4b). The properties of the soft magnetic materials of the coils cores in case of the popular iron-powder materials seriously increase the equivalent serial resistances and change inductances of the chokes [21, 22]. In case of high quality alloy-powder [19] or nanocrystalline [22] materials, the changes of the equivalent serial resitance and inductance are much lower [20]. The method of the inverter control transfer function Bode plots measurements was presented in details in [3, 4, 21].

$$K_{CTRL} = \frac{V_{IOUT}}{V_{CTRL}} = z^{-1} \frac{0.1488z^{-1} + 0.1384z^{-2}}{1 - 0.1519z^{-1} + 0.806z^{-2}} \quad (19)$$

After simple discretization (e.g. ZOH method for the T_c=39 μs sampling period, R_{LOAD}=2000 Ω) we get the discrete control transfer function (19) that can be directly used in the discrete SISO control law [20, 21]. The Bode plots are measured for the highest assumed resistance – 2000 Ω because the simple inverter SISO controllers treat the load current as the independant disturbation [13]. The measured equivalent values of the filter inductor L_F with the core made of Material 26 are L_{Fe}=4.6 mH, R_{LFe}=16.1 Ω in the operating point (Fig. 4a) while L_{Fnom}=2.2 mH, R_{LFDC}=0.22 Ω. The Z-Source increases equivalent serial resitance to R_{LFe}=23.3 Ω.

Conclusions

The paper presents the basic design hints for the Z-Source inverter (the calculation of the inductances and capacitances). The influence of the Z-Source impedance network on the increase of the output voltage distortions is shown. It was not focused in the literature till now. Finally the two types of influence of the impedance network on the control transfer function of the inverter are shown by means of measurements of the experimental inverter. The ZSI discrete control transfer function that is required for microprocessor based control is calculated from measurements. The paper is useful for the designers of the ZSI.

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