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Evolution of Low Drop Out Voltage Regulator in CMOS Technologies

*Abstract. The demand for low voltage devices has initiated the development of Low Drop Out (LDO) regulator in manifold. This paper presents a review of various LDO frameworks that have been implemented in CMOS technologies and the impact of frameworks related to the parameters of the LDO. The LDO architecture is evaluated through its Power Supply Rejection (PSR) and transient response performance. The transient response performance mostly depends on the added buffer and the PSR performance depends on the pass device capacitance and the LDO loop gain. *

Streszczenie. W artykule przedstawiono przegląd rozwiązań układów LDO (Low Drop Pout) w technologii CMOS. Przedstawiono także rozwiązania typu PSR – Power Supply Rejection. Analizowano dynamikę tych układów. Tendencje rozwojowe układów LDO (Low Drop Out) w technologii CMOS

Keywords: CMOS, Low Drop Out (LDO) Regulator, Power Supply Rejection (PSR), transient response.
Słowa kluczowe: układy LDO – Low Drop Out, technologia CMOS.

Introduction

Power supply is one of the most vital modules in any electronic devices such as smart phones, tablet PCs, camera, MP3 player, Personal Data Assistant (PDA), Radio Frequency Identification (RFID) etc. [1-3]. Due to the rapid increasing demand for portable devices the use of efficient power management systems to prolong battery life cycle and operating time for device is becoming the most important factor [4-9]. A linear regulator is a popular power supply which is an inductor-less, ripple-less and low-noise power converter with a bulk line frequency transformer [10]. In the 1970s, the linear regulators have been implemented in BJT technology and are referred as the "20 kHz revolution" [7, 10]. However, the power efficiency was not sufficient for low-power operations as the ground current was load-current dependent and the dropout voltage was large [11]. In the 1980s, the power MOSFET appeared as the dominant power device due to its high-switching frequency operation (above 100 kHz), easier driving requirement and higher reliability [10]. With the rapid development of CMOS technology, many variations of CMOS voltage regulators have appeared [12-13]. There are several types of voltage regulators such as LDO linear regulator, Switch-Inductor Regulator (switching regulator) and Switch-Capacitor Regulator (charge pump) [4].

CMOS linear regulators can be categorized as low supply current, large current, high voltage, high-speed and Low Drop Out (LDO). The device that uses a low drop-out voltage regulator can provide a stable output voltage with good noise performance and less power consumption compared to switching regulators to drive small sub-circuit [5-6]. LDOs can operate at a low supply voltage, which is suitable for single-cell and two-cell battery applications as the ground current LDO is load-current independent [11]. In practical applications, such as portable devices, the conventional power management system consists of Switching Power Converter (SWPC) to boost up the voltage cascaded with LDOs in series to suppress the inherent noise associated with switchers and control logic [5, 14-15]. By turning the regulator's outputs on and off or by varying the output voltage levels to optimize the power consumption of the device, the control logic can change the elements of each subsystem as active mode, standby mode and sleep mode [5].

This paper discusses the evolution of LDO voltage regulator based on CMOS technology and the various properties of existing regulator topologies with their advantages. First the architecture, principle and specification of LDO are discussed and then the description of circuit, transient response and power supply rejection characteristics of the LDO voltage regulator are portrayed. Finally the discussion of all the framework are presented.

Architecture and principle of LDO

The drop out voltage is the bare minimum differential voltage between the output and input voltage at such a point where the circuit stops to regulate. Also, low-dropout voltage indicates that the voltage across pass device is as low as 100mV to 1.5V [4]. For LDO regulator, the output voltage is always lower than input voltage by a minimum value of dropout voltage. The performance is enhanced as it has low output impedance. The LDO can be applied to high power, low power and ultra-low power applications.

LDO Linear Regulator Architecture

Basic LDO regulator topology usually consists of a pass device of PMOS, a decoupled capacitor C_L with a parasitic resistor R_{esr}, two feedback resistors R1 and R2, reference voltage and a critical error amplifier as shown in Figure 1. There are mainly three poles. p1 is from the output node, p2 is from the gate of the pass device and p3 is the internal pole within the error amplifier [16]. The basic schematic of generic LDO voltage regulators is based on a PMOS. The PMOS FET with common source connection works as the pass transistor between the input and output voltages. A part of the output voltage is fed back through R1 and R2 to the input and is compared to the voltage reference V_{REF}. Capacitor C_L stands for the capacitive load [17].
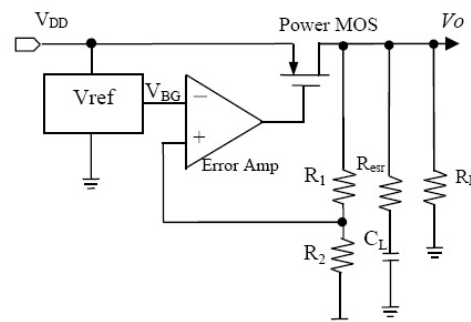

Fig. 1. Basic Low Dropout Regulator Topology [5]

The operating principle of LDO is based on the output of the regulator. It generates an error signal through the

feedback network to control the output current flow through the pass transistor. The output voltage is set to a constant voltage level by R1, R2 and reference voltage [5]. The divided voltage feedback through R1 and R2 and reference voltage difference, force the error amplifier to adjust the current flow through PMOS when changes happen at output voltage. The error amplifier compares the error signal with the reference voltage and amplifies the difference to control the pass device. A constant output voltage can be achieved by controlling the load current flow through the pass device. Output voltage is determined by Equation 1 [5]. The efficiency of LDO regulator can be expressed by Equation (2) and drop-out voltage can be expressed by Equation (3) [5].

(1) $\qquad V_0 = V_{ref} \times \left(1 + \frac{R_1}{R_2}\right)$

(2) $\qquad \mu = \frac{V_{out}}{V_{in}}$

(3) $\qquad V_{drop-out} = (1 - \mu)V_{in}$

Error amplifier creates an error signal whenever there is a variation between the reference voltage and feedback voltage. The error signal controls the gate of power transistor for maintaining constant voltage with a supply of variable current to the load circuit as shown in Figure 2. This topology has the advantages of improved power supply rejection ratio (PSRR) and presents a dominant pole that is determined only by the load capacitance. The power consumption of the error amplifier is kept at minimum to avoid degrading the efficiency of the low voltage regulator (LVR). It uses a centroid configuration to minimize any offset voltage [18].
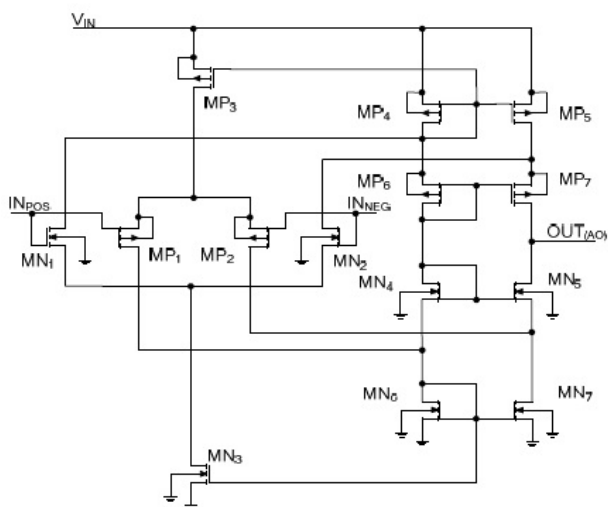

Fig. 2 . Error amplifier circuit [18]

To boost the output current capabilities of the error amplifier required by the load to the higher levels for maintaining the constant output value, the pass element is used. It requires to transfer large currents under the low power regulation of the error amplifier from the source voltage to the load [4]. Bipolar or MOS transistors can be used to implement the pass element. Smaller power consumption and consequently higher efficiency are offered by the MOS transistor. The main advantage of using the MOSFETs as the pass transistor is that, in addition to some gain, it also is self protected to short circuit current. As such, the additional short circuit protection circuit is not needed to some point [19]. The MOS transistor can be either N or P type. The NMOS as the power transistor had a large dropout voltage. Therefore, the NMOS transistor requires a gate voltage higher than the source voltage. Thus, a charge pump is necessary to increase the voltage

level [16]. The proper choice for low voltage systems is PMOS LDO [18] for obtaining a low dropout voltage which also results stability problem [16]. The pass device influences loop gain, bandwidth, stability and dropout voltage.

Feedback network is a sampling resistor scales down the output voltage to a suitable value for comparing with the reference voltage by the error amplifier. To obtain the low power and voltage operation with small chip area, most of the transistors are designed to work at the sub threshold region and no resistor or bipolar transistor is required in voltage regulator. Feedback network in general is a voltage divider used to return part of the regulated voltage to the error amplifier input. If the desired regulated voltage is twice of the reference, the feedback network consists of two devices with same resistance in series with one end to output and one end to ground and the middle point connect to error amplifier.

VREF is used as a predefined reference level. A feedback signal of loading is compared with VREF by the error amplifier [20]. Off-chip external capacitors for to improving the transient-response and stability are at times required by the LDO regulators [4]. A voltage reference circuit is shown in Figure 3 [18].
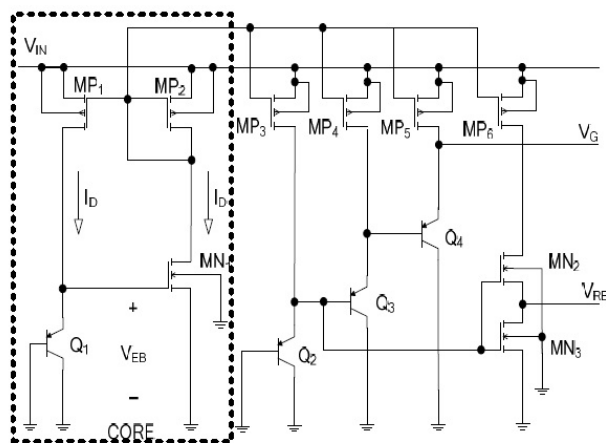

Fig. 3. Voltage reference circuit [18]

LDO linear regulator specification
Regulating performances, operating voltages and quiescent current are the vital characteristics to be considered during designing LDO. Output capacitor and equivalent series resistance (ESR) range, load regulation, input/output voltage range, drop-out voltage, line regulation and output voltage variation are the other specifications [4].

Quiescent or ground current is the difference between output and input currents. To maximize the current efficiency, the low quiescent current is needed. The value of quiescent current is determined by the biasing currents of band gap, sampling resistor and error amplifier. The load regulation is defined as how much the output voltage varies with load current which depends on the LDO loop gain, Aβ, and the output impedance of the pass device, r_{op}. The load regulation is approximately the ratio of the pass device output impedance to the loop gain. The smaller the output impedance of the pass device, the better is the load regulation. Since, the output impedance of the pass device cannot really be controlled, the loop gain should be designed to be high for best load regulation.

The line regulation of the LDO is defined as the output voltage variation due to input voltage variation. The output voltage should be independent of input voltage, so the ideal line regulation is zero. With a perfect input voltage reference, the dependent variables are loop gain, Aβ, and the gain of the pass device, g_{mprop}. The line regulation is the ratio of the pass device gain to the loop gain.

The dropout voltage of the LDO is defined as the minimum voltage drop across the pass device to maintain regulation. The dropout voltage is typically specified at maximum load current. The maximum load current specifications determine the size of the pass device, dropout voltage and power dissipation constraints. When the maximum load current specification increases, the overall die area of the pass device, the control circuitry and the ground pin current increases in order to drive the additional parasitic capacitances of the increased device sizing.

PSR and transient response performance scheme

The low dropout regulators suffer from Power Supply Rejection Ratio (PSRR) and transient response in their implementations [4-5]. The PSRR measures the LDO's ability to suppress the power supply noise [7]. It is also defined as how the output voltage changes with high frequency noise on the input voltage or the ability of a linear regulator to resist the high frequency noise at the input. The PSR is dependent on the pass device's parasitic capacitances and LDO loop gain.

There are two types of transients; load and line. Load transients occur when the output current rapidly changes levels, such as a 1mA to 200mA step in load current. Load transient response usually reflects the loop gain, bandwidth and stability of the regulator. Line transients occur when the input voltage rapidly changes levels, such as a 4V to 5V step. Line transient response usually reflects the PSR of the regulator. For both load and line transients, important specifications are overshoot, undershoot and response time and are usually shown as a plot with a particular output capacitor. Decoupling capacitors with different values will put at the input to filter out the high frequency noise.

MOS Resistor as Feedback Network

The LDO framework without any external discrete components at feedback network was proposed by as shown in Figure 4 [18]. To achieve low power consumption and small silicon area, a source follower stage (MNFOL) and the replacement of the resistive sampler (R1 and R2) were introduced. The sampler was replaced by a single MOS transistor along with a grounded MOS resistor (biasing from transistor MNAUX). The source follower stage (transistor MNFOL) was added in order to provide stability to the LDO system. This LDO regulator was designed for important conditions such as low power consumption and low silicon area due the lack of external discrete components.
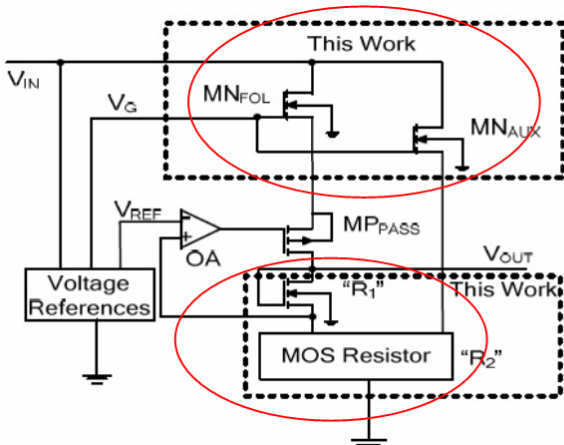
PSR enhancer

Recent improvement proposed by Park et al. as shown in Figure 5 was the PSR-compensated LDO architecture with single-ended two-stage error amplifier, PSR enhancer and frequency compensation circuit [8]. For error amplifier, a fully-differential PMOS input stage is used to achieve high power supply noise rejection. PSR enhancer consists of a scaled replica of the pass transistor, a current buffer, a current amplifier and a current mirror. To achieve the loop stability, the frequency compensation zero is required by the combination of differentiator and amplification stage [8]. The frequency compensation also used to improve the transient response of LDO.
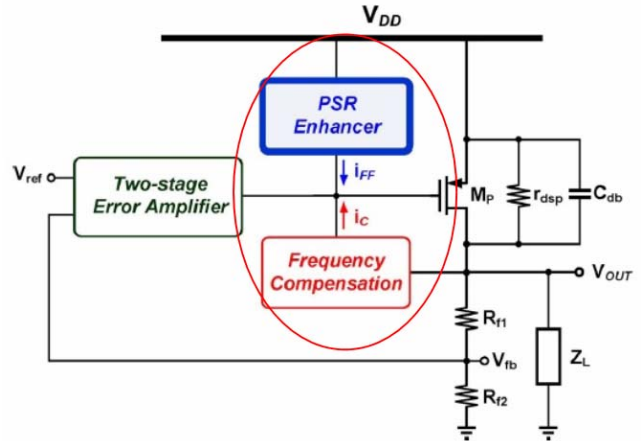

Fig. 5. PSR compensated LDO architecture [8]

Ganta et el. designed an LDO with transient and PSR enhancer [21]. The current amplifier was implemented by reusing the differentiator in the undershoot canceller as shown in Figure. 6. The current amplifier together with variable C_{vdd} serves as the PSR enhancer block. C_{vdd} samples and differentiates the power supply noise. The current is then converted into voltage by R1 and the converted back into current to the action of M2. Therefore, the capacitive current is then amplified by the current gain factor given by gm_2R_1 where gm_2 is the transconductance of transistor M2. Most of the circuits are reused for both functions: overshoot and power supply noise cancellation.
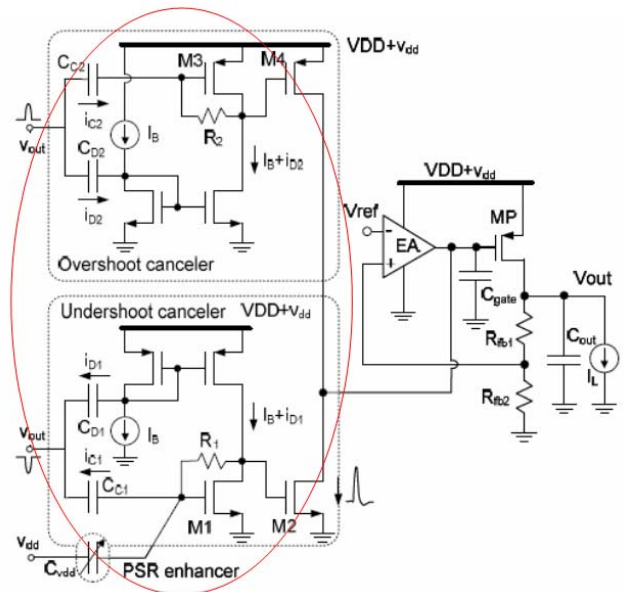

Fig. 4. Simplified diagram of linear voltage regulator [18]

Fig. 6. LDO with transient and PSR enhancer [21]

Super gain amplifier(SGA) and feed forward(FF) noise cancellation

The architecture of the LDO regulator proposed by Yuk et al. is shown in Figure. 7 [22]. It consists of an error amplifier (A_{e1} and A_{e2}), a summing amplifier As, a buffer amplifier B, a main power MOSFET MP, a frequency compensator and a feedback network. The feed-forward block was for improving the high-frequency PSR of the LDO regulator. The PSR of the conventional LDO regulator is largely determined by the loop gain at very low frequency. The loop gain also determines the PSR.
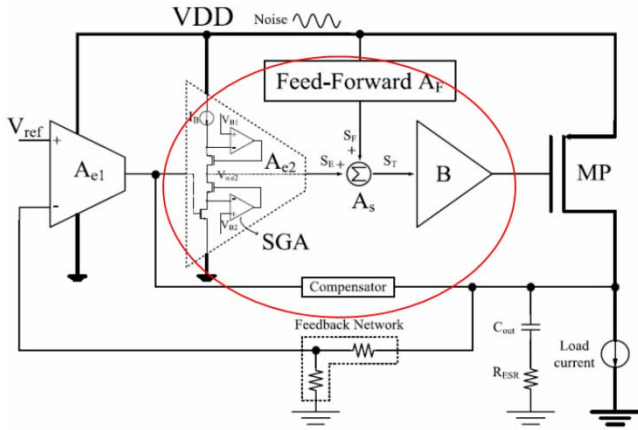

Fig. 7. Architecture of the LDO regulator [22]

High pass filter and replica feedback loop

A highpass filter added in the replica feedback loop is proposed by Coulot et al. [23]. Highpass filter was used to avoid the PSR variation at low frequencies. It feeds forward the supply ripple and filters the DC offset and low-frequency components of V_{rep}, corresponding to the difference between load and replica. Hence, the PSR is constant at low frequencies, independent of the corresponding between the load and the replica, and becomes dependent on the amplifier gain.
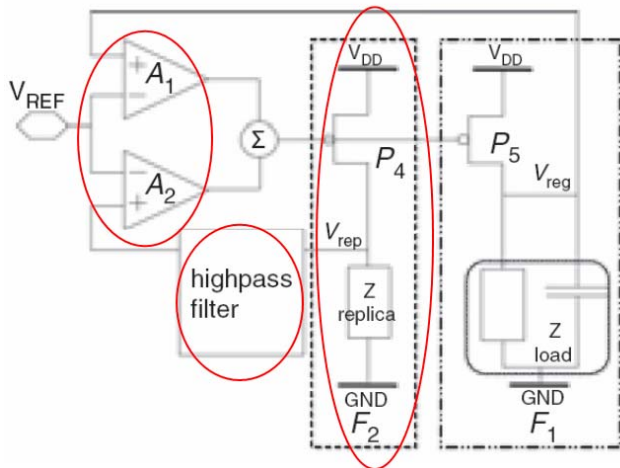

Fig. 8. LDO regulator with highpass filter [23]

Two stage cascaded OTA

The framework for LDO consisting of three main blocks: An error amplifier, a voltage reference and a pass transistor with external load capacitance with small value of internal resistance (ESR) for the frequency compensation is proposed by [19]. Error amplifier using two-stage cascaded OTA in CMOS technology having a single ended output was used in the proposed design. Pass transistor element is the pMOS transistor whose dimensions are set to withstand maximum output current of 450 *mA*. Thus, dimensions were *W*=8000 µ*m*, and *L*=1 µ*m*. Since, the

usage of pMOS is as pass transistor in open drain configuration, there is an issue in the output impedance being very high, causing a pole within the unity gain frequency, decreasing the phase margin. Therefore, an external load capacitance (C_L) with small value of internal resistance R_{ES}there were needed $_R$ so that it forms a zero, nullifying the effect of pole formed by high output impedance. C_L=35n*F* was chosen in the design.
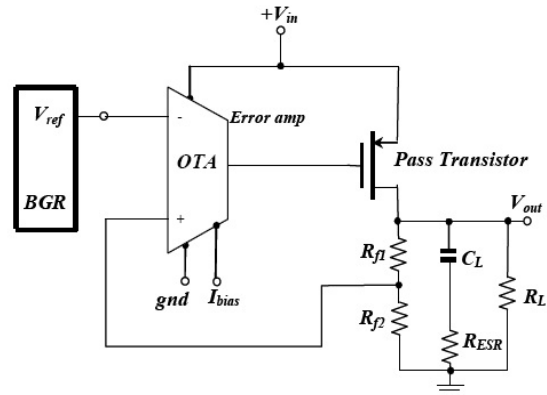

Fig. 9. LDO voltage linear regulator [19]

Voltage control current source(VCCS)

A buffer is required to drive the gate capacitance of PMOS while designing the LDO framework, to get a fast transient response. A significant pole is stimulated by the gate capacitance which degrades the stability. As such, to keep significant pole faraway away from the dominant pole, a buffer was required. The LDO regulator proposed by Lin and Liu consists of an error amplifier, a mirror stage (M1-M6), a power transistor (M_{pw}), feedback resistors and an output capacitor as shown in Figure 9 [6]. The mirror stage could keep the bias current of the mirror stage proportional to the output current. The current I_{M1} was equal to K_1xI_o. The quiescent current of the LDO can be written as I'_q =K_1x1_0+I_{qbase} where the $I'_{q,base}$ is a constant factor. As such, when *Io* is low, the power loss from Iq x V_{DD} can be decreased. The equation also shows that 1q will be big when Io goes high. In a heavy load condition, the large quiescent current may degrade the efficiency of the LDO. However, Io x Vo becomes dominant as found from the equation of η_2, when Io goes high. As such, the power loss resulted from Iq xV_{DD} does not reduces the efficiency much [6].
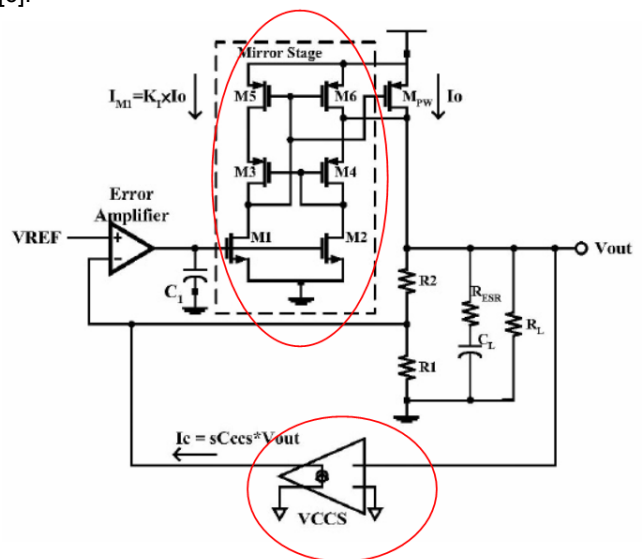

Fig. 10. LDO architecture with Mirror Stage and VCCS [6]

LDO with VCCS is proposed by Li et al. as shown in Figure 11. A zero depending on the equivalent capacitor C and the feedback resistor R2 of VCCS is created according to node current at node vx. A stable zero could be achieved with VCCS with C and R2 staying unchanged. LDO can operate active or sleep modes in the proposed design. A stable LDO was achieved with a small 1pF on-chip capacitor.
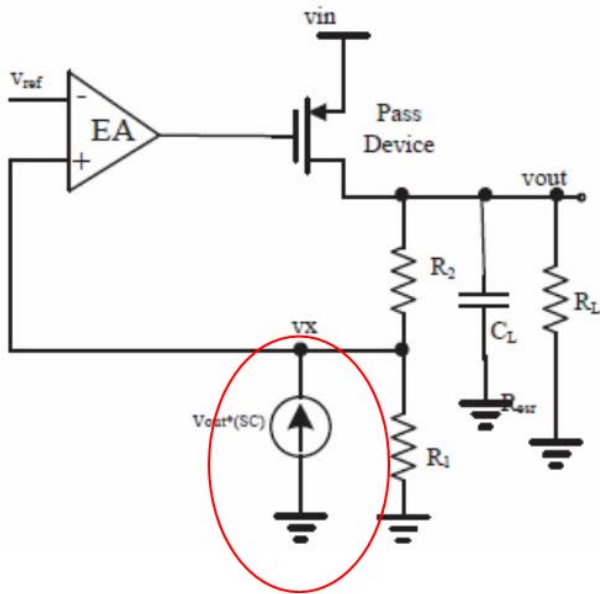
Fig. 11. LDO regulator with VCCS [16]

Three gain stages and current follower

LDO linear regulator presented by Huang et al. is shown Figure 12 [24]. The regulator consisted of three gain stages and a current follower (CF). Mc1–Mc5 and Ma1–Ma3 are the CF. CF was inserted between the Miller compensation capacitor, C_m and the output of the first stage. The lumped output parasitic capacitance of the first and second stage is C_{p1} and C_g. The equivalent open-loop output resistance of the LDO linear regulator is $1/g_{out}$ ($=R_L//R_{opass}//(R_{F1}+R_{F2})$). This LDO regulator employed with a single Miller capacitor to reduce the dips and peaks of the output voltage and the settling time.
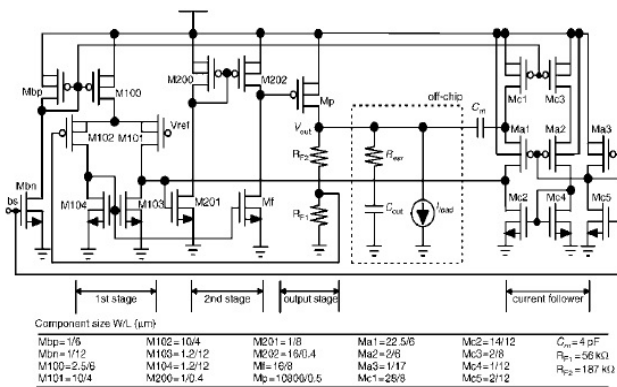
Fig. 12. LDO regulator [24]

ARC technique

The block diagram of the LDO with ARC technique proposed by Lin et al. is shown in Figure 13 [25]. The LDO was composed of a transconductance amplifier, a power transistor, an ARC circuit, an output capacitor with ESR and resistors. ESR frequency compensation was used to introduce a pole-zero cancellation to ensure closed-loop stability. It is a simple and popular method to compensate the phase margin of the system. However, in case of load variations, ESR degenerates the overshoot/undershoot voltage and limits the performance of the regulator. An ARC technique was used in order to overcome this issue.
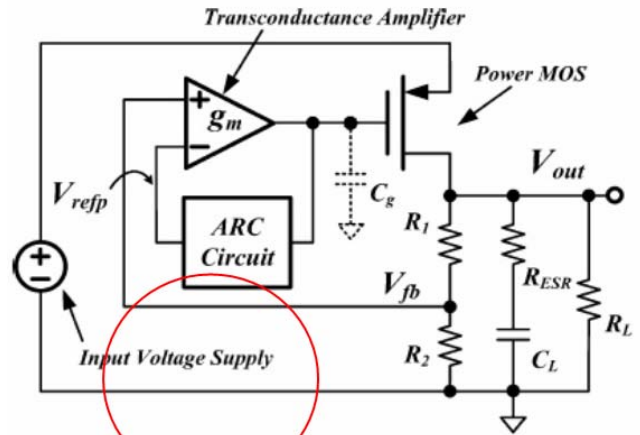
Fig. 13. LDO with ARC technique [25]

D² Coupling Technique

LDO architecture proposed by Zheng et al. is shown in Figure 14 [26]. The design was consisted of includes two feedback control loops; outer transient enhancement loop and inner error correction loop. The inner loop is active for all operation conditions and formed by the transistors. A direct dynamic (D²) coupling technique was used to improve the transient response. Voltage variation at V_{out} and V_{ref} is directly coupled to the voltage coupling node V_{cout} and V_{cref}. This was to adjust I_{out} and I_{ref} and to establish two direct sensing paths for DVS reference tracking and load transient. V_{out} can vary drastically during load or DVS transients as there is no output filter capacitor. An outer transient enhancement loop with an adaptive transmission control (ATC) scheme is employed to overcome this. To enhance the large signal transient, a high-slew-rate push-pull comparator with a flipped voltage follower (FVF) input stage was employed. Both the drop-out voltage and the quiescent current were maintained at low levels to achieve high power efficiencies and current.
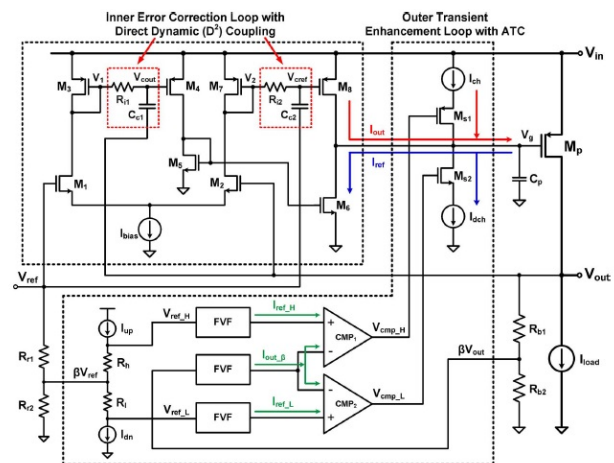
Fig. 14. System architecture of LDO regulator [26]

Buffer compensator

The error amplifier proposed by Al-shyouin et al. was realized by a transistors M1 – M6 with single-stage folded-cascade structure [27]. The pole p2 at the output of the

buffer was pushed sufficiently high frequencies by using dynamically biased shunt feedback with different load currents. The pass device Mp recognizes a common-source gain stage and be the second gain stage in the LDO. As such, the LDO structure can be utilized as a two-stage amplifier driving a large capacitive load with two poles located the LDO output and at N1. The utilization of a μF range off-chip output capacitor C_L makes the capacitive load large. Current-buffer or cascode-Miller frequency compensation wa used in the LDO structure for stabilization. The pole-splitting compensation was aimed for splitting two poles p_1 at N_1 and p_0 at the LDO output to attain constancy in the full range of the load current.
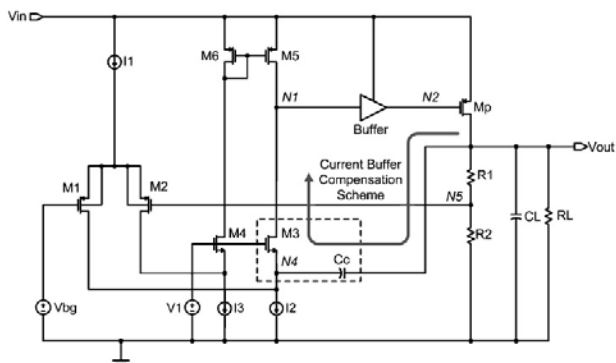

Fig. 15. LDO using current-buffer compensation scheme [27]

A framework with programmable output was proposed by Wu and Huang as shown in Figure 16 [5]. The design included error amplifier, power transistor, output off-chip compensated circuit (Resr, CL), feedback network (R1, R2, R3, R4), logic circuit and reference voltage to control the programmable output voltage for low dropout regulator. For decreasing the power consumption and dropout voltage of LDO as low as possible, large ratio of the channel-width-to channel- length was created. This increased the gate capacitance of the power transistor. With the large gate capacitance, the loop stability of LDO degraded. To generate a pole at high frequency, a buffer with low output impedance was added in between the power transistor and the error amplifier. The loop speed was improved when the buffer split the poles like the regular Miller compensating scheme. Two NMOS switch transistors and two resistors were added to form an adjustable LDO circuit to design a LDO with programmable output. The NMOS transistors were acted as an open-circuit or a short-circuit according to the control logic of the NMOS switch transistors. Thus, the

programmable LDO was able regulate four various voltages which was 0V, 1.8V, 2.5V and 3.3V. The LDO's transient response improves when the current compensation circuit is added in front of the buffer [5].
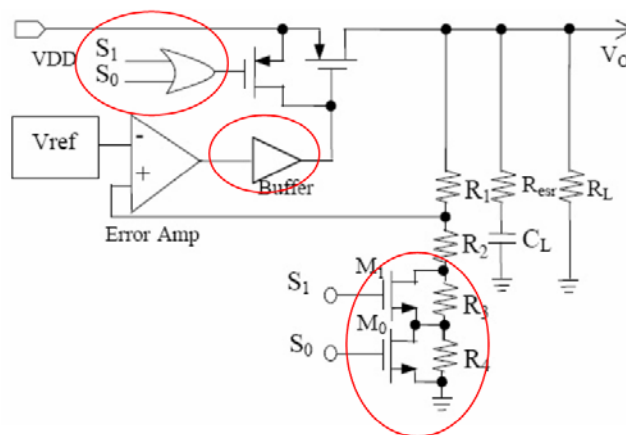

Fig.16. Framework of LDO [5]

Gong et al. proposed an LDO as shown Figure 17 [7]. The system consisted of PMOS pass transistor, an error amplifier, the stepping several stages Miller compensation capacitor *C2*, Transient Enhancement Unit (TEU), buffer and feedback resistors *R1* and *R2*. The PSRR performance for this circuit improved significantly to 50dB at 1MHz and 51dB at 100 KHz. 1pF Miller compensation capacitor was only used.
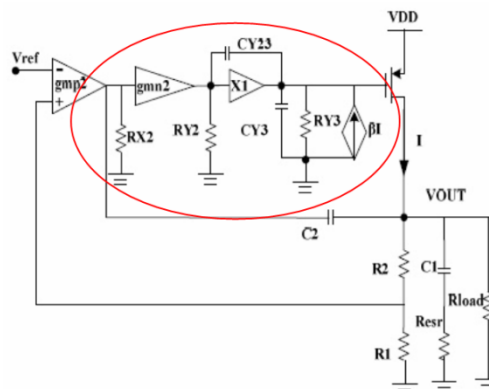
Fig. 17. Structure of LDO with TEU [7]

Table 3. Performance comparison PSRR and Transient scheme for LDO regulator

Ref	LDO Scheme	CMOS Tech. /μm	Parameter					PSR (dB)	Transient Response
			V_{out} (V)	Dropout (mV)	Iq (μA)	Line reg. mV/V	Load reg. mV/mA		
[8]	PSR Enhancer	0.18	1.6	200	55	75	0.14	-70dB @1MHz -37dB @10MHz	0 to 50mA @0.1μs
[21]		0.18	N/A	200	0.018	N/A	0.03	-55dB @1MHz	0 to 50mA @1μS
[7]	Buffer	0.35	N/A	767	0.063	2	0.5	-51.5dB @100KHz -50dB @1MHz	1mA to 100mA @0.1μS
[27]		0.35	1.8	200	20	2	0.17	>45dB@ 0-20kHz	1 to 200mA @0.1μs
[5]		0.35	3.3 2.5 1.8	410 500 690	0.17 0.16 0.14	N/A	N/A	-63dB -68dB -71dB @1kHz	0 to 100mA @2μS

[6]	VCCS	0.35	2.5	N/A	24	N/A	20	N/A	1 to 138mA @2µS
[16]		0.35	1.8	N/A	N/A	N/A	N/A	N/A	1 to 100mA @0.1µs
[22]	SGA&FF	0.065	1	200	150-350	N/A	<0.04	-61dB @1MHz -47dB @10MHz	N/A
[19]	2 Stages OTA	0.35	4.5	50 500 150	N/A	3.2 3.4 3.2	0.012	-54.45dB @100Hz -34.31dB @10kHz	N/A
[24]	3 Stages OTA	0.35	1.8	220	53	N/A	92.8 ppm/mA	N/A	0 to 150mA @3.2µs
[18]	MOS resistor	0.35	1	47	35.7	39	13	-38dB @10MHz	N/A
[23]	HPF& replica loop	0.09	1.2	200	140	N/A	N/A	-60dB@ 100MHz	1 to 50mA @0.1ns
[25]	ARC	0.35	2	60	40	5	0.06	N/A	1 to 100mA @10µs
[26]	D^2 Coup	0.35	1-3.1	200	42	<1.5%	<1.7%	N/A	2µs

Discussion

It is revealed from the above review that the performance of LDO can be evaluated by the drop out voltage, quiescent current, line regulation, load regulation, PSR and transient response as shown in Table 1. Various researchers employed several techniques to increase the performance of LDO regulator. The chosen technique was dependent on the application of the device.

The PSR and transient response were improved by adding the frequency compensation with PSR enhancer in LDO circuit in [8]. At 1MHz, the PSR improved about 19dB compared to the proposed design by [21] which was without frequency compensation. The transient response was 0.1µs at 0-50mA operating range. Therefore, the frequency compensation was used to improve the transient response and with the PSR enhancer scheme. This improved the performance of PSR. The LDO structure proposed by [8] offered an effective way to solve the PSRR and transient response performance to meet the demands of low noise power supply

To improve the transient response performance, buffer was attached in the LDO circuit between error amplifiers and pass transistor. In [5], the performance of transient response was increased when LDO circuit added with buffer. To increase the performance on transient response, the LDO can add with the buffer and transient enhancement unit (TEU) or LDO, buffer and 2 stages OTA at error amplifier [7, 27]. LDO in has a good transient response performance due to the TEU unit which was 0.1µs from 1mA to 100mA [7]. But the LDO proposed by [27], offered better performance for transient response which was 0.1µs from 1mA to 200mA.

To increase the transient response performance, VCCS also can add in LDO architecture. VCCS was used to perform a real stable LDO and very small compensation capacitor. In [16], the performance of transient response was 0.1µs from 1mA to 100mA. The result showed that the performance in term of transient response were same for [7] and [16].

The PSR variation at low frequencies can be avoided by using the high pass filter (HPF) which includes in replica loop as proposed by [23]. The performance for transient response and PSR were improved in the design. The PSR reached better than 60dB over the whole of simulated frequency range (from 1kHz to 100MHz). To make the programmable output for LDO, two NMOS and switch transistor can be add by series it with feedback network as shown in [5]. All the frameworks that have been discussed can be used to improve the PSR and transient response performance in LDO.

Conclusion

The paper has discussed on the evolution on LDO voltage regulator. From the review, it is found that that even though there are various frameworks that have been implemented for LDO, the selection of the framework is based on the applications of the systems. The framework of LDO is mainly dependent on PSR, transient response performance or both of them. The transient response performance is majorly dependent on the added buffer between error amplifier and pass transistor. The PSR performance is majorly depends on the pass device capacitance and the LDO loop gain. The demand for low voltage shall remain a challenging and active research area for years to come. Thus, this review shall work as a guideline for the researchers who wish to study on the LDO.

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