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ZVS single-switch inverter for induction heating – optimum operation

Abstract. *The optimum operation of a single-switch class E transistor inverter for induction heating has been discussed in the paper. The graphs of the most important inverter parameters as a function of the values of the resonant circuit components are shown. The results presented have been illustrated with some current and voltage waveforms obtained on the basis of mathematical analysis as well as using IsSpice simulation program. A concept of a control system has also been presented, which should ensure nearly optimum operation of the inverter.*

Streszczenie. *W artykule omówiono pracę optymalną jednołącznikowego tranzystorowego falownika klasy E do nagrzewania indukcyjnego. Przedstawiono wykresy najważniejszych parametrów falownika w funkcji wartości elementów obwodu rezonansowego. Podano przykładowe przebiegi czasowe prądów i napięć w falowniku otrzymane zarówno na podstawie analizy matematycznej, jak i poprzez symulacje w programie IsSpice. Przedstawiono również koncepcję układu sterowania falownika, który powinien zapewniać pracę w warunkach bliskich optymalnym.* ***(Jednołącznikowy falownik z przełączaniem ZVS do nagrzewania indukcyjnego - praca optymalna)***

Keywords: single-switch topology, ZVS, class E inverters, induction heating
Słowa kluczowe: układ jednołącznikowy, ZVS, falowniki klasy E, nagrzewanie indukcyjne

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Introduction

Several topologies of single-switch inverters are used, among others, to carry out induction heating. One of them, shown in Figure 1, is the subject of the paper. This class E ZVS inverter is presented in literature [1-7], especially in connection with its application in induction cookers operating usually in the range of 20 ÷ 50 kHz.

The author's aim is to analyze the inverter properties and next to test it experimentally in an induction-heating appliance at a frequency of several hundred kilohertz, that is a frequency which is circa one order higher than the one used in induction cookers. Therefore, a special emphasis will be put on the optimum operation of the inverter which minimizes turn-on losses in the transistor.

Principle of operation

The inverter (Fig. 1) is supplied from a DC voltage source U_d. Resistance R_0 and inductance L_0 represent the inductor-charge system. The power electronic switch S can conduct current in both directions.

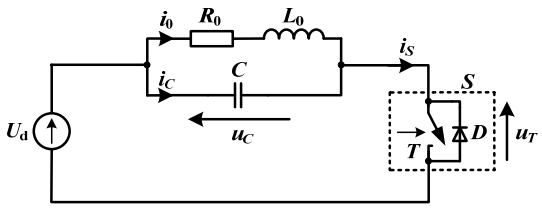

Fig. 1. Circuit diagram of the single-switch inverter

It is advantageous that the inverter operates in a way assuring switching the transistor at zero voltage (ZVS). In each switching cycle the inverter operates in two modes and its equivalent circuits for each mode are shown in Figure 2:

– In mode I switch S conducts electrical current. The voltage u_C across C and R_0L_0 is practically constant and equal to U_d and load current i_0, equal to switch current i_S, rises exponentially.
– In mode II switch S is off. An oscillation occurs in the R_0L_0C circuit, which lasts until u_C reaches the supply voltage U_d.

Two cases of ZVS operation of the inverter are distinguished in Figure 3:

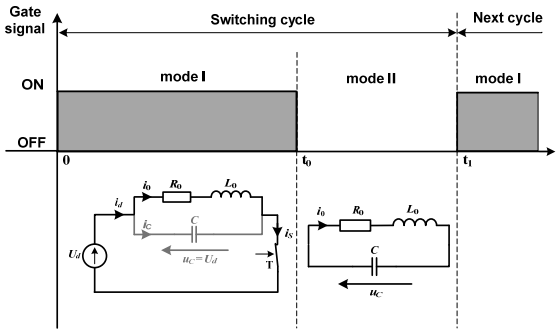

Fig.2. Equivalent circuits of the inverter in modes I and II

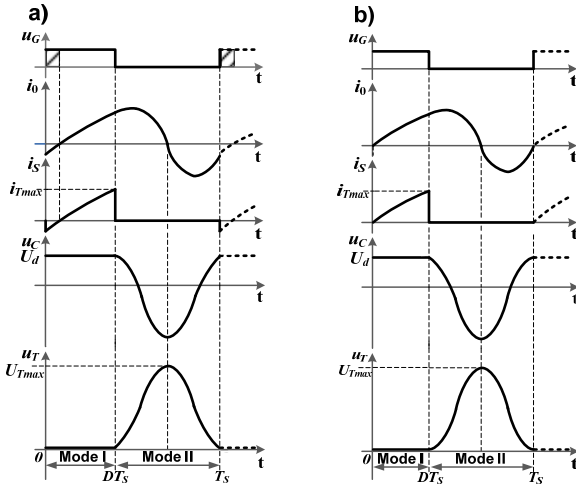

Fig. 3. Current and voltage waveforms in the inverter under ZVS operation: a) suboptimum operation; b) optimum operation; u_G – gate signal, i_0 – load current, i_S – switch current, u_C – voltage across the capacitor, u_T – voltage across the switch

– In the first case – suboptimum operation - voltage u_c reaches the value of supply voltage U_d while current i_0 is negative (Fig.3a). Freewheeling diode D starts conducting, which determines the end of mode II and the beginning of mode I of the next switching cycle. At time interval between the beginning of diode conduction and the instant when current i_0 reaches zero (the shaded area of gate signal u_G in

Figure 3a) the gate signal should be applied to the transistor so that it can take over the diode current.

– The other case - optimum operation - occurs if voltage u_c reaches U_d at the same time when current i_0 reaches zero (Fig. 3b). The transistor should be turned on at this moment, which initiates mode I of the next cycle. The transistor is turned on at zero voltage and zero current; therefore the turn-on losses in the transistor are zero.

The inverter can also be operated at hard switching. If the transistor conduction time is too short or damping of the resonant circuit is too big, voltage u_C will never reach the supply voltage in mode II. As a consequence, it will be necessary to turn the transistor on at non-zero voltage (NZVS), which generates turn-on losses in it. Therefore, this kind of the inverter operation should be avoided.

General equations for the inverter

The mathematical analysis of the inverter of Figure 1 is based on the following assumptions:

– switch S and all the other circuit components are ideal,
– supply voltage U_d is constant in one switching cycle,
– inverter operates in steady state.

The current and voltage waveforms are as follows:

(1)
$$i_{0n}(\omega_s t)=\begin{cases}\dfrac{1}{2}\sqrt{1+\dfrac{1}{\alpha_{0n}^2}}+\\ +\left(i_{0n}(0)-\dfrac{1}{2}\sqrt{1+\dfrac{1}{\alpha_{0n}^2}}\right)\exp\left(-2\dfrac{\alpha_{0n}}{\omega_{sn}}\omega_s t\right)\\ \quad \text{for } 0<\omega_s t\le 2\pi D\\ \exp\left(-\dfrac{\alpha_{0n}}{\omega_{sn}}(\omega_s t-2\pi D)\right)\\ \cdot\left[i_{0n}(2\pi D)\cos\left(\dfrac{\omega_s t-2\pi D}{\omega_{sn}}\right)+\right.\\ \left.+\left(\sqrt{1+\alpha_{0n}^2}-\alpha_{0n}i_{0n}(2\pi D)\right)\sin\left(\dfrac{\omega_s t-2\pi D}{\omega_{sn}}\right)\right]\\ \quad \text{for } 2\pi D<\omega_s t\le 2\pi\end{cases}$$

(2)
$$u_{Cn}(\omega_s t)=\begin{cases}1 \quad \text{for } 0<\omega_s t\le 2\pi D\\ \exp\left(-\dfrac{\alpha_{0n}}{\omega_{sn}}(\omega_s t-2\pi D)\right)\\ \cdot\left\{\cos\left(\dfrac{\omega_s t-2\pi D}{\omega_{sn}}\right)+\right.\\ \left.+\left[\alpha_{0n}-\dfrac{1}{2}\left(\alpha_{0n}+\dfrac{1}{\alpha_{0n}}\right)\right.\right.\\ \left.\left.\cdot\left(1-\exp\left(-4\pi D\dfrac{\alpha_{0n}}{\omega_{sn}}\right)\right)\right]\right\}\\ \cdot\sin\left(\dfrac{\omega_s t-2\pi D}{\omega_{sn}}\right)\\ \quad \text{for } 2\pi D<\omega_s t\le 2\pi\end{cases}$$

(3)
$$u_T(\omega_s t)=U_d-u_C(\omega_s t) \quad \text{for} \quad 0<\omega_s t\le 2\pi$$

in which

(4)
$$i_{0n}=\frac{i_0}{\frac{U_d}{Z_0}};\ u_{Cn}=\frac{u_C}{U_d};\ \alpha_{0n}=\frac{R_0}{2\omega_0 L_0};\ \omega_{sn}=\frac{\omega_s}{\omega_0}$$

where

(5)
$$Z_0=\sqrt{\frac{L_0}{C}};\ \ \omega_0=\sqrt{\frac{1}{L_0C}-\left(\frac{R_0}{2L_0}\right)^2}$$

are characteristic impedance and natural frequency of a series R_0L_0C circuit, $\omega_s = 2\pi f_s$ is the operating angular frequency of the inverter and D is switch duty ratio.

The parameter α_{0n} can be replaced by Q-factor

(6)
$$Q=\frac{\sqrt{\frac{L_0}{C}}}{R_0}=\frac{1}{2}\sqrt{1+\frac{1}{\alpha_{0n}^2}}\ .$$

Optimum operation of the inverter

Class E inverters greatly reduce the transistor power losses occurring during the off-to-on transition of the device [8]. In order to achieve this in the inverter under discussion, the optimum turn-on conditions have to be fulfilled:

(7)
$$u_T(2\pi)=0;\quad \frac{du_T}{dt}(2\pi)=0\ \Rightarrow\ i_0(2\pi)=0\ .$$

Load current i_0, voltages u_C and u_T for optimum operation can be calculated using (1) – (4) after substituting $i_{0n}(0) = 0$. Substitution of (7) into (1) – (3) yields the relationships among α_{0n}, D and ω_{sn}, which are given by the system of equations

(8)
$$\left[1-\exp\left(-4\pi D\frac{\alpha_{0n}}{\omega_{sn}}\right)\right]\cos\left(\frac{2\pi(1-D)}{\omega_{sn}}\right)+$$
$$+\alpha_{0n}\left[1+\exp\left(-4\pi D\frac{\alpha_{0n}}{\omega_{sn}}\right)\right]\sin\left(\frac{2\pi(1-D)}{\omega_{sn}}\right)=0$$

(9)
$$\exp\left(-2\pi(1-D)\frac{\alpha_{0n}}{\omega_{sn}}\right)\left\{\begin{array}{l}\cos\left(\dfrac{2\pi(1-D)}{\omega_{sn}}\right)+\\ +\left[\alpha_{0n}-\dfrac{1}{2}\left(\alpha_{0n}+\dfrac{1}{\alpha_{0n}}\right)\right.\\ \left.\cdot\left[1-\exp\left(-4\pi D\dfrac{\alpha_{0n}}{\omega_{sn}}\right)\right]\right]\\ \cdot\sin\left(\dfrac{2\pi(1-D)}{\omega_{sn}}\right)\end{array}\right\}=1$$

The system of equations was solved numerically [9] and the results for a single oscillation in mode II are shown in Figure 4a. The transistor must be controlled with a duty ratio and switching frequency which depend on Q (α_{0n}), determined by the circuit components. Increase in α_{0n} results in increase in D and decrease in ω_{sn}. The inverter optimum operation is possible only for α_{0n} < ca 0.1953 (Q > ca 2.6085). For smaller values of Q voltage u_T never reaches U_d in mode II and soft turn-on of the transistor is not possible.

An increase in α_{0n} results in an increase of maximum transistor current I_{Tmax} and voltage U_{Tmax} as well as of inverter power P. Normalized values of these quantities (10) are shown in Figure 4b.

(10) $$I_{\mathrm{Tnmax}} = I_{T\max}\frac{Z_0}{U_\mathrm{d}}; U_{\mathrm{Tnmax}} = \frac{U_{T\max}}{U_\mathrm{d}}; P_\mathrm{n} = P\frac{Z_0}{U_\mathrm{d}^2}$$

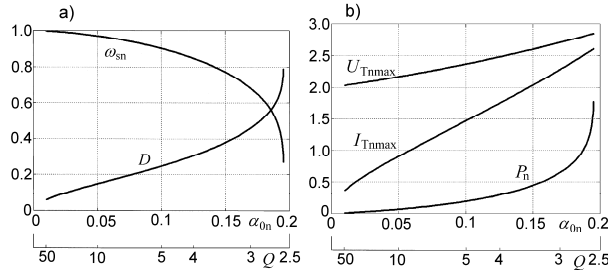

Fig. 4. Dependences for optimum operation of the inverter: a) relationships among α_{0n} (Q), D and ω_{sn}, b) normalized maximum transistor current, maximum transistor voltage and inverter power

Idealized waveforms of the inverter currents and voltages for optimum operation are plotted in Figures 5a and 5b. An increase in load current distortion for lower Q is clearly visible.

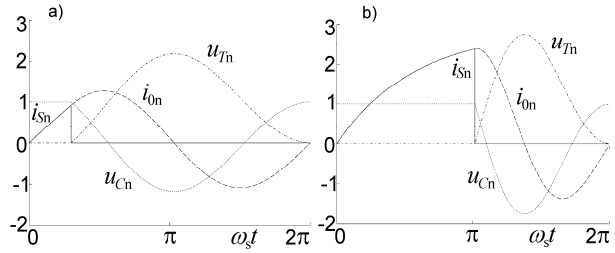

Fig. 5. Idealized waveforms in the inverter operated optimally at: a) lower damping: α_{0n} = 0.0507 (Q = 9.87), D = 0.1486, ω_{sn} = 0.9696, b) higher damping: α_{0n} = 0.1780 (Q = 2.8531), D = 0.5050, ω_{sn}= 0.6275

Figures 6a and 6b show waveforms of currents and voltages at optimum operation for inverters with parameters corresponding to those from Figures 5a and 5b, respectively, obtained using IsSpice simulation program. In view of using a model of the transistor IRFP260 in the simulations it was necessary to slightly modify the transistor conduction time t_1 and the duration of the switching cycle as compared with the values determined from relationships in Figure 4a.

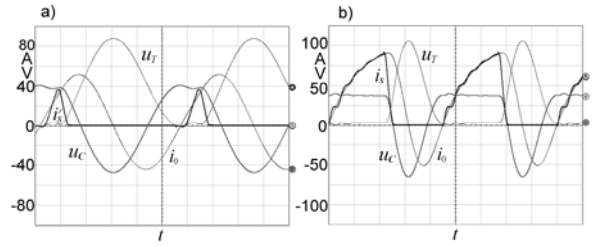

Fig. 6. IsSpice waveforms for circuits corresponding to the ones shown in: a) Figure 5a) - U_d = 40 V, R_0 = 0,101 Ω, L_0 = 0,42 μH, C = 0,423 μF, t_1 = 0.45 μs, f_s = 361 kHz, b) Figure 5b) - U_d = 40 V, R_0 = 0,3493 Ω, L_0 = 0,42 μH, C = 0,423 μF, t_1 = 2.17 μs, f_s = 222 kHz

Figure 7 shows the computed harmonic spectrum of the load current waveform given by (1) with $i_{0n}(0)$ = 0 for four different values of α_{0n} (Q). $I_0(n)$ is the amplitude of the n-th harmonic of the load current and $I_0(n)/I_0(1)$ is the amplitude of the n-th harmonic of the load current normalized to the fundamental-frequency component of the load current. The constant component and the harmonic content in the load current increase with α_{0n} (Figs. 5a and 5b) and the rate of the increase is especially high at high values of α_{0n} (low values of Q). The presence of the constant component in the load current in the inverter used for induction heating is disadvantageous.

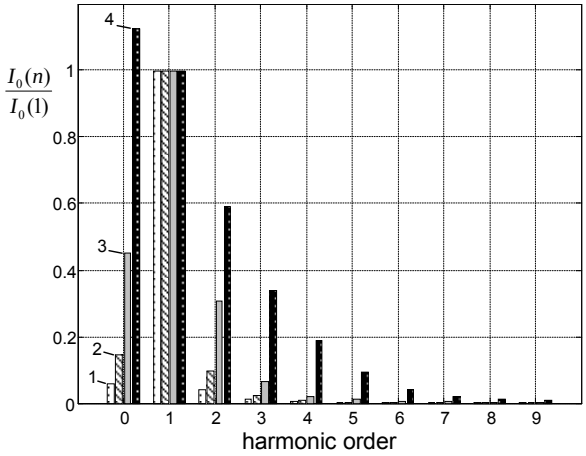

Fig. 7. Harmonic components of current i_0 for: 1 - α_{0n} = 0.0507 (Q = 9.87); 2 - α_{0n} = 0.102 (Q = 4.93); 3 - α_{0n} = 0.178 (Q = 2.85); 4 - α_{0n} = 0.195 (Q = 2.61)

Concept of the inverter control system

The concept of the inverter control system (Fig. 8) is based on the use of four functional systems: the detector of zero of load current, transistor's current limiter, capacitor's voltage regulator and pulse generator for transistor control with adjustable pulse width control.

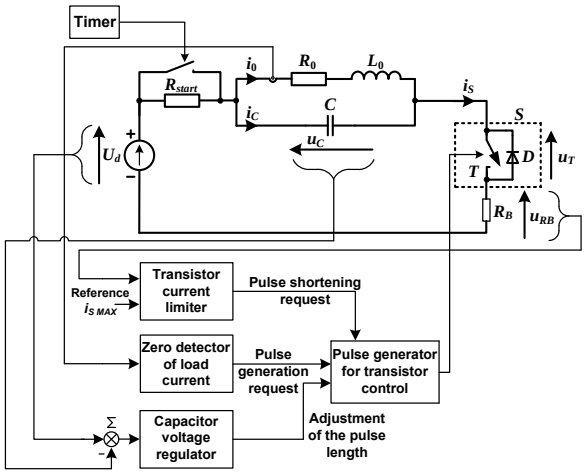

Fig.8. Block diagram of the inverter control system

Detection of zero (from negative values) of load current i_0, marks the point to turn on the switch S (modulation of transistor T). Thus, the transistor begins to conduct the current and the energy is stored in the inductance of the inductor.

The length of control pulse of transistor is initially minimal (e.g.: 10% of the switching cycle, that is, D = 0.1). Consequently there is an oscillation in the resonant circuit, and a measure of energy, related to the conduction time of the transistor is the maximum voltage across the capacitor.

The signal which is the difference of the measured maximum positive voltage u_C (after the resonant process the voltage across the capacitor should be equal to the supply voltage) and voltage U_d is applied to the input of the capacitor voltage regulator.

The output signal of the regulator determines the length of the transistor conduction time (increase or decrease of the current value of the D-factor), and also determines the amount of energy supplied to the resonant circuit. As a

result, the regulator reduces the error of control to zero and the transistor tends to be switched on at zero voltage (optimum operation). u_C voltage adjustment will be executed in many control periods, but with an accuracy of a few millivolts.

If the output of transistor's current limiter (voltage measurement on the shunt R_B), does not block switching on the transistor, it will conduct the current during time interval corresponding to the value of the D-factor determined by the regulator. If the current exceeds the limit value of i_S, resulting from the parameters of the transistor, the conduction time will be reduced accordingly.

The inverter contains a starting system, which is necessary due to the structure of the inverter circuit. The system is implemented with an additional start-up resistor limiting a peak of current loading the capacitor of the resonant circuit. After start-up the resistor is short-circuited. This can be realized using a simple timer circuit (for example NE555) with an adjustable time delay.

Some tests have been performed to check the proper operation of the presented control system. A 10-wire inductor was loaded with a steel rod. Figure 9 shows some registered waveforms. Load current is nearly a sine wave. At turn-off of the transistor a significant peak can be seen in the waveform of the voltage u_T across the transistor, which is a result of the presence of parasitic inductances in the circuit. It increases the turn-off losses in the transistor and worsens the inverter efficiency. This drawback can be minimized by changing the layout of the inverter.

In case of load variation the inverter returned, after transient state, to optimum operation mode with new control parameters (transistor conduction time and switching frequency).

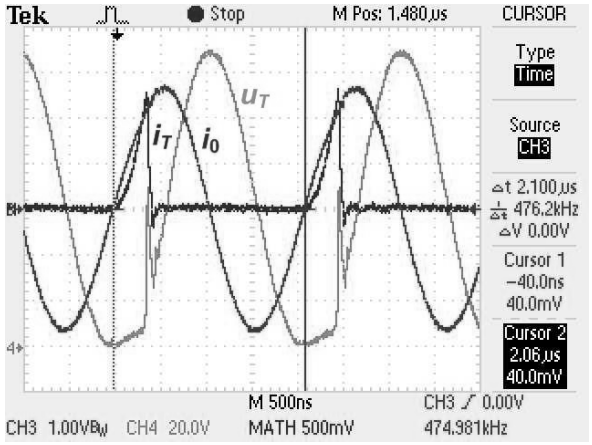

Fig.9. Waveforms of the load current i_0 (25A/div), the transistor voltage u_T (20V/div) and transistor current i_T (25A/div) in a model of the inverter with steel load inside the inductor: U_d = 59 V, C = 0.329 μF

Conclusions

The inverter under analysis can be operated optimally in class E if the Q-factor (6) is high enough (Q > ca 2.61). Based on the plots given in the paper it is possible to determine conduction time of the transistor and its switching frequency for an inverter with given network parameters. Maximum values of transistor current, transistor voltage and the inverter power can also be determined.

Power of the inverter operated optimally can be controlled by means of varying supply voltage. The alternative is abandoning optimum operation by increasing adequately the transistor conduction time and its switching cycle, which results in power increase while maintaining ZVS switching (Fig.3a).

The advantage of the inverter is that it needs only one power electronic switch. The disadvantages are: content of a constant component and higher harmonics in the load current and high voltage across the transistor. However, the latter is less important in case of using a power-electronic device of new generation, e.g. a SiC transistor.

Preliminary tests of the presented control system have been carried out at frequencies of several hundred kilohertz and they confirmed its correct operation. In order to minimize turn-off losses in the transistor, the layout of the inverter should be modified to minimize parasitic inductances.

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