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Comparison on Staircase, PWM and Partial PWM Scheme for Hybrid Cascaded Multilevel Inverter

Abstract. *Cascaded Multi-level Inverter (CMLI) consists of H-bridge modules which can generally be divided into the one with the same DC bus voltage and another with different DC bus voltages. By using the same power devices as a standard seven-level 3H-bridge converter, the proposed converter operates with 15-level resolution, with separate DC voltage sources of voltage ratio 4:2:1. The total harmonic distortion (THD) and switching losses of the proposed hybrid cascaded converter among staircase, PWM and partial PWM control are compared with analysis and Saber simulation.*

Streszczenie. *W niniejszym artykule przedstawiono trzy metody modulacji dla 15-poziomowego kaskadowego falownika hybrydowego. Dokonano porównania analitycznego i symulacyjnego metod przełączania schodkowego, modulacji PWM i częściowej PWM pod względem THD oraz strat łączeń. Analiza i symulacja wyników wykazują, że proponowane metody modulacji pozwalają na uzyskanie wysokiej jakości napięcia. (**Porównanie metod Staircase, PWM i częściowego PWM dla hybrydowego kaskadowego falownika wielopoziomowego**).*

Keywords: Hybrid cascaded multilevel inverter, Staircase modulation, PWM, Partial PWM, THD
Słowa kluczowe: hybrydowy kaskadowy przekształtnik wielopoziomowy, Modulacja schody, PWM, częściowe PWM, THD

Introduction

Multilevel converters have become an essential part of the high-power application area recently. Cascaded by a series of H-bridge modules supported by several individual DC sources [1], the Cascaded Multilevel Inverter (CMLI) can provide higher resolution output voltage which largely increases the output power and reduces harmonics of AC waveforms comparing to the single H-bridge inverter [2].

Conventional multilevel inverters such as Diode Clamped Multilevel inverters [3-6], Flying Capacitor Multilevel inverters [7-10] and Cascaded Multilevel Inverters [11-13] have some drawbacks if the number of voltage levels increases. The cost of the switching components and capacitors increases quickly as the number of voltage levels grows, and it also happens to the complexity of their implementations [14].

By applying different voltage ratios to different individual DC sources which support the H-bridge modules of the conventional CMLI, the conventional CMLI then becomes a hybrid CMLI, which can produce more voltage levels without increasing the number of H-bridge modules [15]. Hence, the THD of output voltage can be reduced as more voltage levels lead to an output voltage closer to the referenced sinusoid waveform. Hybrid CMLI can be applied in many application, such as Solid-State Transformer [16], static var compensator, active power filter [17] and renewable energy generation [18].

For hybrid CMLI, both staircase and PWM are presented in 5-level, 7-level and 9-level output waveforms with unequal cell voltages [19], and staircase and partial PWM are presented in 31-level output waveform with DC voltage ratio 8:4:2:1 [15]. However, those researches mainly focus on the topologies, instead of the modulation schemes.

In this paper, PWM, partial PWM and staircase modulation scheme are proposed to control a 15-level inverter, which consisted of 3 H-bridge modules with DC voltage ratio 4:2:1. For this purpose, a simulation model is built in Saber environment. The simulation results of different modulation schemes are compared based on Total Harmonic Distortion (THD), low-order harmonics and switching losses. Due to the results of the comparison, one may select the proper modulation scheme for specific application for larger reduction on filter size and higher efficiency.

Section 2 gives the topology, operational principles and switching patterns of the conventional 7-level inverter and the proposed hybrid 15-level inverter. It also gives the theoretical background and the design details of the proposed staircase control scheme with its modification. Section 3 illustrates the simulation results of the proposed 15-level cascaded H-bridge inverter in staircase modulation, PWM and partial PWM schemes. Conclusions are given in Section 4.

Topology and schematic of the 15-level inverter

Figure 1(a) shows the basic schematic of 3 H-bridge 7-level inverter [1] for a single phase system which can provide an output with 7 voltage levels including 0, -1Vpu, -2Vpu, -3Vpu, 1Vpu, 2Vpu and 3Vpu. Those 7 voltage levels are formed by controlling 12 switches (S11 to S34), integrating H-bridge inverters connected in cascade. Hence, the output voltage is the sum of the voltages of H-bridge modules which are supported by the same DC voltage sources.

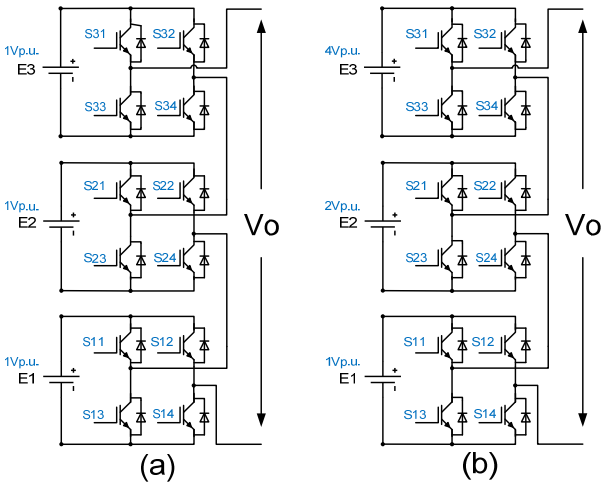

Fig.1. (a) Conventional 7-level CMLI; (b) Proposed hybrid 15-level CMLI

By changing the voltage of the DC power source to the ratio of 4:2:1, the conventional 7-level inverter can provide an output with 15 voltage levels including 0, -7Vpu, -6Vpu, -5Vpu……5Vpu, 6Vpu and 7Vpu. The topology of 3 H-bridge 15-level inverter is shown in Figure 1(b).

The main advantages of the proposed inverter comparing to the conventional one are:

1) The cost can be reduced by replacing high frequency switching components to low frequency ones.
2) Larger number of voltage levels and lower harmonic distortion with the same topology.
3) The increase in the number of voltage levels leads to an improvement on power quality and reduction on the size and power loss of filter.

The disadvantages are:

1) The larger the number of voltage levels is, more complex that the control of inverter becomes.
2) The high frequency switching switches generate more power losses than the low frequency switching ones; hence resulting in more losses and shorter lives.

In order to generate 15 levels output voltage, one must add the voltages of different DC sources as the output voltage is the sum of the DC voltage sources. Hence, the 15 voltage levels are synthesized as shown in Table 1. As the DC sources are usually supported by voltages across the electrolytic capacitors or batteries, the switching patterns that form the 15 voltage levels therefore only allow the DC voltage sources to be connected with the same polarity [3]. By avoiding having the electrolytic capacitors connected in the opposite polarity, it can prevent the unexpected power flowing among them, which always causes the voltage rise and voltage drop of the electrolytic capacitors.

Table 1. Switching table of the proposed 15-level inverter

V(p.u.)	Switching Patterns	V(p.u.)	Switching Patterns
7	+1+2+4	-7	-1-2-4
6	+2+4	-6	-2-4
5	+1+4	-5	-1-4
4	+4	-4	-4
3	+1+2	-3	-1-2
2	+2	-2	-2
1	+1	-1	-1
0	0	0	0

The inverter operates in the staircase waveform generation mode, however it can also operates in PWM based switching scheme [19]. Furthermore, the inverter can partially work in PWM, which only applies PWM on 1Vpu H-bridge and staircase on 2Vpu and 4Vpu H-bridge, hence reducing the switching losses of the H-bridge fed by higher DC voltage. However, the dV/dt for the switching device may increase as well as the size of the filter if the output voltage waveform is pulse-width-modulated pulses [20, 21].

As the waveform of 15 voltage levels is close enough to the sinusoidal reference, the size of filer can be reduced largely.

Proposed staircase, partial PWM and PWM modulation scheme

To synthesize the 15-level output voltage waveform, the switching angles has been calculated in advance according to the switching pattern from the Table 1 for 3 H-bridge modules.

The modulation schemes for CMLI are mostly based on multiple-carrier arrangements with pulse-width modulation (PWM). Hence, in the traditional PWM scheme, the 15 voltage levels need 15 carrier signals which are arranged with vertical shifts or horizontal displacements. As a result, the high-order harmonic components generated by the PWM scheme can be easily attenuated by filter or load inductance, hence provide an output voltage with good reference tracking and low harmonic distortion. Hence, it also leads to high switching losses as the device switching frequency is usually quite high. As a result, the staircase modulation with low device switching frequency is introduced.

The staircase modulation scheme has all the switching angles of the 3 H-bridges calculated in advance and then stored in a table for digital implementation. However, the proposed staircase modulation scheme requires only one sinusoidal modulating wave which has been divided into 15 zones in magnitude. Each zone refers to one switching pattern which can generate the corresponding output voltage level, respectively. And by continuously sampling the sinusoidal modulating wave, the controller select the corresponding zone and voltage level as the current output voltage.

Figure 2 shows the stepped-voltage waveform consisted of the output of 3 H-bridge modules, where 4Vpu, 2Vpu and 1Vpu are the output voltages of them. The 3 H-bridge modules share the same switching angle from θ_1 to θ_{30} during the scheme. For example, the 2Vpu H-bridge shares the switching angle θ_2 with 1Vpu H-bridge, and all 3 H-bridge modules share θ_4 as their switching angle. Hence only one sinusoidal modulating wave for 1Vpu H-bridge module is needed, as the switching angles of 1Vpu H-bridge module include the other two modules' switching angle. The switching angles are chosen, aiming to adjust the output voltage and to reduce the harmonics [22-25].

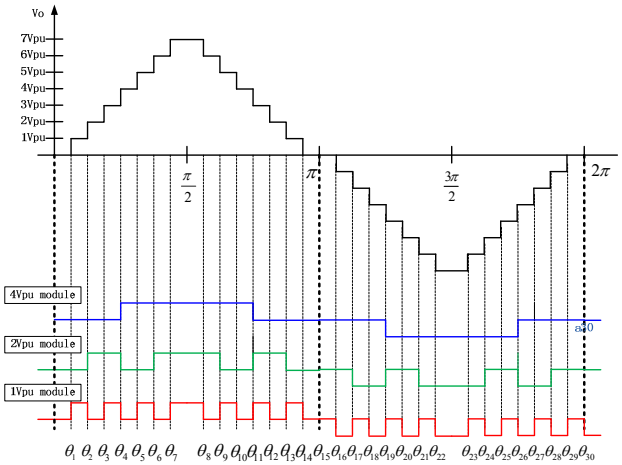

Fig.2. Stepped-voltage waveform consists of the output of 3 H-bridge module

The switching frequency of this circuit can be given by:

$$f\_switch = f\_fundamental \times 2\left(2^n - 1\right) \quad (1)$$

where the fundamental frequency is 50Hz, n represents the number of the particular H-bridge in per unit voltage order.

The device switching frequency of 4Vpu H-bridge module, 2Vpu H-bridge module and 1Vpu H-bridge module are 100Hz, 300 Hz and 700Hz respectively. The H-bridge with higher voltage output works at a lower switching frequency comparing to the H-bridge with lower voltage output, which reduces the switching losses largely. Hence, the high-voltage switching device with a low switching frequency can be applied on a higher voltage H-bridge such as 4Vpu module; while the low-voltage switching device with a high switching frequency can be applied on a lower voltage H-bridge such as 1Vpu module, which realizes the hybrid switching devices inverter. At the same time, the low switching frequency leads to low electromagnetic interference (EMI) [26].

The Fourier series expansion of the stepped-voltage shown in Figure 2 can by described by

(2) $$Vo(\omega t) = \sum_{n=1,3,5}^{\infty} \frac{4V_{dc}}{n\pi} \left(\sum_{p=1,2,3}^{m} (\cos(n\theta_p)) \sin(n\omega t) \right)$$

where n is the harmonic order, m is the maximum number of switching angles, and $m=7$ in this case. The coefficient $4V_{dc}/\pi$ represents the peak value of the maximum fundamental voltage, from which $V_{dc}=V_{pu}$.

The switching angles calculated in advance can be given by

(3) $$\theta_n = \arcsin \frac{(n-1)+k}{m+k}$$

where n is the number of the switching angles, m is the maximum number of switching angles, and k is a coefficient added to adjust the switching angle to track the sinusoidal modulating wave tighter, hence reducing the THD of the output voltage. Eq. (3) provides an adjustable modulation index, defined by

(4) $$M = \frac{V_1}{m \times \frac{4V_{dc}}{\pi}}$$

where V_1 is the peak value of the fundamental inverter output voltage, and m is the maximum number of switching angles.

The THD of the output voltage is defined as:

(5) $$THD = \frac{1}{V_1} \sqrt{\sum_{n=3,5,7}^{\infty} V_n^2}$$

where V_1 and V_n are both calculated according to Eq. (2), and the equations can be formulated to:

(6) $$V_1 = \frac{4V_{dc}}{\pi} (\cos(\theta_1)) + \cdots + \cos(\theta_7))$$

(7) $$V_n = \sum_{n=3,5,7}^{m} \frac{4V_{dc}}{n\pi} (\cos(n\theta_1)) + \cdots + \cos(n\theta_7))$$

The MathCAD (Mathsoft Engineering & Education, USA) calculates the THD as well as V_1 and V_n by applying Eq. (5), (6), and (7). Figure 3 shows the THD profile of the output voltage versus the coefficient k, and THD is 4.7% and 6.8% under the condition of $k=0.5$ and $k=0$, respectively. Hence the THD has been reduced by 2.1% by applying the additional coefficient k. Although both 4.7% and 6.8% for THD mean negligible small harmonics, and the 4.7% one which is less than 5% meets the requirement of the IEEE standards [27].

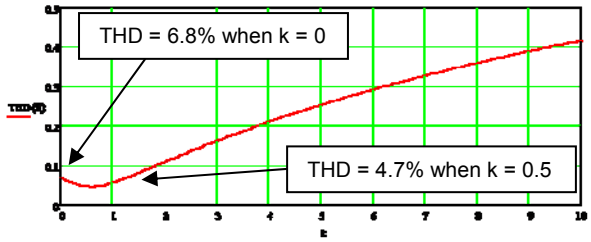

Fig.3. THD profile of the output voltage with 50th harmonics

Simulation Results

Simulation is performed in Saber (The Synopsys, Mountain View, California, USA) simulation platform. The system parameters are the following:

DC source voltage 1: 100V
DC source voltage 2: 50V
DC source voltage 3: 25V
Load resistor: 47Ω

1. Simulation with staircase modulation

The 3 H-bridge inverter is driven by the controller which generates the gate signal for 12 switches of the inverter. By comparing the sinusoidal modulating wave at a specific sampling rate (in this case 16 kHz), the switching pattern referring to the sampled value is determined according to Table 1 and Eq. (3) under the condition of $k=0.5$.

Figure 4 shows the simulation results of 15-level output voltage waveform with sinusoidal modulating wave. By tracking the reference sinusoidal wave, the amplitude of AC output voltage is $175V$. It can be observed that the AC output voltage follows the sinusoidal modulating wave quite well, which indicates the harmonics would be small.

The THD is also calculated and plotted in Figure 5, which shows the output voltage waveform with fast Fourier transform (FFT) analysis and implies that the THD is 5.425%. The sidebands include 3th, 5th, 21th, 23th, 27th, and 41th, 45th harmonics. Noticing the fact that the simulation circuit does not include any filter, the size of the filter for the proposed 15-level cascaded inverter can be reduced largely, as well as the filter losses.

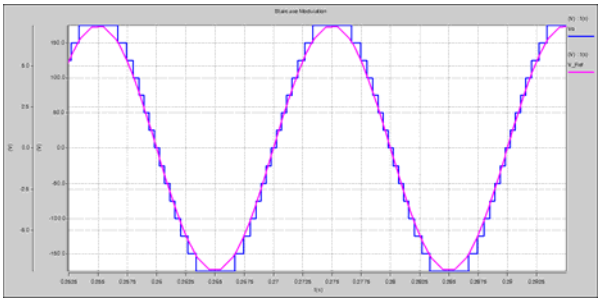

Fig.4. Simulation results of output voltage waveform with sinusoidal modulating wave for staircase modulation scheme

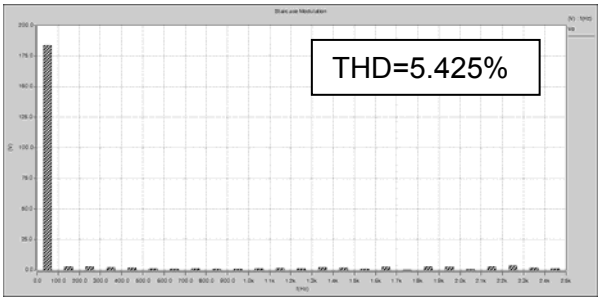

Fig.5. Simulation results of spectrum for 15-level output voltage waveform for staircase modulation scheme

As the THD calculated by MathCAD does not include even harmonics, hence it is smaller than the one calculated by Saber simulation software which includes both even and odd harmonics.

2. Simulation with PWM

To apply PWM on 15-level cascaded inverter, the PWM scheme in the simulation requires one sinusoidal modulating wave which has been divided into 15 zones in magnitude. Each zone between two different voltage levels refers to two switching patterns, respectively.

By continuously sampling the sinusoidal modulating wave and then select the corresponding zone, the controller selects two corresponding voltage levels as the current output voltage.

When the voltage of the sinusoidal modulating wave is found smaller than a voltage level (V_high) while bigger than another (V_lower) which is one level smaller, the CMLI will generate an output with V_high and V_low as high level and low level.

The duty-cycle time (on-state time) of the chosen switch during a sample period of the modulation scheme can be expressed as:

(8) $$T\_on = \frac{V\_ref - V\_low}{(V\_high - V\_low) \times f\_samp}$$

where the V_ref is the voltage of sinusoidal modulating wave, V_high and V_low are the top and bottom of the zone, f_samp is the sampling frequency.

Figure 6 shows that the CMLI generates two voltage levels as 75V and 50V, with duty-cycle time determined by the voltage of sinusoidal modulating wave. Hence the bigger V_ref is, the longer T_on is, vice versa.

Figure 7 shows the simulation results of 15-level output voltage waveform with sinusoidal modulating wave. Figure 8 shows the output voltage waveform with fast Fourier transform (FFT) analysis, which implies that the THD is 7.753%, with negligibly small low-order harmonics. The 16 kHz switching frequency states that the first significant harmonics will be 32 kHz; however only up to 25 kHz harmonics are considered.

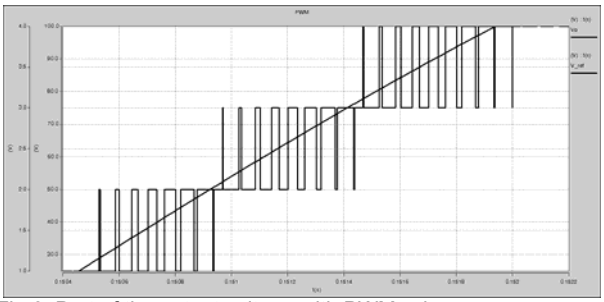

Fig.6. Part of the output voltage with PWM scheme

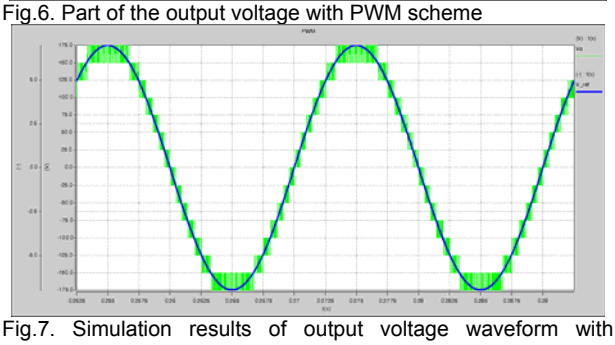

Fig.7. Simulation results of output voltage waveform with sinusoidal modulating wave for PWM scheme

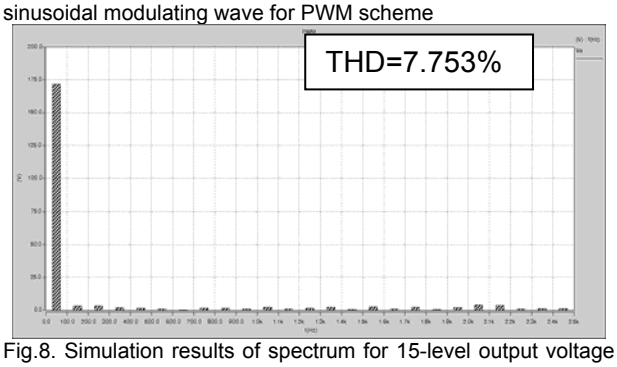

Fig.8. Simulation results of spectrum for 15-level output voltage waveform for PWM modulation

3. Simulation with partial PWM

To reduce the high switching losses caused by PWM scheme without increasing THD, the partial PWM scheme is applied on 15-level cascaded inverter. The switching frequencies of 4Vpu and 2Vpu modules are 100Hz and 300Hz respectively with staircase modulation, while the 1Vpu module is 16 kHz with PWM. Combined the staircase for 4Vpu and 2Vpu modules and PWM for 1Vpu, Figure 9 shows the simulation results of 15-level output voltage waveform with partial PWM scheme. Figure 10 shows the output voltage waveform with fast Fourier transform (FFT) analysis, which implies that the THD is 7.406%. The sidebands include 3th, 5th, 7th, 21th, 23th, 27th, and 41th, 45th harmonics.

By applying partial PWM scheme, the THD of output voltage decreases from 7.753% to 7.406%, and the switching losses of 4Vpu and 2Vpu modules are largely reduced.

The harmonics spectrums of the inverter output voltage with 3 different modulation methods are shown in Figure 11, where the Y-axis is the magnitude value of the nth-order harmonic voltage. To focus on the harmonics, the range of voltage is set to be 0V to 5V, and frequency is set to be 45 Hz to 2.5 kHz. It can be seen from Figure 11 that both staircase modulation and PWM scheme are with negligibly small even-order harmonics. Although the even-order harmonics of the PWM scheme are small, its THD is still higher than the THD of partial PWM scheme.

Table 2 gives a comparison among 3 modulation

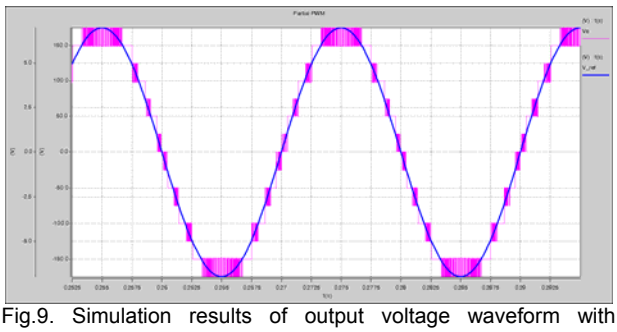

Fig.9. Simulation results of output voltage waveform with sinusoidal modulating wave for Partial PWM scheme

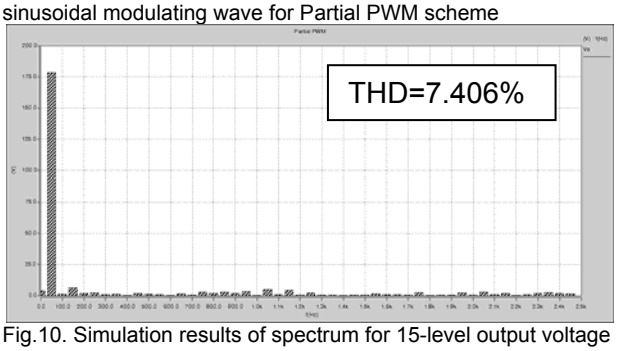

Fig.10. Simulation results of spectrum for 15-level output voltage waveform for Partial PWM modulation

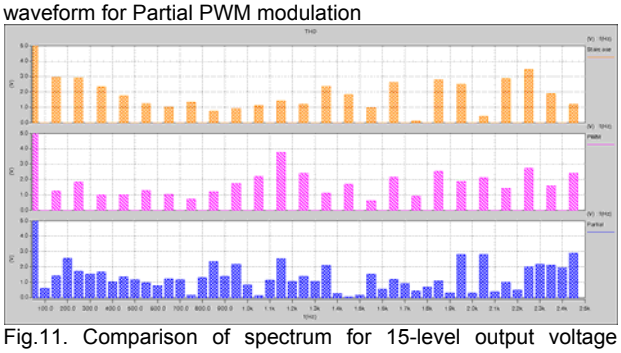

Fig.11. Comparison of spectrum for 15-level output voltage waveform for staircase, PWM and Partial PWM modulation

schemes, and it can be seen that even though the THD of staircase modulation is low, it still requires a big filter due to its big low-order harmonics. Meanwhile, the THD of PWM is high, however only a tiny size filter is needed due to its small low-order harmonics. To balance the 2 modulation schemes, partial PWM can be selected, with medium THD and lower-order harmonics.

Table 2. Comparison among the 3 modulation schemes

Modulation schemes	Switching losses	Low-order harmonics	THD
Staircase	Low	High	Low
PWM	High	Low	High
Partial PWM	Medium	Medium	Medium

Conclusion

A hybrid 15-level cascaded H-bridge inverter with staircase modulation, PWM and partial PWM is presented. The proposed topology and 3 modulation schemes result in near sinusoidal waveform. Based on simulation in Saber environment, a significant reduction of output voltage THD is obtained, and the 3 modulation schemes as well as their pros and cons based on THD, low-order harmonics and switching losses have been discussed in detail.

In the condition that no filter is considered, staircase modulation is with the lowest THD and switching losses, while PWM is with highest ones. The partial PWM combines those 2 modulation schemes and gives medium THD and switching losses. Each modulation scheme has its unique characteristic, hence fit for a specific application. Due to the results of the comparison, one may select the proper modulation scheme for specific application based on the requirement on THD, low-order harmonics (related to size of filter), efficiency and control complexity.

This technology can be implemented to conventional 7-level inverter easily and also extended to 3-phase inverter where the line-voltage will be 29 voltage levels.

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