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Modelling and Implementation of ZCS Buck Converter

Abstract. *A Current mode control of ZCS Interleaved Buck converter is presented. A robust PID controller is designed in order to achieve the stability of the converter. The pulse width modulation scheme is adopted to obtain the output voltage regulation. In order to improve the transitory response and dynamic constancy of the converter, the controller parameters are designed based on current mode control. The design is evaluated and verified using MATLAB/ Simulink. Experimental setup has been done to evaluate the controller platform using LabVIEW.*

Streszczenie. *W artykule przedstawiono metodę sterowania prądem dla przekształtnika obniżającego napięcie typu ZCS interleaved Buck z zastosowaniem modulacji PWM. W celu weryfikacji sterowania przeprowadzono badania symulacyjne w programie Matlab-Simulink, a także badania eksperymentalne z wykorzystaniem platformy LabVIEW. (**Modelowanie i implementacja przekształtnika obniżającego napięcie ZCS**).*

Keywords: Buck converter, Interleaved, LabVIEW, resonant component, Zero Current Switching
Słowa kluczowe: przekształtnik obniżający napięcie, interleaved, LabVIEW, składowa rezonansowa, ZCS.

Introduction

Switched mode dc-dc converters are the most efficient power electronic systems that convert an unregulated dc input voltage into a regulated dc output voltage. Switched mode power supplies when compared with the linear power supplies are smaller in size, much more efficient and have high power density. Therefore they are used extensively in personal computers, computer peripherals, communication, medical electronics and adapters of consumer electronic devices to provide different level of dc voltages. Among the basic topologies of dc-dc converters buck converters are widely used in portable consumer electronics. In general dc-dc converters are time variant, non linear dynamic systems. The non linear nature of the dc-dc converters arise mainly due to switching power devices, inductors and capacitors. One inherent disadvantage of buck converter is its reliance on large passive components. The increase in switching frequency reduces the size of components but it leads to various converter losses thereby reducing the efficiency when used particularly in light loads. In order to overcome these limitations soft switching methods are used [1].

The main challenge in the field of power electronics is accentuated more on designing the dc-dc converters with high power density, low Electromagnetic Interference (EMI) and low cost. Therefore it is a necessity that the operating frequencies of the dc-dc converters have to be increased in order to reduce the volume of transformers and filters especially in the case of isolated converters. To overcome these problems, soft switching circuits must be designed. Soft switching techniques such as zero voltage switching and zero current switching substantially reduce the switching losses resulting in higher efficiency. It may suppress the EMI and additional switching stress when compared against its hard switching counterpart [2]. It is also an essential one to implement the control circuits as simple as possible.

Many literatures are evolved presenting the analysis and behavior of the soft switched dc-dc converters. Some of them are discussed now. In [3] a soft switching PWM Interleaved two switch forward dc-dc converter is proposed. The features of the proposed converter includes (i) much reduced switching losses inspite of load variations (ii) lesser conduction losses due to low idling and circulating currents (iii) no auxiliary circuit is employed and (iv) the transformers are free of flux imbalances. This paper is well organized and shows very much improved results with higher efficiencies. But the closed loop control is not considered. The performance parameters of the dc-dc converter such as settling time, rise time and peak overshoot are not taken into account.

In [2], isolated dc-dc ZVS converter which is composed of two half bridge converters associated in series was presented. This paper mainly focuses the low frequency dynamics associated with the duty cycle variation. It proposes the use of faster controllers, thereby achieving some interesting results. But the inherent nature and subharmonic oscillations of the converters are not considered. The literature [4] presents interleaved ZVS converters combining two, two switch forward type converters with ripple current cancellation. Active snubber circuit is adopted and the voltage stresses are limited. Improved performances of the converters are evident. However due to the large count of switches complexity is high and it requires complex control and driving circuits.

The literature [5] proposes a new ZCS PWM commutation cell for the dc-dc converters. The conduction losses and current stress impaired on the main switch is minimized. Averaged model of the ZCS converter is developed and the highest efficiency is achieved. But no results have been produced for the evidence of improved dynamic performances and the transient behavior of the proposed converter. The non minimal phase behavior of the converter has not been considered. In general, almost in all the literatures it has been stated that the ZCS converters are preferred only for the applications in which the input current is high and in which the conduction losses dominate and can be effected through the IGBT's. But [6] proposes that the ZCS techniques can be used for converters with very low input voltages also. The proposed converter is more efficient and produces some desirable results.

In particular considering the assumption made in [6] and other literatures discussed above in this paper a closed loop current mode control of Interleaved ZCS Buck converter has been designed and analysed. This paper particularly deals with zero current switching which facilitates the following advantages: (i) Before the initiation of the next switching cycle the inductor current is zero inferring higher efficiency. (ii) Zero current switching always forces the inductor to begin its charging at zero current which limits the peak value of the inductor current to exactly twice the average current. This is quite desirable for both steady states and instantaneous switching cycle relationships [7].

In high power applications, it is often required to join together the converters in series or in parallel due to the unavailability of a single device to withstand the voltage stress or current stress. The advantages of connecting the converters in parallel called interleaving are:(i) input current ripple is reduced (ii) inductor size is reduced (iii) current rating of the semiconductors are reduced (iv) good current sharing among the converter modules (v) I^2R losses and inductor ac losses are reduced (vi) easier system maintenance and expansion (vii) increased system

reliability. The main challenge in the field of Power Electronics is emphasized more on the control aspects of the dc-dc converters. The control approach requires effective modeling and a thorough analysis of the converters.

The main objective of a control scheme is to make the system to track the desired reference input even in the presence of noise, modeling error and disturbances. In control system, controller plays a vital role by generating appropriate control signal for the system to regulate the performance. Inspite of the advancements in process control techniques, PID (Proportional – Integral – Derivative) controller is still popular in closed loop control. In most of the industries PID controllers are widely used due to their simplicity, applicability, low power consumption and ease of implementation. A simple Ziegler-Nichols tuning rule is one of the most popular methods of tuning to obtain reasonable good initial setting of PID controllers because of familiarity and ease of use [8].

The design of feedback compensator requires a dynamic model of the switching converter. In order that the transient analysis and control design are easy a number of equations must be solved in a sequence. This problem can easily be solved by arriving at a single equation describing the converter approximately over a number of switching cycles using state space averaging technique. The zero current switching (zcs) interleaved Buck converter with PID controller has been designed, modeled and simulated using MATLAB/Simulink. The main objective is to implement this control scheme to the converter which describes its operation, implementation, simulation performance and also to study the performance of the converter with source and load variations. Prototype of the Buck converter has been developed to evaluate the controller platform using LabVIEW.

Design of Interleaved Buck Converter

The switches of the zero current switching (ZCS) Buck converter turn on and off at zero current. The circuit shown in the fig.1 consists of the inductor connected in series with the switch to achieve ZCS. This type of connection is called as L type connection which is advantageous than the other type of connection called the M type. In M type of connection an amount of energy is trapped in the inductor due to the recovery times of the practical devices. This results in the voltage transients across the switch. This condition favors the L type over M type.

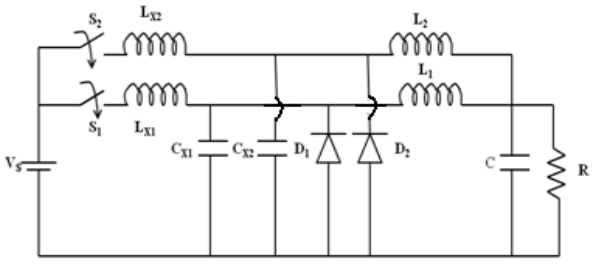

Fig.1. Schematic diagram of ZCS Interleaved Buck Converter

The ZCS Interleaved Buck Converter comprises of the resonant component inductors L_{X1}, L_{X2} and capacitors C_{X1} and C_{X2}, inductors L_1 and L_2, a capacitor C, two semiconductor switches, two diodes D_1 and D_2 and a load resistor R.The resonant components can be determined as follows:

The ratio between the peak resonant current and the load current is given by the following equation,

$$x = \frac{I_m}{I_o} = \frac{V_S}{I_o}\sqrt{\frac{C_x}{L_x}} \tag{1}$$

The value of inductor L_X and the capacitor C_X are determined by,

$$T = \frac{\pi V_S}{X I_o} C_x + \frac{2V_S}{I_o} C_x \tag{2}$$

and

$$L_x = \left(\frac{V_S}{x I_o}\right)^2 C_x \tag{3}$$

The following are the parameters considered for design:
V_S = 48V, V_O = 12V, f_S = 50kHz, P_O = 100W,I_O = 8.33A,
R = 1.44Ω, $L_1 = L_2$ =2.16x10^{-4}, C = 1.736x10^{-5}, $L_{X1} = L_{X2}$ = 5.89μH , $C_{X1} = C_{X2}$= 7.584μF.

Modeling of ZCS Buck Converter

The ZCS interleaved buck converter is modeled using state space averaging technique in which the design is carried out in time domain based on their performance indices. Therefore the converter specifications are very well met. This method is highly significant for this kind of converters since the PWM converters are the special type of non linear systems which is switched in between two or more non linear circuits depending upon the duty ratio [9].The unique feature of this method is that the design can be carried out for a class of inputs such as impulse, step or sinusoidal function in which the initial conditions are also incorporated.

As a general case state space averaging method for two switched basic PWM converters is discussed now. The inductance currents and capacitance voltages are state variables and matrix form of equation is mentioned below,

$$\dot{X} = A_1 x + B_1 u \tag{4}$$

$$\dot{X} = A_2 x + B_2 u \tag{5}$$

where x is a state variable vector, u is a source vector, A_1, B_1, A_2, B_2 are the system matrices respectively. The significance of state space averaging technique lies in replacing the above two sets of state equations by a single equivalent set described as follows,

$$\dot{X} = Ax + Bu \tag{6}$$

The A and B matrices are the weighted averages of actual matrices describing the switched system given by the following equations,

$$A \equiv dA_1 + (1-d)A_2 \tag{7}$$

$$B \equiv dB_1 + (1-d)B_2 \tag{8}$$

where d is the duty cycle ratio. Based on the above discussion, state model of Interleaved Boost converter is derived and is discussed now. Mode of operation is assumed as continuous conduction since higher power densities are possible only with this mode of operation. During this mode D_1 and D_2 are always in complementary state with the switches S_1 and S_2 respectively that is when S_1 is on, D_1 is off and vice versa. Similarly when S_2 is on, D_2 is off and vice versa. Accordingly four modes of switching states are possible and the corresponding state equations are arrived as follows:

Mode1: S_1 and S_2 are on

$$\dot{X} = A_1 x + B_1 V_S \tag{9}$$

$$x = \begin{bmatrix} i_1 \\ i_2 \\ i_{Lx1} \\ i_{Lx2} \\ V_{Cx1} \\ V_{Cx2} \\ V_C \end{bmatrix} \tag{10}$$

where i_1 and i_2 are currents flowing through the inductances L_1 and L_2, i_{LX1} and i_{LX2} are the currents flowing through the resonant inductances L_{X1} and L_{X2},V_{X1} and V_{X2} are the

voltages across the resonant capacitances and V_C is the capacitance voltage respectively.

Mode 2: S_1 is on and S_2 is off

(11) $$\dot{X} = A_2 x + B_2 V_S$$

Mode 3: S_1 is off and S_2 is on

(12) $$\dot{X} = A_3 x + B_3 V_S$$

Mode 4: S_1 and S_2 are off

(13) $$\dot{X} = A_4 x + B_4 V_S$$

where,

(14) $$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{1}{L_1} & 0 & \frac{-1}{L_1} \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{L_2} & \frac{-1}{L_2} \\ 0 & 0 & 0 & 0 & \frac{-1}{L_{x1}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_{x2}} & 0 \\ \frac{-1}{C_{x1}} & 0 & \frac{1}{C_{x1}} & 0 & 0 & 0 & 0 \\ 0 & \frac{-1}{C_{x2}} & 0 & \frac{1}{C_{x2}} & 0 & 0 & 0 \\ \frac{1}{C} & \frac{1}{C} & 0 & 0 & 0 & 0 & \frac{-1}{RC} \end{bmatrix}$$

(15) $$A_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{1}{L_1} & 0 & \frac{-1}{L_1} \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_2} \\ 0 & 0 & 0 & 0 & \frac{-1}{L_{x1}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{L_{x2}} & 0 \\ \frac{-1}{C_{x1}} & 0 & \frac{1}{C_{x1}} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C} & \frac{1}{C} & 0 & 0 & 0 & 0 & \frac{-1}{RC} \end{bmatrix}$$

(16) $$A_3 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_{x1}} \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{L_2} & \frac{-1}{L_2} \\ 0 & 0 & 0 & 0 & \frac{-1}{L_{x1}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_{x2}} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{-1}{C_{x2}} & 0 & \frac{1}{C_{x2}} & 0 & 0 & 0 \\ \frac{1}{C} & \frac{1}{C} & 0 & 0 & 0 & 0 & \frac{-1}{RC} \end{bmatrix}$$

(17) $$A_4 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_1} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{L_{x1}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-1}{L_{x2}} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C} & \frac{1}{C} & 0 & 0 & 0 & 0 & \frac{-1}{RC} \end{bmatrix}$$

(18) $$B_1 = B_2 = B_3 = B_4 = \begin{bmatrix} 0 \\ 0 \\ \frac{1}{L_{x1}} \\ \frac{1}{L_{x2}} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

The average state model takes the form described as follows:

(19) $$\dot{X} = [A][X] + [B][U]$$

where $[A] = A_1 d_1 + A_2 d_2 + A_3 d_3 + A_4 d_4$, $[B] = B_1 d_1 + B_2 d_2 + B_3 d_3 + B_4 d_4$, $[U] = V_S$ and the duty cycle ratio is given by $d_1 + d_2 + d_3 + d_4 = 1$.The output equation is defined as follows,

(20) $$y = [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1] \begin{bmatrix} i_1 \\ i_2 \\ i_{Lx1} \\ i_{Lx2} \\ V_{Cx1} \\ V_{Cx2} \\ V_C \end{bmatrix}$$

Design of Robust PID Controller

The ideal continuous time PID controller can be expressed as,

(21) $$u(t) = k_p \left[e(t) + \frac{1}{T_i} \int_0^t e(t)dt + T_d \frac{d}{dt} e(t) \right]$$

Where u(t) is the control output, k_p is constant coefficient of the proportional gain, T_i is the integral time, T_d is the derivative time and e(t) is the error between the Vref and Vo. The transfer function corresponding to the PID controller is given as,

(22) $$u(s) = \left[k_p + \frac{k_i}{s} + k_d s \right] e(s)$$

Where k_p , $k_i = \frac{k_p}{T_i}$ and $k_d = k_p T_d$ are the proportional, integral and derivative gains of the controller respectively [8]. K_p, T_i and T_d are calculated according to Ziegler – Nichols tuning rules. This method is an accurate heuristic method for determining good settings of PID controllers. This method is based on the empirical knowledge of the ultimate critical gain P_{cr}, which is given by $2\pi/\omega$, where ω is the natural frequency of oscillation of the converter under consideration. The Ziegler – Nichols tuning formulae is illustrated in the Table 1.

Table 1. Ziegler – Nichols tuning rules for PID Controller design

Sl.No	Parameters	Formulae
1	Proportional gain(k_p)	0.6 P_{cr}
2	Integral Time (T_i)	0.5 P_{cr}
3	Derivative Time (T_d)	0.125 P_{cr}

P_{cr} value is obtained by the careful evaluation of the converter by assuming appropriate natural frequency of oscillation. The k_p value thus obtained is properly tuned in order that the system tracks the required step response. The main objective in tuning the controller is to choose the parameters in such a way that the control signal generates the accurate duty cycle command for the regulation of the dc-dc converter under consideration, irrespective of the source voltage or load disturbance. Hence it presents the faster dynamic response which is evident from the simulation results. The k_P, k_I and k_D values thus designed for the converter stages are k_P = 0.33, k_I = 17.89X10^3 and k_D =1.522X10^{-}6.

Simulation Results

The ZCS Interleaved Buck Converter with PID Controller is designed and simulated using MATLAB/Simulink. The design is carried out in time domain and hence the converter specifications such as rise time, settling time, peak overshoot and steady state error are achieved as per the Industrial standards and is illustrated in Table.2. The simulation has been carried out for variable voltage source and variable load not limiting to R load, which is illustrated in Table 3.The simulation results for the output current i_o,

inductor currents i_1 and i_2, output Voltage Vo with PID Controller for zcs interleaved Buck converter is shown in fig.2.

Table 2. Performance Parameters for the Converter

Sl.No	Parameters	Values
1	Rise Time(s)	0.012
2	Settling Time(s)	0.014
3	Peak Overshoot (%)	0
4	Steady State Error(V)	0.02

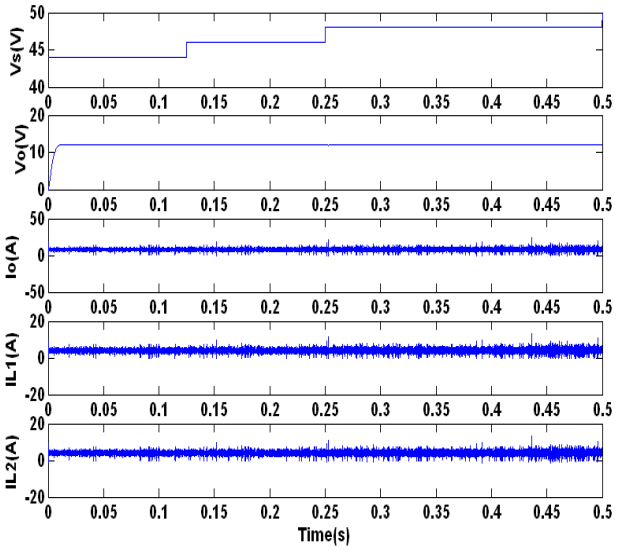

Fig. 2. Simulation results for ZCS Interleaved Buck Converter(V_S-Input Voltage, V_O-Outpur Voltage, I_O-Load Current, I_{L1} and I_{L2} – Inductor Currents)

It is obviously understood from the simulation results that for the input transients of 44V-46V-48V, the output voltage is maintained constant, which is considered as 12V.The output voltage settles down much faster and hence the dynamic performance of the converter is improved. No undershoots and overshoots are evident. The output voltage ripple is almost negligible. It is understood from fig.2 that the two inductors L_1 and L_2 share the current equally and hence good current sharing is being achieved which is one of the major advantages in designing the controller. The simulation results reveal the fact that the PID controller is the robust one in which the results are in concurrent with the mathematical calculations. The converter is designed in time domain and hence the converter specifications are very well met. The output current contains some ripple which is evident from fig.2 needs some improvement.

Table 3. Output Voltage for Load Variations

Sl.No	R(Ω)	L(H)	E(V)	Reference Voltage (V)	Output Voltage (V)
1	1.44	-	-	12	12.01
2	2	-	-	12	12.03
3	5	-	-	12	12.01
4	1.44	$10X10^{-6}$	-	12	12.01
5	2	$100X10^{-6}$	-	12	12.01
6	5	$100X10^{-6}$	5	12	12.03

The efficiency of the ordinary Buck Converter, Interleaved Buck converter and ZCS Interleaved Buck Converter are determined and are shown against the load current in fig.3. The efficiency of the interleaved state is slightly lesser than the ordinary Buck converter where as the efficiency of the Interleaved converter with zero current switching is much improved. It is almost same and even high at some load currents when compared with the ordinary Buck converter stage. The highest efficiency is obtained as 98% with a load current of 1.41A.

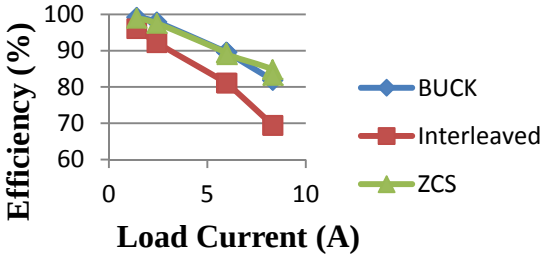

Fig. 3. Comparison of Efficiencies

In order to prove that the controller is robust and efficient enough in tracking the reference votages irrespective of the input voltage variations and disturbances the output voltage for the references of 5V and 8V are shown with respective input voltage variations of 10V, 12V and 14V in fig.4. In this figure green line represents the set value and the blue line represents the actual output voltage.

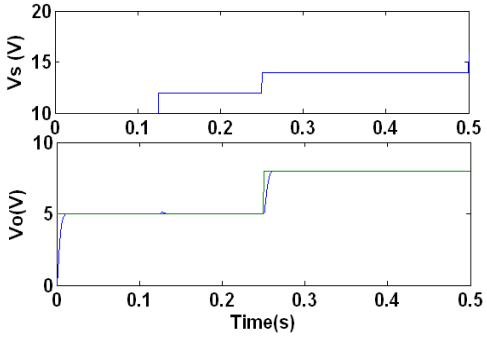

Fig. 4. Output Response of the ZCS interleaved Buck converter

Hardware Implementation

LabVIEW Package: The ZCS Interleaved Buck converter with PID Controller has been implemented using LabVIEW as a controller platform. LabVIEW (Laboratory Virtual Instrumentation Engineering Work Bench) is a system design platform and development environment for a visual programming language from National Instruments. It is a widely used software to implement the projects with a shorter duration due to its programming flexibility combined with built in tools designed especially for testing, measurements and control. The key feature of LabVIEW is that it extensively supports accessing the instrumentation hardware. It is provided with drivers and abstraction layers for almost all types of instruments. The buses are also available for inclusion. The abstraction layers and drivers act as graphical nodes and enable to communicate effectively with the hardware devices thereby offering standard software interfaces [10].

Interfacing Circuit: The NI DAQ Pad-6009 multifunction data acquisition (DAQ) devices provide plug and play connectivity via USB for acquiring, generating and data logging in a variety of portable applications. It comprises of 8 analog inputs with referenced single ended signal coupling or 4 inputs with differential coupling, 2 analog outputs, 12 bits A/D and D/A converters and 32 bits counters. There are 12 channels of digital Input/output lines which can be used either as input or output. It eventually provides an excellent platform for the PID controller. The prototype model of the Buck converter with PID controller is shown in fig.5. To evaluate the performance, the reference values of 5V and 8V are set for which the output is obtained

as 5.04 V and 7.98 V respectively. The steady state error thus observed is very minimum to the order of 0.04V and the system settles down fast. The acquisition of the error signal from the hardware takes place instantaneous as and when the program is run and at the same time the controlled signal from the LabVIEW package is also generated within a very shorter duration of time without any delay or time lag. The experimental results thus obtained are in concurrence with the simulation results and mathematical calculations.

Table 4. Efficiency for the converters

Sl.No	I_O(A)	P_O(W)	Buck Converter			Interleaved Buck Converter			ZCS Interleaved Buck Converter		
			Losses(W)	P_{in}(W)	η (%)	Losses(W)	P_{in}(W)	η (%)	Losses(W)	P_{in}(W)	η (%)
1	1.408	16.89	0.1345	17.0545	99.21	0.6875	17.58	96.11	0.1758	17.07	98.98
2	2.435	29.22	0.6150	29.835	97.94	2.4700	31.69	92.22	0.7369	29.96	97.54
3	5.968	71.62	8.2700	79.89	89.65	16.6254	88.25	81.16	8.4470	80.07	89.45
4	5.997	71.96	8.3880	80.348	89.56	16.7809	88.74	81.09	8.9940	80.95	88.89
5	8.317	99.80	22.0550	121.855	81.90	43.7970	143.59	69.50	17.8100	117.61	84.86
6	8.330	99.96	22.1509	122.111	81.86	44.0950	144.06	69.39	20.1410	120.101	83.23

Fig.5. Experimental set up

Conclusion

A closed loop control system has been designed for the ZCS Interleaved Buck converter in continuous time domain using robust PID controller. The simulation results thus obtained using MATLAB/Simulink is in agreement with the mathematical calculations. The controller thus designed for the converter is implemented using LabVIEW as a control platform and the results are illustrated. The mathematical analysis, simulation study and the experimental study show that the ZCS interleaved buck converter with PID controller thus designed achieves tight output voltage regulation and good dynamic performances and higher efficiency of the order of 98%. The soft switching thus implemented reduces the switching stress and losses and hence leading to the highest efficiency of 98% with a load current of 1.41A. The controller enables good current sharing among the parallel connected Buck converters. This method is topology independent and also can be extended for any of the applications such as power factor preregulation, photovoltaic cell and speed control applications. The prototype developed is more suitable for portable electronic systems and more effective and easy to be implemented.

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