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A Three-level Inverter Neutral Voltage Balancing Control Method

Abstract: *Owe to three-level inverter mature topological structure and low harmonic content of output voltage, it has been applied widely in large power and high voltage applications, but three-level topological structure leads to an inherent problem that is the neutral potential imbalance. This paper analyses the intrinsic causes in neutral voltage imbalance and presents the voltage balance method based on a hysteresis loop control. According to the different combinations of load current direction, the method controls two-capacitor voltage dynamically by adjusting the small redundant vectors and fully considering the effect of medium vectors on the neutral point potential balance. The paper analyses the switching states choice, the order of switch sequence and allocation of time in detail when the reference voltage vector falls into small triangle having one or two redundant small vector. Simulation and experimental results show that the control method can achieve a good neutral point voltage balance.*

Streszczenie. *W artykule przedstawiono analizę zagadnienia regulacji napięcia punktu neutralnego w przekształtniku trójpoziomowym. Opracowana metoda regulowania napięć na kondensatorach DC-link bazuje na regulatorze histerezowym i znakach prądów fazowych. Odpowiedź regulatora decyduje o doborze odpowiednich stanów łączników (wektory krótkie). Wyniki symulacyjne i eksperymentalne potwierdzają skuteczność algorytmu.* (***Algorytm regulacji napięcia punktu neutralnego w falowniku trójpoziomowym***).

Key words: *neutral potential imbalance; hysteresis control; neutral point voltage control; current direction*
Słowa kluczowe: potencjał punktu neutralnego, nierówność napięć, sterowanie histerezowe, kontrola napięcia punktu neutralnego, kierunek prądu.

Introduction

For the topological structure of three-level inverter is considerable mature, and the harmonic content is very low, it gains widely uses in high-voltage high-power applications. In respect to two-level inverter, three-level inverter has following advantages: if the DC bus voltage is a constant value, the withstand voltage degree of switching devices may be reduced by half; in case of the same switching frequency, the harmonic content of output voltage of three-level inverter may lower 50%; when using switching devices with same power grade, the output power may be doubled. However, the topological structure of three-level inverter brings an inherent problem, which is known as unbalanced neutral potential [2]. Aiming at the inherent problem of unbalanced neutral potential of three-level inverter, this paper analyzed the root reasons for the unbalanced capacitor voltage, and then proposed a control method for voltage balance based on hysteresis control technology. The selection of function sequence of neutral potential balancing and switching over are both considered in this paper, while the selection of switching sequence and the distribution of acting time are discussed detailedly within following two aspects: one is the reference voltage vector falls into Area C, where has two kind of redundant switching state with small vectors; the other one is Area B, where has only one redundant switching state with small vectors. For the balancing control of capacitor voltage of three-level inverter, related results prove that this method could achieve a considerable good effect.

Basic Principle of Three-level Inverter

Fig.1 is the topological structure of a three-phase three-level inverter. Take Phase A as an example, when switch tube A1 and A2 are turned on, and A3 and A4 are turned off at the same time, $U_{ao}=\frac{U_{dc}}{2}$, when expressed as State 1; when switch tube A2 and A3 are turned on, and A1 and A4 are turned off at the same time, $U_{ao}=0$, when expressed as State 0; when switch tube A3 and A4 are turned on, and A1 and A2 are turned off, $U_{ao}=-\frac{U_{dc}}{2}$, when expressed as State -1.Define the switch state of three-level inverter as $S_i(i=a,b,c)$:

$$S_i=\begin{cases}1, & \text{the upper two switch tubes of the } i^{th} \text{ phase are turned on}\\ 0, & \text{the middle two switch tubes of the } i^{th} \text{ phase are turned on}\\ -1, & \text{the lower two switch tubes of the } i^{th} \text{ phase are turned on}\end{cases}$$

The phase voltage output by each phase may be expressed by switching functions as follows:

$$U_{io}=S_i\cdot\frac{U_{dc}}{2},\ \text{where } (i=a,b,c) \tag{1}$$

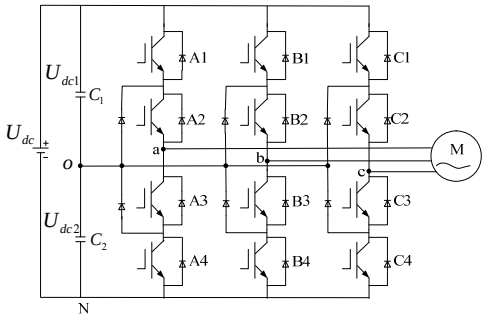

Fig.1 Three-phase three-level inverter topological structure

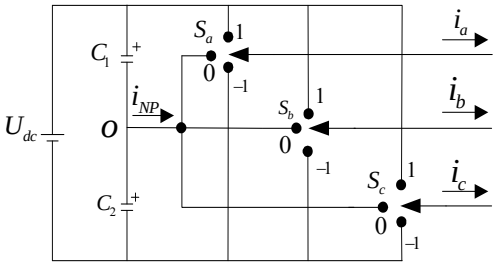

Fig.2 Switch model of three-level circuit

The switching model of three-level circuit established by formula (1) is shown as Fig.2 [3].

The Park transformation of three-level inverter is:

(2) $$\overline{U_s}=\frac{2}{3}(U_{ao}+\alpha\cdot U_{bo}+\alpha^2\cdot U_{ao})$$

where $\overline{U_s}$ - the voltage space vector, $\alpha=e^{j\frac{2\pi}{3}}$.

According to formula (1), formula (2) may be expressed as:

(3) $$\overline{U_s}=\frac{U_{dc}}{2}(S_a+\alpha\cdot S_b+\alpha^2\cdot S_c)$$

According to different switching combinations of (S_a,S_b,S_c), the output of three-phase three-level inverter may have 3^3=27 states as per formula (3), within which there are 19 effective voltage vectors after removing redundant ones. Based on the amplitude and phase, the space voltage vector diagram of three-phase three-level inverter may be schemed as Fig. 3.

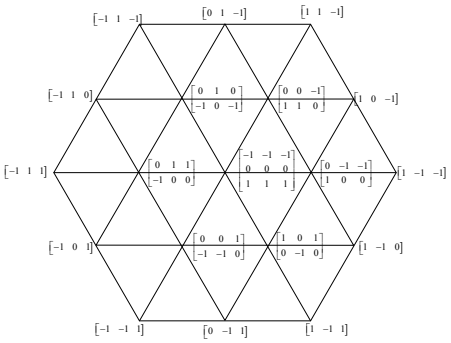

Fig.3 Distribution of space vector sector

For Fig.3, vectors with module length equal to U_{dc} are called for large vectors, such as [1 –1 –1]; vectors with module length equal to $\frac{\sqrt{3}U_{dc}}{2}$ are middle vectors, such as [1 0 –1]; vectors with module length equal to $\frac{U_{dc}}{2}$ are small vectors, such as [1 0 0]; vectors with module length equal to 0 are zero vectors, such as [1 1 1]. They divided the regular hexagon into 6 large triangle areas equally, and then each large triangle area is divided into 4 small triangle areas.

Control Method for Neutral Potential Balancing of Three-level Inverter

As shown in Fig.2, the direction of currents within motor winding is prescribed as follows: current flows from inverter to motor is a positive current, or else is a negative current; current extract from the neutral potential is a positive current, while inject current is a negative current. Within the 27 voltage vectors, only 18 vectors' switch states may affect the neutral potential current i_{NP}, the value of such neutral potential current flow in (or flow out) at any time functioned by these 18 vectors should be equal to a certain phase current $i_x(x=a,b,c)$. If the direction of i_x is determined, for small vectors with redundant states, within switch states mentioned above, there are three possible cases explained as follows: if this phase is connected with the neutral potential on DC side directly, that is to say define the small vector do not change the current output direction as positive small vector, the neutral current is $i_{NP}=i_x$; if this phase is not connected with the neutral potential directly, namely define the small vector changes the current output direction as negative small vector, the neutral current is $i_{NP}=-i_x$; if the middle vector is functioning at that time, the neutral current is $i_{NP}=i_x$, where related corresponding relationships are shown in Table 1.

Table 1 Different switch state of the corresponding neutral current i_{NP}

Small vector	i_{NP}	*Small vector*	i_{NP}	*Middle vector*	i_{NP}
0-1-1	i_a	100	$-i_a$	01-1	i_a
-10-1	i_b	010	$-i_b$	10-1	i_b
-1-10	i_c	001	$-i_c$	1-10	i_c
011	i_a	-100	$-i_a$	0-11	i_a
101	i_b	0-10	$-i_b$	-101	i_b
110	i_c	00-1	$-i_c$	-110	i_c

In Fig.2, the current relationship equation of node o on the DC side may be obtained according to KCL law:

(4) $$i_{NP}=S_a\cdot i_a+S_b\cdot i_b+S_c\cdot i_c$$

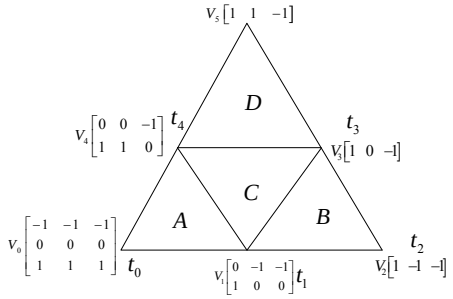

Fig.4 The first sector voltage vector

For various sections on the SVPWM coordinate plane are symmetric, analyze one sector for the balance of neutral potential voltage is enough. Take the first sector as an example, as shown in Fig.4, in the process of linear modulation, the small triangle with space voltage vectors fallen in may be reduced to two situations: one is Area C, with two kinds of redundant small vectors, while the other one is Area B, with one kind of redundant small vector. In both cases, the selection principle, according to the condition of current affecting the balance of capacitor voltage, may be described detailedly as follows.

(1) *Reference vector falls in Area C of the triangle*

If $U_{dc1}-U_{dc2}>h$ (h is the hysteresis width), to control $U_{dc1}-U_{dc2}\le h$, capacitor C_2 should be charged, while C_1 discharged. From Fig.4 we can see that: currents may affect the neutral voltage within Area C are i_a,i_b,i_c, generated by small vector V_1, middle vector V_3 and small vector V_4 respectively. Let d_1,d_3,d_4 are duty ratios corresponding with acting time t_1,t_3,t_4 of vectors V_1,V_3,V_4 within one switch period respectively. For V_4, the acting time of [1 1 0]、[0 0 –1] are $\frac{(1+k_4)}{2}d_4\cdot T_s$ and $\frac{(1-k_4)}{2}d_4\cdot T_s$ respectively; for V_3, the acting time of [1 0 –1] is $d_3\cdot T_s$; for V_1, the acting time of [0 –1 –1]、[1 0 0] are $\frac{(1+k_1)}{2}d_1\cdot T_s$ and $\frac{(1-k_1)}{2}d_1\cdot T_s$ respectively. In this way, the neutral current may be expressed as:

(5) $$\begin{aligned}i_{NP}&=d_3\cdot i_b+\frac{(1+k_1)}{2}d_1\cdot i_a-\frac{(1-k_1)}{2}d_1\cdot i_a\\&+\frac{(1+k_4)}{2}d_4\cdot i_c-\frac{(1-k_4)}{2}d_4\cdot i_c\\&=d_3\cdot i_b+k_1\cdot d_1\cdot i_a+k_4\cdot d_4\cdot i_c\end{aligned}$$

Form formula (5) we can see that: current generated by middle vector V_3 has no redundant state, it is a uncontrolled value, the balancing control only depends on the selection of small i_a and i_c. To simplify the switch sequence, the general concept of neutral balancing control should be based on the basic principle expressed as the switch state should not be changed abruptly. Within each switch period, the balance control of neutral potential voltage should be implemented by selecting i_a or i_c. Considering with the direction of i_a and i_c, the specific analyze process may be described as follows:

1) when $i_a \geq 0$, to ensure the injection of neutral current, select vector with neutral current $i_{NP} = -i_a$, namely select [1 0 0] to ensure $|U_{dc1} - U_{dc2}| \leq h$, here $k_1 = -1$.For the acting time of redundant small vector controlling i_c are same, namely $k_4 = 0$. In this case, the effect of i_c to the neutral potential voltage within one period will be balanced automatically, the direction of i_c may be ignored. According to formula (5), here $i_{NP} = d_3 i_b - d_1 i_a$.

2) When $i_a < 0$, to ensure the injection of neutral current, select vector with neutral current $i_{NP} = i_a$, namely select [0 -1 -1] to ensure $|U_{dc1} - U_{dc2}| \leq h$. In this case, the switch sequence should be started with start vectors such as [1 1 0] or [0 0 –1]. If we set [1 1 0] as the start vector, then 110 → 10–1 or 110 → 0–1–1, the former has two phases switch state changed at the same time, the latter has three phases switch state changed at the same time, thus [1 1 0] should not be used as a start vector; if we set [0 0 –1] as the start vector, then 00–1 → 10–1 → 0–1–1 or 00 –1 → 0–1–1 → 10 –1, both of the sequence selection method have two phases switch state changed at the same time, thus [0 0–1] should not be used as a start vector also. In this case, i_c is the unique choice for controlling the balance of neutral potential voltage. When $i_c \geq 0$, to ensure the injection of neutral current, select [0 0 –1] to ensure $|U_{dc1} - U_{dc2}| \leq h$, here $k_4 = -1$, $i_{NP} = -i_c$. Control the acting time of redundant small vector of i_a equal with each other, namely $k_1 = 0$. In this case, effect on neutral potential voltage within one switch period of i_a will be eliminated mutually. According to formula (5), here $i_{NP} = d_3 i_b - d_4 i_c$. If $i_c < 0$, to ensure the injection of neutral current, select vector [1 1 0], here $i_{NP} = i_c$, when the balance control of neutral potential voltage depends on i_c.In this case, the switch sequence should be started with start vectors such as [0–1–1] or [1 0 0]. If we set [0–1–1] as the start vector, then 0–1–1 → 10–1 or 0–1–1 → 110, the former has two phases switch state changed at the same time, the latter has three phases switch state changed at the same time, thus [0–1–1] should not be used as a start vector; if we set [1 0 0] as the start vector, then 100 → 10–1 → 110 or 100 → 110 → 10–1, both of the sequence selection method have two phases switch state changed at the same time, thus [0 0–1] should not be used as a start vector also. Therefore, for $i_a < 0$ and $i_c < 0$, only when i_a and i_c cooperate together, the balance control of neutral potential voltage could be realized, which even satisfy the principle of switch state is kept without abrupt changes. When $i_a < 0$ and $i_c < 0$, let the acting time of redundant switch vector [1 0 0] and [0 –1 –1] of space vector V_1 equal, namely $k_1 = 0$, and then change the value of k_4 to adjust the acting time $\frac{(1+k_4)}{2} d_4 \cdot T_s$ of [0 0 –1] and that of $\frac{(1+k_4)}{2} d_4 \cdot T_s$ (the numeric area of k_4 is –1～1) of [1 1 0] to control the balance of neutral potential voltage (or set the acting time of redundant switch vectors [1 1 0] and [0 0 –1] of space vector equal, and then adjust the acting time of redundant switch vectors [0 –1 –1] and [1 0 0] of space vector V_1 to control the balance of neutral potential voltage). The analysis method of the case of $U_{dc1} - U_{dc2} < -h$ is similar to that described above.

(2) *Reference vector falls in Area B of the triangle (reference vector falls in Area D is similar to that of Area B)*

When falls in Area B, for large vector V_2, the acting time is $d_2 \cdot T_s$, having no effect on the neutral current. According to formula (5), here $i_{NP} = d_3 \cdot i_b + d_1 \cdot i_a$.Therefore, the balance control of neutral potential voltage should be realized depending on i_a only. If $U_{dc1} - U_{dc2} > h$, when $i_a \geq 0$, select [1 0 0] to ensure $|U_{dc1} - U_{dc2}| \leq h$. If $i_a < 0$, [0 -1 -1] may be selected to ensure $|U_{dc1} - U_{dc2}| \leq h$. The analysis method of the case of $U_{dc1} - U_{dc2} < -h$ is similar to that described above. In summary, the overall switch sequence and the acting time within the first sector are shown in Table 2.

Simulation and experiment results

To verify the correctness of control strategy introduced above, simulation researches related to the balance method for neutral potential voltage proposed in this paper are conducted through MATLAB/SIMULINK. Meanwhile, corresponding experimental verifications of the control method are conducted based on the experimental platform mainly composed of the three-level high-power inverter developed. The experimental system diagram is shown in Fig.5.

Table 2 Pulse sequence and timing table

Sector	*Voltage relationship*	*Case*	*Current relationship*	*Arrangements of time and sequences*							
Area C of triangle	$U_{dc1}-U_{dc2}>h$	1	$i_a \geq 0$ $i_c \geq 0$		00-1 t4/4	10-1 t3/2	100 t1/2	110 t4/2	100 t1/2	10-1 t3/2	00-1 t4/4	
		2	$i_a \geq 0$ $i_c < 0$		00-1 t4/4	10-1 t3/2	100 t1/2	110 t4/2	100 t1/2	10-1 t3/2	00-1 t4/4	
		3	$i_a < 0$ $i_c \geq 0$		100 t1/4	10-1 t3/2	00-1 t4/2	0-1-1 t1/2	00-1 t4/2	10-1 t3/2	100 t1/4	
		4	$i_a < 0$ $i_c < 0$	110 (1+k4)t4/4	100 t1/4	10-1 t3/2	00-1 (1-k4)t4/4	0-1-1 t1/2	00-1 (1-k4)t4/4	10-1 t3/2	100 t1/4	110 (1+k4)t4/4
	$U_{dc1}-U_{dc2}<-h$	5	$i_a < 0$ $i_c < 0$		00-1 t4/4	10-1 t3/2	100 t1/2	110 t4/2	100 t1/2	10-1 t3/2	00-1 t4/4	
		6	$i_a < 0$ $i_c \geq 0$		00-1 t4/4	10-1 t3/2	100 t1/2	110 t4/2	100 t1/2	10-1 t3/2	00-1 t4/4	
		7	$i_a \geq 0$ $i_c < 0$		100 t1/4	10-1 t3/2	00-1 t4/2	0-1-1 t1/2	00-1 t4/2	10-1 t3/2	100 t1/4	
		8	$i_a \geq 0$ $i_c \geq 0$	110 (1+k4)t4/4	100 t1/4	10-1 t3/2	00-1 (1-k4)t4/4	0-1-1 t1/2	00-1 (1-k4)t4/4	10-1 t3/2	100 t1/4	110 (1+k4)t4/4
Area B of triangle	$U_{dc1}-U_{dc2}>h$	9	$i_a \geq 0$		100 t1/2	10-1 t3/2	1-1-1 t2/2	1-1-1 t2/2	10-1 t3/2	100 t1/2		
		10	$i_a < 0$		0-1-1 t1/2	1-1-1 t2/2	10-1 t3/2	10-1 t3/2	1-1-1 t2/2	0-1-1 t1/2		
	$U_{dc1}-U_{dc2}<-h$	11	$i_a < 0$		100 t1/2	10-1 t3/2	1-1-1 t2/2	1-1-1 t2/2	10-1 t3/2	100 t1/2		
		12	$i_a \geq 0$		0-1-1 t1/2	1-1-1 t2/2	10-1 t3/2	10-1 t3/2	1-1-1 t2/2	0-1-1 t1/2		
Area D of triangle	$U_{dc1}-U_{dc2}>h$	13	$i_c \geq 0$		00-1 t4/2	10-1 t3/2	11-1 t5/2	11-1 t5/2	10-1 t3/2	00-1 t4/2		
		14	$i_c < 0$		110 t4/2	11-1 t5/2	10-1 t3/2	10-1 t3/2	11-1 t5/2	110 t4/2		
	$U_{dc1}-U_{dc2}<-h$	15	$i_c < 0$		00-1 t4/2	10-1 t3/2	11-1 t5/2	11-1 t5/2	10-1 t3/2	00-1 t4/2		
		16	$i_c \geq 0$		110 t4/2	11-1 t5/2	10-1 t3/2	10-1 t3/2	11-1 t5/2	110 t4/2		

Simulation waveforms of the capacitor voltage on DC side without balance control on neutral potential voltage is shown in Fig.6(a). From 6(a) we can see that, the fluctuation of capacitor voltage is considerable large, and offset to opposite directions. Simulation waveforms of the

capacitor voltage on DC side with balance control on neutral potential voltage is shown in Fig. 6(b). From Fig. 6(a) we can see that, the offset of capacitor voltage is controlled better, and the fluctuation of voltage is limited in a very small range. Waveform shown in Fig. 6(b) is that measured in field operating with neutral balance control. From Fig. 6(b) we can see that the voltage of capacitors on the DC side is kept constant with very small ripples, the capacitor voltage up and down of the bus keep a very good balance feature. After applying the neutral potential balance control method, related requirements for capacitor voltage balance are satisfied. Waveform of line voltage output by the established three-level inverter with neutral potential balance control is shown in Fig.7. From Fig.7 we can see that: the line voltage U_{ab} of AC side has five levels and a steady waveform, proving that the capacitor voltage on DC bus is controlled properly, which satisfies the requirements for output constant direct current.

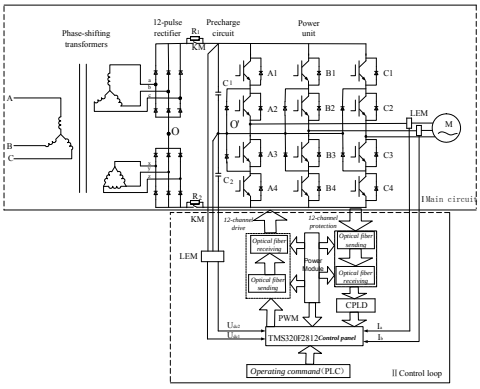

Fig.5 Structure diagram of three-level inverter system

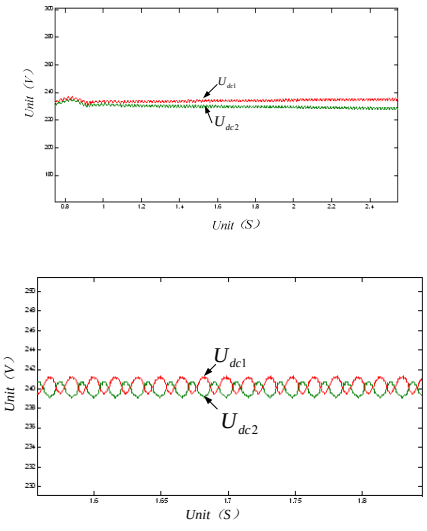

Fig.6 (a) U_{dc1} and U_{dc2} without neutral potential control; (b) U_{dc1} and U_{dc2} with neutral potential control

Conclusions

Comparing with two-level inverter, three-level inverter has much more advantages. However, the topological structure of three-level inverter brings an inherent problem, which is known as unbalanced neutral potential. Aiming to this problem, this paper analyses the root reason for unbalanced neutral voltage and then proposed a control method for voltage balance based on hysteresis control technology. Furthermore, it gives related methods for selecting switch states and switch sequences and the distribution principle for the acting time of switches when the reference voltage vector falls in Area B with one redundant switch state and Area C with two such states, it also lists the switch sequences and acting time table detailedly. The simulation and experimental results shows that this method could achieve a very good neutral balance effect, it owns a considerable good practice guidance on the balance control of capacitor voltage of three-level inverter.

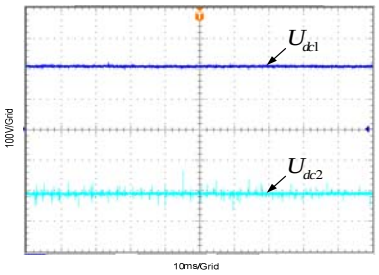

Fig.7 Capacitor voltage waveform U_{dc1} and U_{dc2} with neutral potential control

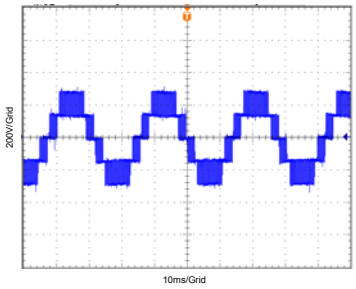

Fig.8 Three inverter line voltage waveform U_{ab}

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