Jiangang HAN, Tianhao TANG

Shanghai Maritime University

A multilevel active rectifier based on series connection of asymmetrical H-bridge cells

Abstract. A novel multilevel active rectifier based on series connection of asymmetrical H-bridge cells is presented in this paper. The converter can generate seven voltage levels with eight power switches. However it can lead the output capacitor voltage unbalanced. Then PI controller has been applied to guarantee the output DC voltage in the outer loop. A proportion controller is used to control the inductance current in phase with the grid voltage and to reduce the harmonic feed to gird. All the methods have also been verified by the results of simulation and experiment.

*Streszczenie. W artykule przedstawiono nową strukturę wielopoziomowego prostownika aktywnego, opartą na szeregowo połączonych, niesymetrycznych mostkach typu H. Przekształtnik może wygenerować 7 poziomów napięcia z wyjściowego, wykorzystując 8 łączników. Opracowano algorytm sterowania i modulacji, pozwalające na uzyskanie stabilności napięcia DC, redukcję przesunięcia fazowego prądu dławika oraz zawartości harmonicznych. Działanie układu i sterowania poddano weryfikacji symulacyjnej i eksperymentalnej. (**Wielopoziomowy prostownik aktywny oparty na szeregowo połączonych, niesymetrycznych mostkach typu H**).*

Keywords: Active rectifier, multilevel converter, asymmetrical bridge, voltage balance.
Słowa kluczowe: prostownik aktywny, przekształtnik wielopoziomowy, mostek niesymetryczny, regulacja napięcia.

Introduction

Multilevel converter has been receiving increased attention for their capability of high voltage operation, high efficiency [1]. Numerous topologies and modulation strategies have been introduced and studied extensively for utility and drive application in recent literature [1, 2]. Three main types of multilevel converters, i.e. diode-clamp, flying-capacitor, and cascade converter with separated dc supplies, have been developed. The cascade multilevel converter uses several full bridges in series to synthesize waveforms. This topology is free from complicated connections and large numbers of components to diode clamp and flying capacitor converters. And it does not have a capacitor voltage-balancing problem with separated dc sources. Then it is a good choice to be used active rectifier for high power and high voltage applications [3-10]. A cascade H-bridge active rectifier is presented for drive application which allows the bidirectional power flow [3], but it needs a transformer. The design procedure of single-phase multilevel rectified is proposed [4]. And an energy-based method is applied to the cascade H-bridge rectifier [5]. A selective harmonic elimination approach, which can keep the dc voltage balance, is adopted to cascade H-bridge rectifier. A low frequency predictive current control is applied to multilevel rectifier.

This paper presents a novel multilevel active rectifier, which consists of two asymmetrical four-level H-bridge. Then the detailed analysis of active rectifier is proposed. And the design of the two-loop controller is shown. Finally, the simulation and experimental results validate the effectiveness of the proposed converter.
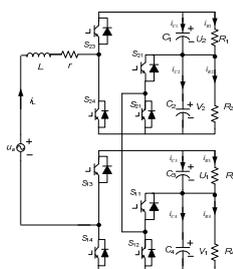
Fig.1. Topology of the proposed converter

Configuration of the Proposed Converter

The cascade multilevel active rectifier is one of the solution for high power and high voltage applications because of it allows to overcome the high power loss and high voltage stress on the power switches in conventional two-level rectifier. The single-phase multilevel active rectifier is shown in Fig.1. Two asymmetrical four-level modules (AFLM) are connected in series to form a single phase-phase multilevel converter. Each asymmetrical full-bridge circuit consists of four power switches and two DC capacitors. One half-bridge is connected to a DC capacitor in parallel, which is in series with the capacitor. And the other half-bridge is in parallel with the two capacitors in series. The AC terminal voltage of the cascade active rectifier is connected in series, and can be obtained by the following equation:

$$(1) \qquad v_{ab} = v_{ao} + v_{ob}$$

where: v_{ab}–AC voltage of active rectifier, v_{ao}, v_{ob}– voltage of AFLM. Each AFLM can generate four voltage levels, if we assume voltages of C_1 and C_2 are constant as U. The voltage levels and switching states are shown in Table 1. And there exist two complimentary switch pairs in the AFLM, (S_{21}, S_{22}) and (S_{23}, S_{24}). To obtain v_{ao} =0, power switch S_{21} and S_{23} are turned off. The v_{ao} is equal to U, when S_{21} and S_{23} are turned on. Turning on S_{23} and off S_{21} obtains v_{ao} =2U. The v_{ao} is equal to -U, when S_{21} are turned on and S_{23} are turned off. The other AFLM can generate four levels (0, U, -U,-2U) in the same, when V_1 and $U_1$are assumed as U. The active rectifier can generate total seven voltage levels when v_{ab} is kept symmetrical.

Table1. Voltage levels and switching states of AFLM

V_{ao}	Switch States			
	S_{21}	S_{22}	S_{23}	S_{24}
V_{ao}= 0	0	1	0	1
V_{ao}= U	1	0	1	0
V_{ao}= 2U	0	1	1	0
V_{ao}=-U	0	1	1	0

Principles of the converter

The Table 2 shows the voltage levels and switching states of the cascade multilevel active rectifier. There are sixteen switching combinations shown in the table. And it can be seen that some voltage levels are redundant from the table. More in detail, there are four different switching combinations for the 0 voltage level, three for U and -U, and

two for 2U and -2U, and no redundant combination for 3U and -3U. According the voltage levels, the detailed analysis of the operation modes of the proposed active rectifier is followed.

Table 2. Voltage levels and switching states

Mode / Voltage v_{ab}		Voltage		Switch States			
		v_{ao}	v_{ob}	S_{11}	S_{13}	S_{21}	S_{23}
1	Mode3: $v_{ab}=U$	U	0	0	0	1	1
2		0	U	1	0	0	0
3		2U	-U	1	1	0	1
4	Mode2: $v_{ab}=2U$	2U	0	0	0	0	1
5		U	U	1	0	1	1
6	Mode1: $v_{ab}=3u$	2U	U	1	0	0	1
7	Mode4: $v_{ab}=0$	0	0	0	0	0	0
8		-U	U	1	0	1	0
9		U	-U	1	1	1	1
10		2U	-2U	0	1	0	1
11	Mode7: $v_{ab}=-3U$	-U	-2U	0	1	1	0
12	Mode6: $v_{ab}=-2U$	0	-2U	0	1	0	0
13		-U	-U	1	1	1	0
14	Mode5: $v_{ab}=-U$	0	-U	1	1	0	0
15		-U	0	0	0	1	0
16		U	-2U	0	1	1	1

Mode 1($v_{ab}=3U$): There is only one switching combination, and the equivalent circuits are shown in Fig.2a. In Fig.2a, S_{11} and S_{23} are turned off, and S_{13} and S_{21} are turned on. When the AC power source works as positive power, the positive inductance current will decrease with the slop of $(v_{C1}+ v_{C2}+ v_{C4}-u_a)/L$ for $v_{C1}+ v_{C2}+ v_{C4}>u_a$. Then the positive current charges C_1, C_4 and C_2, and supplies the load power. Mode 2($v_{ab}=2U$): There are two different switching combinations, and the equivalent circuits are shown in Fig.2b and 2c respectively. In Fig.2b, S_{11}, S_{21} and S_{13} are all turned off, and S_{23} is turned on. The positive current charges C_1 and C_2, which approximately linearly decreases with the slop of $(v_{C1}+ v_{C2} -u_a)/L$ if $v_{C1}+ v_{C2} >u_a$. In Fig.2c, The positive current charges C_1 and C_4, and supplies the load. Mode 3($v_{ab}=U$): There are three different switching combinations shown in Fig.2d, 2e and 2f. Fig.2d shows the equivalent circuit of one of those operation modes, where the S_{11} and S_{13} are turned off, and S_{21} and S_{23} are turned on. In Fig.2d and 2e, for the positive main current, the capacitor C_2 (or C_4) will be charged when the $v_{ao}=U$, and $v_{ob}=0$ (or $v_{ao}=0$, and $v_{ob}=U$). If the current is negative, the capacitor C_2 (or C_4) will be discharged. In the positive half-cycle of AC voltage, the main current will vary with the slope of $(u_a-v_{C1})/L$. It will increase if $u_a>v_{C1}$ or decrease if $u_a<v_{C1}$. The switching state shown in Fig. 2f can be used to compensate capacitor voltage, where the S_{11}, S_{13} and S_{23} are turned on, and S_{21} is turned off. The capacitor C_1 and C_2 are charged and C_3 is discharged if the main current is positive. Otherwise the capacitor C_1 and C_2 are discharged and C_3 is charged. Mode 4($v_{ab}=0$): There are four different switching combinations shown in Fig.3a-3d. In this mode, the voltage v_{ab} is equal to 0. Then the inductance voltage is equal to the AC voltage u_a and the inductance current increase or decrease with the slop of u_a/L. In Fig.3a, the switches of S_{11}, S_{13}, S_{21} and S_{23} are turned off. It means the current will not charge or discharge any capacitor although the main current is positive or negative. But the other three switching combinations can be used to compensate the capacitor voltage. For example, Fig.3b shows the equivalent circuit of one of those operation modes, where the S_{11} and S_{13} are turned off, and S_{21} and S_{23} are turned on. If the main current is positive, the current charges the capacitor C_4 and discharges the capacitor C_2

when the $v_{ao}=-U$, $v_{ob}=U$. Otherwise it will discharge C_4 and charge C_2. It's similar to the other two switching states. Mode 5($v_{ab}=-U$): There are three different switching combinations shown in Table 2. In this mode, the working principle is similar to Mode 3, but the active rectifier works in the negative half-cycle of AC voltage. Mode 6($v_{ab}=-2U$): There are two different switching combinations shown as state 12 and 13. This mode is similar to Mode 2. Mode 7($v_{ab}=-3U$): There is only one switching state which works like Mode 1.

Mathematical model
According to the switching states of the active rectifier, differential equations of the converter can be described as:

$$(2) \qquad \frac{di_L}{dt} = \frac{1}{L}(u_a - i_L R - v_{ab})$$

$$(3) \qquad \frac{du_{C1}}{dt} = \frac{1}{C_1}(S_{23}i_L - \frac{u_{C1}}{R_1})$$

$$(4) \qquad \frac{du_{C2}}{dt} = \frac{1}{C_2}[(S_{21} - S_{21}S_{23} + \overline{S}_{21}S_{23})i_L - \frac{u_{C2}}{R_2}]$$

$$(5) \qquad \frac{du_{C3}}{dt} = \frac{1}{C_3}(S_{13}i_L - \frac{u_{C3}}{R_3})$$

$$(6) \qquad \frac{du_{C4}}{dt} = \frac{1}{C_4}[(S_{11} - S_{11}S_{13} + \overline{S}_{11}S_{13})i_L - \frac{u_{C4}}{R_4}]$$

$$(7) \qquad v_{ab} = v_{ao} + v_{ob}$$

where

$$(8) \qquad v_{ao} = S_{23}(v_{C1} + v_{C2}) - S_{21}v_{C2}$$

$$(9) \qquad v_{ob} = S_{11}v_{C4} - S_{13}(v_{C3} + v_{C4})$$

The state equations of the proposed seven-level active rectifier can be rewritten as following:

$$(10) \qquad \dot{x} = Ax + Bu$$

where:

$$(11) \qquad x = \begin{bmatrix} i_L \\ u_{C1} \\ u_{C2} \\ u_{C3} \\ u_{C4} \end{bmatrix} \quad B = \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad u = u_a$$

$$A = \begin{bmatrix} -\frac{R}{L} & -\frac{S_{23}}{L} & \frac{S_{21}-S_{23}}{L} & \frac{S_{13}}{L} & \frac{S_{13}-S_{11}}{L} \\ \frac{S_{23}}{C_1} & -\frac{1}{R_1C_1} & 0 & 0 & 0 \\ \frac{S_{21}-S_{23}S_{21}+S_{23}}{C_2} & 0 & -\frac{1}{R_2C_2} & 0 & 0 \\ \frac{S_{13}}{C_3} & 0 & 0 & -\frac{1}{R_3C_3} & 0 \\ \frac{S_{11}-S_{11}S_{13}+S_{13}}{C_4} & 0 & 0 & 0 & -\frac{1}{R_4C_4} \end{bmatrix}$$

It can be found that the equation (10) is a time-varying nonlinear system.
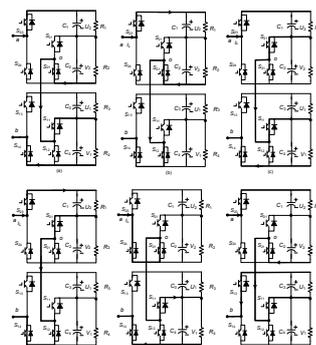
Fig.2. Operations modes of the proposed rectifier (Mode 1: (a). Mode 2: (b), (c). Mode 3: (d),(e), (f).).
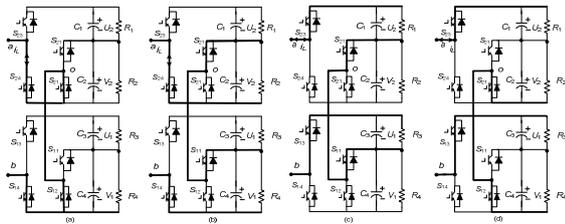
Fig.3. Operations modes (Mode 4: (a), (b), (c), (d).).

Control of the multilevel active rectifier

The cascade multilevel active rectifier is used to produce sinusoidal current in phase with the AC voltage and to eliminate the harmonic which will be feed to the AC side. And the capacitor voltages should be kept be balance.

Fig.4 shows the basic control block of the proposed single phase multilevel active rectifier. The controller consists of two control loop: the outer voltage loop and the inner current loop. A PI voltage controller is used in the outer control loop to regulate the capacitor voltages.
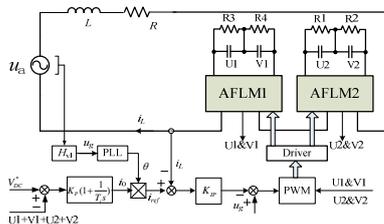
Fig.4. Control scheme of the proposed active rectifier

Current controller

The simplified current control loop is shown in Fig.5. As the current controller is used to control the grid current, the plant can be simplified as $1/(Ls+R)$. K_{PWM} is the converter gain, which can be regarded as unity by measuring the dc bus voltage. A delay is equal to T_s to compensate the modulation and computing time, which is also the sampling time of the system.
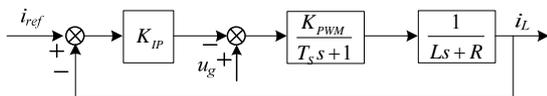
Fig.5. Current control loop.

If the current controller gain is set to K_{IP} and the gird voltage disturbance is ignored, the closed-loop transfer function F(s) of the system is obtained as equation (12), where ω_c is the natural frequency of the current closed loop, ξ is the damping ratio.

$$(12) \quad \begin{aligned} F(s) &= \frac{K_{IP}}{T_S L s^2 + (RT_S + L)s + (R + K_{IP})} \\ &= \frac{K_{IP}}{T_S L} \frac{1}{s^2 + 2\xi\omega_c s + \omega_c^2} \end{aligned}$$

Where:

$$(13) \quad \omega_c = \sqrt{\frac{R + K_{IP}}{T_S L}}$$

$$(14) \quad \xi = \sqrt{\frac{(T_S R + L)^2}{(R + K_{IP})T_S L}}$$

The current-loop dynamics is tuned to get a closed-loop time response of about five to ten times the switching periods, and the desired damping ratio ξ is set to 0.707. The parameter K_{IP} is can be obtained in equation (14).

Voltage controller

Precisely, the voltage-loop time response has to be ten times slower than that of the current loop, which is useful to guarantee the dynamics and stability. The simplified voltage control loop is shown in Fig.5. The current loop simplified as one-order delay. And the time constant T_C is n (n = 5-10) times the switching period T_S. The dc output capacitor can be simplified as C, if we assume $C_1 = C_2 = C_3 = C_4 = C$ [4].
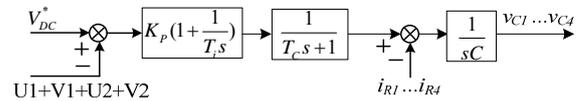
Fig.5. Voltage control loop.

The open-loop transfer function T(s) of voltage loop can be deduce as:

$$(15) \quad T(s) = K_P \frac{T_i s + 1}{T_i s} \frac{1}{T_C s + 1} \frac{1}{Cs}$$

Then PI controller parameters can be obtained by equation (16) and (17) based on the optimum symmetrical method [4, 6].

$$(16) \quad T_i = \frac{1}{T_C \omega_v^2}$$

where: ω_v – open-loop crossover frequency.

$$(17) \quad K_P = \frac{C}{\sqrt{T_i T_C}}$$

Simulation results

A simulation model is carried out with MATLAB/Simulink simulation software utilizing SimPowerSystem toolbox. The system parameters are given as following: $L = 10mH$, $C_1 = C_3 = C_2 = C_4 = 2200uF$, $R_1 = R_3 = R_4 = R_2 = 50\Omega$, $u_a = 311.8\sin(\omega t)V$, $V_1 = U_1 = V_2 = U_2 = 120V$, switching frequency $f=10kHz$, $K_P = 0.0125$, $T_i = 0.0625$, $K_{IP} = 16$. The u_{ab} shown in Fig.6(a) is the typical of seven-level converters. Fig.6(b) shows grid voltage and the low distorted grid current.
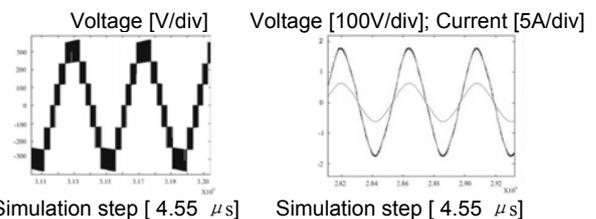
Fig.6 (a) Voltage of u_{ab}; (b) Voltage and current of u_a

Experimental results

After simulation, the active rectifier is developed on the laboratory setup, and the controller is carried out on the FPGA (Spartan-3E) from the Xilinx Corp. The system parameters are given as following: $L = 10mH$, $R_1 = R_3 = R_4 = R_2 = 25\Omega$, $u_a = 114 \sin(\omega t)V$, $V_1 = U_1 = V_2 = U_2 = 60V$, and the other parameters are same to the simulation.

Fig.7 shows the generated seven levels ac voltage and inductance current, and the grid voltage and current. The gird current is approximate in the phase of grid voltage, which will result in a higher efficiency of the system. Fig.8

shows the output capacitor voltages of an asymmetrical H-bridge, which are kept in a satisfactory range.
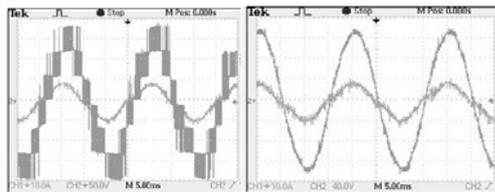
Fig.7 (a)Votltage of u_{ab} and inductiance current (b) Votltage and current of u_a
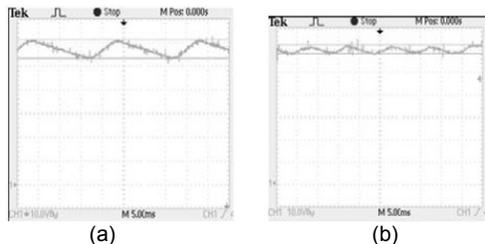
Fig.8 Votltage of capacitors: (a) C_1. (b) C_2.

Conclusions

In this paper, a hybrid multilevel active rectifier based on series connection of asymmetrical H-bridge cells is presented. The detailed analysis of operation modes is shown. The converter allows seven voltage levels with eight power switches. Then PI controller has been applied to guarantee the DC bus voltage in the outer loop. A proportion current controller is used to control the inductance current in phase with the grid voltage and to reduce the harmonic feed to the grid. And redundant switching combinations are used to keep the output capacitor voltage balance considering the AC voltage and current. All the methods have also been verified by the results of simulation and experiment. The method can easily be extended for use on a three-phase active rectifier.

REFERENCES
[1] Rodriguez J., J. Lai, and F. Z. Peng, Multilevel Inverters: a Survey of Topologies, Controls, and Applications, *IEEE Trans. on Industry Electronics*, 49(2002), No.4,724–738.
[2] Jingang Han, Tianhao Tang, A Hybrid Cascade Asymmetrical Multilevel Converter with Isolated Voltage Source, *Proceedings of IEEE IECON*, 2007, 2119-2123
[3] Jian Wang and Yongdong Li, PWM Rectifier in Power Cell of Cascaded H-bridge Multilevel Converter, *Proceedings of International Conference on Electrical Machines and Systems*, 2007, 18-21.
[4] C. Cecati, A. Dell'Aquila, M. Liserre, and V. G. Monopoli, Design of H-Bridge Multilevel Active Rectifier for Traction Systems, *IEEE Trans. on Industry Applications*, 39(2003), No. 5,1541–1550.
[5] A. Dell'Aquila, M. Liserre, V. G. Monopoli, and P. Rotondo, An Energy-Based Control for an n-H-Bridges Multilevel Active Rectifier, *IEEE Trans. on Industry Applications*, 52 (2005), No. 3, 670–678
[6] A. Dell'Aquila, M. Liserre, V. G. Monopoli, and P. Rotondo, Overview of PI-Based Solutions for the Control of DC Buses of a Single-Phase H-Bridge Multilevel Active Rectifier, *IEEE Trans. on Industry Applications*, 44 (2008), No. 3, 857–866

Authors: dr. Jingang Han, the Institute of Electric Drives & Control Systems, Shanghai Maritime University, 201306 Shanghai, China, E-mail: jghan@shmtu.edu.cn; prof. Tianhao Tang, the Institute of Electric Drives & Control Systems, Shanghai Maritime University, 201306 Shanghai, China, E-mail: thtang@shmtu.edu.cn.