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Minimum Operating Supply Voltage of MCML Circuits

Abstract. The power dissipations of the MCML circuits can be effetely reduced by lowering its supply voltage. In this paper, a low-power scheme for MCML circuits is proposed, where the pull-down network (PDN) NMOS transistors operate at saturation region or linear region, so that the minimum source voltage can be effectively reduced. The analysis for minimum operating supply voltage of MCML circuits is addressed. Scaling down the supply voltage of MCML circuits is investigated. A mode-10 counter at a NCSU 45nm technology is implemented to verify its power efficiency.

*Streszczenie. W artykule przedstawiono schemat obwodu logicznego typu MCML niskiej mocy. Struktura zawiera tranzystory NMOS pull-down pracujące w obszarze nasycenia lub liniowym. Przeprowadzono analizy przy minimalnym napięciu zasilającym układ. W celu weryfikacji energooszczędności obwodu zbudowano licznik w trybie mode-10 w technologii NCSU (45nm). (**Układ MCML z minimalnym operacyjnym napięciem zasilającym**).*

Keywords: MOS current mode logic, minimum operating supply voltage, low power and high-speed applications.
Słowa kluczowe: prądowy układ logiczny MOS, minimalne zasilające napięcie operacyjne, aplikacje niskiej mocy dużej prędkości.

Introduction

Total energy dissipation in a conventional CMOS circuit is mostly composed of two components: switching energy due to charging and discharging for loads, and static energy dissipation caused by leakage currents of MOS devices [1]. Technology scaling increases the density and performance of integrated circuits, resulting in large dynamic dissipations. The aggressive scaling of device dimensions has significantly increased leakage current exponentially [2]. With the increasing demand for battery-operated mobile platforms, energy-efficient designs have become more and more important in nanometer CMOS circuits. MOS current mode logic (MCML) techniques are usually used for high-speed applications [3]. However, the MCML circuits have large static power due to their constant operation currents. Recently, the low power MCML designs have obtained some attentions [4]. G. Caruso et al. presented general design methodologies for the low-power MCML circuits [5]. M. H. Anis et al. proposed the multi-threshold MCML (MTMCML) technology to lower the power dissipations [6].

The power dissipation of the MCML circuits can be effetely reduced by lowering its supply voltage. However, in typical designs of the MCML circuits, the supply voltage of the MCML circuits has a minimum limit, at which the pull-down network (PDN) NMOS transistors and the current source transistor should operate at velocity saturation region, resulting in a large minimum source voltage [7]. In this paper, we propose a low-power scheme of high-speed MCML circuits, where the PDN NMOS transistors of the MCML circuits operate at saturation region or linear region, so that the minimum source voltage of the MCML circuits can be effectively reduced.

MCML circuits

The basic MCML inverter/buffer and its bias circuit are shown in Fig. 1. The MCML inverter is composed of three main parts: the load transistors P1 and P2, the full differential pull down switch network consisting of N1 and N2, and the current source transistor Ns. The load transistors are designed to operate at linear region with the auxiliary of the control voltage V_{rfp}, which also controls the output logic swings. The pull-down network NMOS N1 and N2 are used to perform logic operation. The NMOS Ns is used to provide the constant current source, which is controlled by voltage V_{rfn} from the bias circuit. In the MCML, the signal V_{rfn} is generated from the bias circuit to ensure the proper operating for output voltage swings and to provide the constant bias current.

The operation of MCML is performed in the current domain. The pull down network switches the constant current between two branches, and then the load converts the current to output voltage swings. The high and low digital logic levels are

$$(1) \qquad V_{OH} = V_{DD}$$

$$(2) \qquad V_{OL} = V_{DD} - I_B R_D$$

where V_{DD} is source voltage, I_B is bias current, and R_D is PMOS load resistance, respectively. The logic swing is
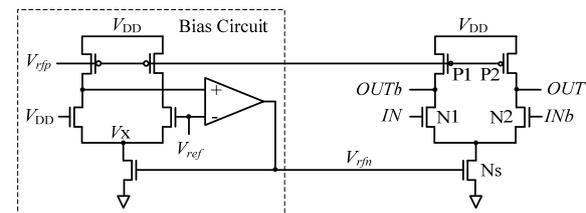
Fig.1. MCML inverter/buffer and its bias circuit

$$(3) \qquad \Delta V = V_{OH} - V_{OL} = I_B R_D$$

The optimization performance metrics of the MCML cells mainly include propagation delay, power dissipation, and power-delay product. The power consumption of a MCML cell can been written as

$$(4) \qquad P = V_{DD} \cdot I_B$$

For given V_{DD} and I_B, the power dissipation of MCML cells is a constant value. It is independent of both the operation frequencies and fanouts.

The delay time of a MCML cell can be calculated assuming that, at each transition, the whole I_B, ideally, flows through one branch of the differential pair and charges the total load capacitance C, is given by

$$(5) \qquad t_d = 0.69 \cdot RC = 0.69 \cdot C \cdot \Delta V / I_B$$

where C is identical load capacitance on an output node. The power-delay product can be calculated as

$$(6) \qquad PDP = P \cdot t_d = 0.69 V_{DD} \cdot \Delta V \cdot C$$

The power dissipation and power-delay product can be optimized from (4) – (6). The power dissipation of the

MCML circuits can be effetely reduced by lowering its supply voltage, since it is proportional to its supply voltage.

Minimum operating supply voltage

The supply voltage of the MCML circuits has a minimum limit, at which the current source transistor should operate at velocity saturation region, and the pull-down network NMOS transistors should be turn on. As shown in Fig. 2, in order that N1 operates at saturation region, in almost all designs, the logic swing is taken as $\Delta V < V_{TH}$.
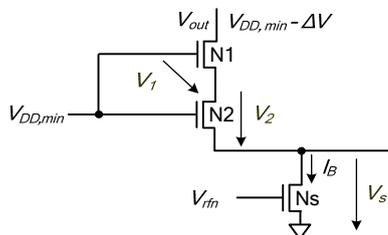
Fig.2. Minimum operating supply voltage of MCML circuits

For a two-level MCML circuits, as shown in Fig. 2, the logic transistor N1 operate at saturation region, while the logic transistor N2 operates at linear region. Therefore, the minimum operating supply voltage can been written as

(7) $$V_{DD,min} = V_{1,gs} + V_{2,ds} + V_{s,dsat}$$

where $V_{1,gs}$ is gate-source voltage of N1 when it operates in saturation state, $V_{2,ds}$ is drain-source voltage of N2 when it operates in linear situation, and $V_{s,dsat}$ is the drain-source voltage of Ns when it operates at velocity saturation point, respectively. When NMOS operating at velocity saturation point, its drain current I_{dsat}, and the drain-source voltage V_{dsat}, are given in the BSIM3 MOSFET model, which represents the standard model for deep submicron to nanoscale CMOS technologiess

(8) $$I_{dsat} = W_{eff} C_{ox} v_{sat} (V_{gs} - V_{th} - A_{bulk} V_{dsat})$$

(9) $$V_{dsat} = \frac{E_{sat} L_{eff} (V_{gs} - V_{th})}{A_{bulk} E_{sat} L_{eff} + (V_{gs} - V_{th})}$$

where W_{eff} is the effective device channel width. C_{ox} is the gate capacitance per unit area, v_{sat} is the saturation velocity of the carrier, E_{sat} is the critical electric field at which the carrier velocity becomes saturated, L_{eff} is the effective device channel length, respectively. A_{bulk} is used to account for the bulk charge effect, including both the short channel effects and narrow width effect, and can be estimated from some extracted parameter listed in the simulation model card. A_{bulk} is close to unity if the channel length is small, and rises as channel length increase. From (8) and (9), eliminating parameter V_{gs}, we have V_{dsat} expressed by I_{dsat}

(10) $$V_{dsat} = \frac{I_{dsat}}{2 A_{bulk} W_{eff} C_{ox} v_{sat}} \times \left(\sqrt{1 + \frac{4 A_{bulk} W_{eff} L_{eff} C_{ox} v_{sat} E_{sat}}{I_{dsat}}} - 1 \right)$$

Since a part of (10) satisfies

(11) $$\frac{4 A_{bulk} W_{eff} L_{eff} C_{ox} v_{sat} E_{sat}}{I_{dsat}} \gg 1$$

Equation (10) can be simplified as

(12) $$V_{dsat} = \sqrt{\frac{L_{eff} E_{sat} I_{dsat}}{A_{bulk} W_{eff} C_{ox} v_{sat}}}$$

Again, by eliminating V_{dsat}, we get V_{gs} expressed by I_{dsat}, from (8) and (9)

(13) $$V_{gs} = V_{th} + \frac{I_{dsat}}{2 W_{eff} C_{ox} v_{sat}} \left(1 + \sqrt{1 + \frac{4 A_{bulk} W_{eff} L_{eff} C_{ox} v_{sat} E_{sat}}{I_{dsat}}} \right)$$

Equation (13) can be simplified as

(14) $$V_{gs} = V_{th} + \sqrt{\frac{A_{bulk} L_{eff} E_{sat} I_{dsat}}{W_{eff} C_{ox} v_{sat}}}$$

Equations (12) and (14) are more convenient and suitable than (10) and (13) for the hand calculation. When NMOS operating in linear mode, the drain current is expressed as

(15) $$I_{ds} = \mu_{eff} C_{ox} \frac{W_{eff}}{L_{eff}} \left(V_{gs} - V_{th} - \frac{A_{bulk} V_{ds}}{2} \right) V_{ds}$$

where μ_{eff} is the effective mobility. A part of this original equation has been omitted at the acceptable range of error for the convenience of hand calculation. From (15), we can get V_{gs} expressed by I_{ds}

(16) $$V_{ds} = \frac{V_{gs} - V_{th}}{A_{bulk}} - \frac{1}{A_{bulk}} \sqrt{(V_{gs} - V_{th})^2 - \frac{2 A_{bulk} L_{eff} I_{ds}}{\mu_{eff} C_{ox} W_{eff}}}$$

Substituting (16) in (8), and applying parameters to suitable transistors according to Fig. 2, and substituting $V_{2,gs}$ with $V_{DD,min} - V_{s,dsat}$, and then rearranged, we arrive at the final equation of the minimum supply voltage of the universal 2-level MCML logic is

(17) $$V_{DD,min} = V_{s,dsat} + \frac{1}{2 - A_{2,bulk}} V_{2,th} - \frac{A_{2,bulk} - 1}{2 - A_{2,bulk}} V_{1,gs}$$

$$+ \frac{1}{2 - A_{2,bulk}} \sqrt{(V_{1,gs} - V_{2,th})^2 + (2 - A_{2,bulk}) \frac{2 L_{2,eff} I_B}{\mu_{eff} C_{ox} W_{2,eff}}}$$

When estimating $V_{s,dsat}$ and $V_{1,gs}$ in (17) through (12) and (14), I_{dsat} should be replaced by the bias constant current I_B, and other parameters should be substituted by the values from the corresponding transistors. According to (17), the minimum supply voltage can be estimated. When substituting the parameters in (17) with actual values from model card, we can get the relationship of the minimum supply voltage $V_{DD,min}$ and the bias current I_B, as shown in Fig. 3. If MCML circuits operate at a low speed application, only a small I_B is required. For low speed applications, a small I_B can be used, and thus the supply voltage can be reduced, so that more power saving can be obtained.

Simulation results

With the purpose of the performance verification, a D flip-flop based on MCML circuits has been verified, as shown in Fig. 4, which composed of two D type latch.

For comparison, the C^{2}MOS positive edge-triggered D flip-flop cell extracted from the NCSU FreePDK45 osu_soc standard cell library is also simulated.
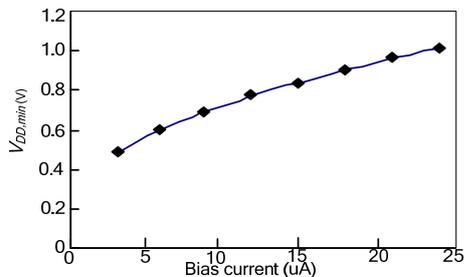
Fig.3. Minimum supply voltage of the 2-level MCML logic circuits
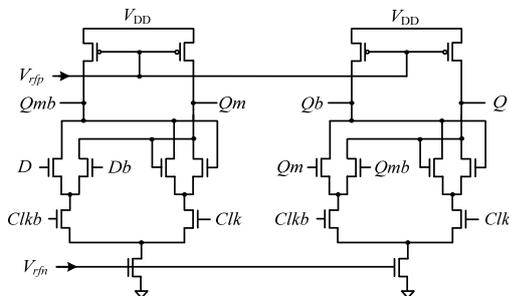
Fig.4. Master-slave positive edge-triggered MCML *D*-Flip flop

A mode-10 counter based on the MCML circuits and other combinational cells is implemented to verify their power dissipations. The full custom layout is drawn, and the full parasitic parameters are extracted. The power dissipation of the mode-10 counters based on the MCML circuits and the conventional CMOS libraries at different operation frequency is shown in Fig. 5 at the NCSU FreePDK 45nm technology and 1.0V supply voltage. As the operation frequency rises from 10MHz to 2GHz, the power dissipations of the counter based on traditional CMOS libraries increase rapidly, while the counterpart based on MCML keeps a constant value. Layout post simulations also have been carried out for the MCML mode-10 counter and the C^{2}MOS counterpart by varying the supply voltage from nominal 1.1V to 0.7V with the operation frequency at 1GHz. Fig. 6 illustrates the power dissipations of mode-10 counters based on the MCML and C^{2}MOS *D* flip-flop at different supply voltages.
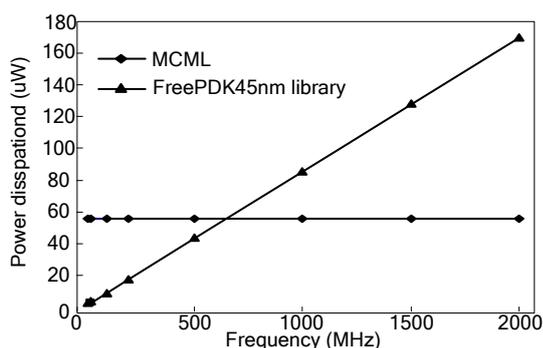
Fig.5. The power dissipations of mode-10 counters based on MCML and conventional CMOS at different operation frequency and 1.0V supply voltage

From Fig. 6, the power dissipated of the MCML mode-10 counter decreases as the supply voltage falls from nominal voltage to near-threshold voltage, as the same trend as the conventional CMOS counterparts.
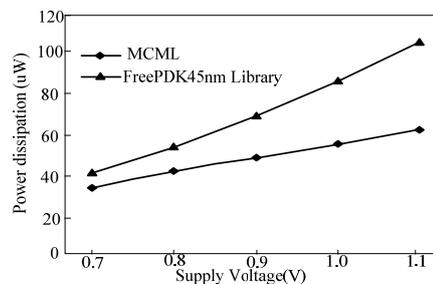
Fig.6. The power dissipation of mode-10 counters based on MCML conventional CMOS at different supply voltages

Conclusions

In this paper, the low-power scheme for the high-speed MCML has been presented, where the pull-down network NMOS transistors operate at saturation region or linear region, so that the minimum source voltage can be effectively reduced. The analysis for minimum operating supply voltage of MCML circuits has been addressed. Scaling down the supply voltage of MCML circuits has been also investigated. The post-layout simulations show that the power consumption of the MCML basic gates can be reduced by lowering the supply voltage without performance degrading. The proposed scheme of MCML circuits can be for low-power high-speed applications.

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