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DC-Link Voltage Balancing Method with Reduced Common-Mode Voltage for a Five-Level ANPC Inverter

***Abstract**. This paper presents a DC-link voltage balancing method with reduced common-mode voltage for a five-level active neutral-point clamped (ANPC) inverter. The DC-link voltage balancing method is based on zero-sequence voltage injection using carrier-based PWM. By further limiting the range of injected zero-sequence voltages, the amplitude of common-mode voltage can be reduced to 1/4 of the dc-link voltage. Experimental results are presented to verify the validity of this method.*

***Streszczenie.** W artykule przedstawiono metodę balansowania napięciami kondensatorów obwodu pośredniczącego DC dla pięcio-poziomowego falownika Active NPC z redukcją napięcia common-mode. W metodzie wykorzystywana jest modulacja PWM z falą nośną i sygnałem kolejności zerowej, o regulowanym zakresie aplikacji. Przedstawiono wyniki eksperymentalne. (**Wyrównywanie napięć w DC-link w pięciopoziomowym falowniku ANPC – redukcja napięcia common-mode**).*

Keywords: DC-link voltage balancing, common-mode voltage, zero-sequence voltage, five-level ANPC converter.
Słowa kluczowe: balansowanie napięciami DC-link, napięcie common-mode, napięcie kolejności zerowej, pięcio-poziomowy przekształtnik ANPC.

Introduction

Multilevel converters receive increasing attentions in recent years due to the requirement of high power and high voltage in power industrial applications [1–3]. Plenty of multilevel topologies have been investigated, but only several of them are practical for industrial applications [1]. Among the existing multilevel converters, neutral-point clamped (NPC) and cascaded H-bridge multilevel converters are the most widely used [2]. As a completely mature topology, three-level NPC converter has become the industry standard in medium-voltage (2.3, 3.3 and 4.16 kV) applications [3]. However, limited by the present semiconductor blocking voltage ratings, three-level NPC converter is hard to be applied to high voltage drives over 6 kV. Although five-level NPC converter is a choice in this case, it suffers from the voltage imbalance of dc-link capacitors and requires mass clamping diodes [3]. Flying-capacitor (FC) converter is another multilevel topology suitable for high power applications [4]. By properly using the redundant switching states, the voltages across all floating capacitors can be balanced. But it also requires mass clamping capacitors as the voltage level increases, which increases the cost and control complexity and makes the topology not so competitive for high voltage applications [2]. Five-level active neutral-point clamped (5L-ANPC) converter first proposed in 2005 [5] is an excellent multilevel topology which can overcome the above mentioned drawbacks in the NPC and FC multilevel converters [5] without transformers. A single phase of the 5L-ANPC converter is shown in Fig. 1. This paper proposes a DC-link voltage balancing method by zero-sequence voltage injection which can also reduce the common-mode voltage. Experimental results are presented to verify this method.

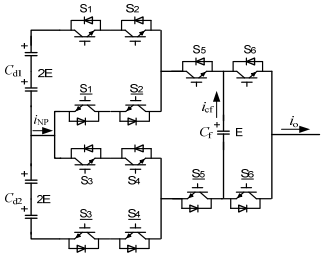

Fig.1. One phase leg of the 5L-ANPC inverter.

Neutral-Point Current Calculation

As shown in Fig. 1, the phase leg of the 5L-ANPC converter is comprised of twelve equally rated devices and a floating capacitor C_f.

Assume the dc-link voltage is $4E$ and the floating capacitor voltage is E. According to the above operating rules, each phase leg can output five voltage levels with eight distinct switching states. Defining the floating capacitor current is i_{cf} and neutral point (NP) current is i_{NP}, all the switching states with corresponding i_{cf} and i_{NP} are list in Table 1.

Table 1. Switching states of the 5L-ANPC inverter

S1	S2	S3	S4	S5	S6	V_o	i_{cf}	i_{NP}	Switching states
0	0	0	0	0	0	-2E	0	0	V0
0	0	0	0	0	1	-E	$\boldsymbol{i_o}$	0	V1
0	0	0	0	1	0	-E	$\boldsymbol{-i_o}$	$\boldsymbol{i_o}$	V2
0	0	0	0	1	1	0	0	$\boldsymbol{i_o}$	V3
1	1	1	1	0	0	0	0	$\boldsymbol{i_o}$	V4
1	1	1	1	0	1	E	$\boldsymbol{i_o}$	$\boldsymbol{i_o}$	V5
1	1	1	1	1	0	E	$\boldsymbol{-i_o}$	0	V6
1	1	1	1	1	1	2E	0	0	V7

As shown in Table 1, for voltage levels $-E$, 0 and E, each corresponds to two redundant switching states. The floating capacitor current i_{cf} is related with $-E$ and E.

For voltage level $-E$, states V1 and V2 generate the same voltage level with reverse i_{cf}. When the phase current i_o is positive, the state V1 will discharge the floating capacitor while state V2 will charge it. It is the same for voltage level E with states V5 and V6. So the floating capacitor voltage can be controlled by selecting different redundant switching states.

For a reference phase voltage u_x ($-2 \le u_x \le 2$), x represents the phase a, b or c, the duty cycle of outputting voltage level k (k = –2, –1, 0, 1 or 2) is defined as follows:

$$d_x^k = \begin{cases} u_x - k + 1, & u_x \in [k-1, k) \\ k + 1 - u_x, & u_x \in [k, k+1) \end{cases} \tag{1}$$

As can be seen from Table I, the two redundant switching states of both voltage levels $-E$ and E have different effects on the NP current. So the average NP current of a single phase in a switching period can be

calculated depending on the duty cycle of voltage level k and the redundant switching state it used.

If V1 is used to generate voltage level $-E$, then the average NP current in a switching period can be written as follows:

$$\bar{i}_{\mathrm{NP}x}=\begin{cases}0, & u_{\mathrm{x}}\in[-2,-1)\\ d_{\mathrm{x}}^{0}\cdot i_{\mathrm{x}}, & u_{\mathrm{x}}\in[-1,0)\end{cases} \tag{2}$$

If V2 is used to generate voltage level $-E$, then the average NP current in a switching period is:

$$\bar{i}_{\mathrm{NP}x}=\begin{cases}d_{\mathrm{x}}^{-1}\cdot i_{\mathrm{x}}, & u_{\mathrm{x}}\in[-2,-1)\\ d_{\mathrm{x}}^{-1}\cdot i_{\mathrm{x}}+d_{\mathrm{x}}^{0}\cdot i_{\mathrm{x}}, & u_{\mathrm{x}}\in[-1,0)\end{cases} \tag{3}$$

If V5 is used to generate voltage level E, then the average NP current in a switching period is:

$$\bar{i}_{\mathrm{NP}x}=\begin{cases}d_{\mathrm{x}}^{0}\cdot i_{\mathrm{x}}+d_{\mathrm{x}}^{+1}\cdot i_{\mathrm{x}}, & u_{\mathrm{x}}\in[0,1)\\ d_{\mathrm{x}}^{+1}\cdot i_{\mathrm{x}}, & u_{\mathrm{x}}\in[1,2]\end{cases} \tag{4}$$

If V6 is used to generate voltage level E, then the average NP current in a switching period is:

$$\bar{i}_{\mathrm{NP}x}=\begin{cases}d_{\mathrm{x}}^{0}\cdot i_{\mathrm{x}}, & u_{\mathrm{x}}\in[0,1)\\ 0, & u_{\mathrm{x}}\in[1,2]\end{cases} \tag{5}$$

Based on equations (1) – (5), the average NP current in a switching period generated by reference voltage u_{x} can be calculated. In a three-phase system, the average NP current in a switching period can be obtained:

$$\bar{i}_{\mathrm{NP}}=\bar{i}_{\mathrm{NPa}}+\bar{i}_{\mathrm{NPb}}+\bar{i}_{\mathrm{NPc}} \tag{6}$$

In order to maintain the DC-link capacitor voltages balanced and eliminate the offset, a reference NP current is expected to inject into the neutral point. Assuming the DC-link voltage deviation is

$$\Delta u=u_{\mathrm{d1}}-u_{\mathrm{d2}} \tag{7}$$

where: u_{d1} and u_{d2} – voltages of the upper and lower dc-link capacitors. the demanded NP current can be written as:

$$i_{\mathrm{NP,ref}}=-C\frac{\Delta u}{t_{\mathrm{p}}} \tag{8}$$

where: C – capacitance value of C_{d1} and C_{d2}, t_{p} – switching period. The target of DC-link voltage balancing method is to generate the demanded NP current by injecting a proper zero-sequence voltage.

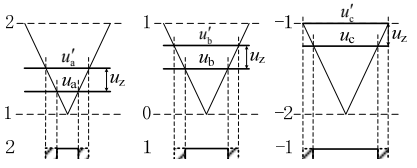

Fig. 2. Diagram of zero-sequence voltage injection.

Zero-Sequence Voltage Injection

As the only freedom degree in carrier-based PWM, zero-sequence voltage does not affect the output line voltage and current, but different zero-sequence voltages can lead to different switching states and so generate different NP currents.

Common-Mode Voltage Reduction

For a three-phase inverter, common-mode voltage is defined as:

$$U_{\mathrm{CM}}=(U_{\mathrm{ao}}+U_{\mathrm{bo}}+U_{\mathrm{co}})/3 \tag{9}$$

where: U_{CM} – the common-mode voltage, U_{ao}, U_{bo} and U_{co} – the actual instantaneous values of output three-phase voltages, which are $-2E$, $-\mathrm{E}$, 0, E or $2E$.

The three-phase reference voltages can be written as the sum of a integer and a positive decimal:

$$\begin{cases}u_{\mathrm{a}}=[u_{\mathrm{a}}]+\{u_{\mathrm{a}}\}\\ u_{\mathrm{b}}=[u_{\mathrm{b}}]+\{u_{\mathrm{b}}\}\\ u_{\mathrm{c}}=[u_{\mathrm{c}}]+\{u_{\mathrm{c}}\}\end{cases} \tag{10}$$

where: u_{a}, u_{b} and u_{c} – three-phase reference voltages before injecting zero-sequence voltage, $[u_{\mathrm{a}}]$, $[u_{\mathrm{b}}]$ and $[u_{\mathrm{c}}]$ – rounded down integer parts of u_{a}, u_{b} and u_{c}, $\{u_{\mathrm{a}}\}$, $\{u_{\mathrm{b}}\}$ and $\{u_{\mathrm{c}}\}$ – positive decimal parts of u_{a}, u_{b} and u_{c}.

For carrier-based PWM, the output phase voltage only changes between two adjacent voltage levels in a switching period, so the instantaneous value of phase voltage can only be $[u_{\mathrm{x}}]E$ or $([u_{\mathrm{x}}]+1)E$. The common-mode voltage in a switching period is described in Fig. 3. It has four values: $\frac{[u_{\mathrm{a}}]+[u_{\mathrm{b}}]+[u_{\mathrm{c}}]}{3}E$, $\frac{[u_{\mathrm{a}}]+[u_{\mathrm{b}}]+[u_{\mathrm{c}}]+1}{3}E$, $\frac{[u_{\mathrm{a}}]+[u_{\mathrm{b}}]+[u_{\mathrm{c}}]+2}{3}E$ and $\frac{[u_{\mathrm{a}}]+[u_{\mathrm{b}}]+[u_{\mathrm{c}}]+3}{3}E$. Owing to $u_{\mathrm{a}}+u_{\mathrm{b}}+u_{\mathrm{c}}=0$, then $\{u_{\mathrm{a}}\}+\{u_{\mathrm{b}}\}+\{u_{\mathrm{c}}\}$ can be 1 or 2 and so $[u_{\mathrm{a}}]+[u_{\mathrm{b}}]+[u_{\mathrm{c}}]$ can be -1 or -2. All the possible common-mode voltages are summarized in Table 2.

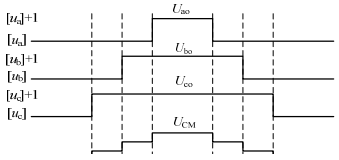

Fig. 3 Generation of common-mode voltage

After injecting zero-sequence voltage, the situation is more complex, because the sum of u_{a}', u_{b}' and u_{c}' is no more zero, hence the sum of $[u_{\mathrm{a}}']$, $[u_{\mathrm{b}}']$ and $[u_{\mathrm{c}}']$ has many possible values. Since $-2\le u_{\mathrm{x}}'\le 2$, the minimal value of $[u_{\mathrm{a}}']+[u_{\mathrm{b}}']+[u_{\mathrm{c}}']$ can reach –6 and the maximal value can reach 4. When applying the proposed zero-sequence voltage injection method, one of the three reference phase voltages is an integer, so the common-mode voltage in a switching period has three values. All the possible common-mode voltages are summarized in Table 3.

Table 2. Possible common-mode voltages without zero-sequence voltage injection

$[u_{\mathrm{a}}]+[u_{\mathrm{b}}]+[u_{\mathrm{c}}]$	Common-mode voltages
-1	$-E/3$, 0, $E/3$, $2E/3$
-2	$-2E/3$, $-E/3$, 0, $E/3$

Form table 2 and table 3 it can be seen that the amplitude of common-mode voltage without zero-sequence voltage injection is $2E/3$ and is increased to $2E$ after zero-sequence voltage injection. In order to limit the amplitude of

the common-mode voltage, the range of injected zero-sequence voltage must be limited. However, too narrow range of zero-sequence voltage will also make the DC-link volatge balancing effect poor.

Table 3. Possible common-mode voltages after zero-sequence voltage injection

$[u'_a]+[u'_b]+[u'_c]$	Common-mode voltages
-6	$-2E$，$-5E/3$，$-4E/3$，
-5	$-5E/3$，$-4E/3$，$-E$
-4	$-4E/3$，$-E$，$-2E/3$
-3	$-E$，$-2E/3$，$-E/3$
-2	$-2E/3$，$-E/3$，0
-1	$-E/3$，0，$E/3$
0	0，$E/3$，$2E/3$
1	$E/3$，$2E/3$，E
2	$2E/3$，E，$4E/3$
3	E，$4E/3$，$5E/3$
4	$4E/3$，$5E/3$，$2E$

(11) $$-3 \le [u'_a]+[u'_b]+[u'_c] \le 1$$

Experimental Results

A low power three-phase 5L-ANPC inverter prototype has been built up to verify the proposed control method. Infineon IGBT module BSM75GB120DN2 is used as the power semiconductor switch. The DC-link capacitor is 500 μF and the floating capacitor is 1 mF. The switching frequency is 2 kHz and the DC-link voltage is set at 120V.

Fig. 4 shows the output phase current and phase to phase voltage and Fig. 5 depicts the voltages of floating capacitors. It can be seen that all the three-phase floating capacitors are regulated at their reference voltage and the ripple amplitude is limited within 2 V.

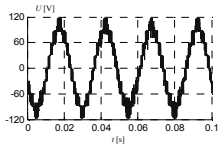

Fig. 4. Phase current and phase to phase voltage

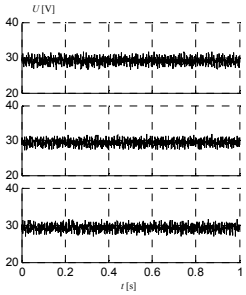

Fig. 5. Three-phase floating capacitor voltages

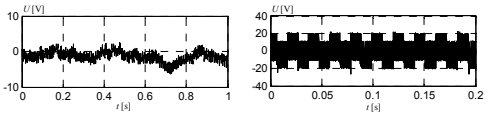

Fig. 6. NP potential and common-mode voltage without zero-sequence voltage injection

Fig. 6 is the experimental results of NP potential U_{NP} and common-mode voltage U_{CM} when the DC-link voltage balancing method is not used. When the DC-link voltage balancing method is utilized, the experimental results are shown in Fig. 7 and Fig. 8. Fig. 7 is the experimental result when the range of zero-sequence voltage is not limited.

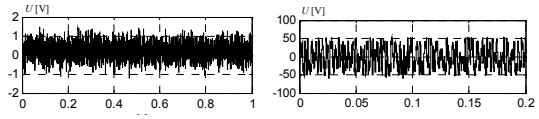

Fig. 7. NP potential and common-mode voltage with unlimited zero-sequence voltage injection

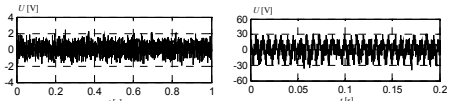

Fig. 8. NP potential and common-mode voltage with proposed DC-link voltage balancing method

When limiting the range of injected zero-sequence voltage with formula (11), the experimental results is shown in Fig. 8. The offset in the NP potential is also eliminated completely and the voltage ripple is slightly inceased to 2 V. But the common-mode voltage is reduced to 30 V.

Conclusions

This paper has presented a DC-link voltage balancing method based on zero-sequence voltage injection. By selecting some key zero-sequence voltages and calculating their corresponding average NP currents, the most appropriate zero-sequence voltage can be selected to generate the demanded NP current. By limiting the range of the injected key zero-sequence voltage, the common-mode voltage is reduced to 1/4 of the DC-link voltage. Experimental results demonstrat the validity of this method.

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