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Data mining based algorithm for analog circuits fault diagnosis

Abstract. *The paper deals with feature selection of testing signals used for fault-driven analysis of analog circuits based on some grey systems properties. Simple two stages fault diagnostic strategy for circuits with limited access to internal nodes is presented, illustrated with the examples and discussed. Algorithm enabling to detect and localize single and multiple catastrophic faults, is prepared under assumption, that input data sets are extracted from DC analysis.*

Streszczenie. *W artykule przedstawiono dwuetapowy algorytm detekcji I lokalizacji pojedynczych i wielokrotnych uszkodzeń układów analogowych, oparty o pewne techniki drążenia danych i elementy teorii systemów szarych. Założono ograniczony dostęp do punktów wewnętrznych oraz możliwość analizy dynamicznej i stałoprądowej badanych układów. (**Diagnostyka układów analogowych z wykorzystaniem technik drążenia danych.**).*

Keywords: fault diagnosis, feature selection, tolerance , catastrophic faults, grey systems theory
Słowa kluczowe: diagnostyka uszkodzeń, selekcja cech, tolerancja, uszkodzenia katastroficzne, teoria systemów szarych

Introduction

Fault diagnosis of analog electrical circuits with elements tolerances included seems to be still an important part of modern modeling, designing and manufacturing process. Basically, there exist two main methods for taking into account the parameters variations: direct one, based on the tolerance regions calculations [1] and indirect, grounded on the use of particular classifiers including tolerance in the learning stage of pattern recognition process. Most recently, the algorithms using some ideas of grey relational data analysis [2], introduced by Deng Julong, widely applied in economics, industry and agriculture were introduced also to the analog circuit fault diagnosis. Mentioned above, indirect methods enabling us to investigate circuits with parameters variations, need very large data sets. Data mining techniques called feature selection seem to be one of the most important methods for dealing with this problem [3]. This paper deals with feature selection of testing signals used for fault-driven analysis of analog circuits based on some grey systems properties. Simple two-stage fault diagnostic strategy for circuits with limited access to internal nodes is presented, illustrated with the examples and discussed. Algorithm enabling to detect and localize single and multiple catastrophic faults, is prepared under assumption that input data sets are extracted from DC analysis and time variant signals.

Ranking list classifier

Let us consider the set of data followed from circuit under test measurements:

$$x_j^k \in \mathrm{X}, \quad j = 0,1,2,...,M,\ k = 1,2,.....N \tag{1}$$

where N is a number of features (attributes) defined for the circuit under test, M – number of all investigated states of the circuit, including nominal one, x_j^k denotes k-th feature of the investigated j-th circuit state. Than, for all *M* circuit states (M-1 faults and golden state) we define rational degree [4] between CUT (circuit under test) series x_o^k and reference series $x_j^k, j = 1,2,....,M$:

$$\mathbf{\Gamma}_j = \sum_{k=1}^{N} a_k \rho_{jk} \tag{2}$$

where

$$\mathbf{A} = \left[a_1\ a_2 ... a_N\right]^T, \qquad a_i \in \left[0,1\right), \sum_{i=1}^{N} a_i = 1, \tag{3}$$

denotes the vector of weight coefficients.

The relational coefficient ρ_{jk} for k-th feature at j-th state is defined by the formula:

$$\rho_{jk} = \frac{\mu_o + \omega\eta_o}{\left|x_o^k - x_j^k\right| + \omega\eta_o}, \quad \omega \in (0,1) \tag{4}$$

$$\mu_o = \min_j \min_k \left|x_o^k - x_j^k\right|, \eta_o = \max_j \max_k \left|x_o^k - x_j^k\right|$$

where ϖ is the heuristic coefficient enabling us to improve effectiveness of the procedure.

If all the selected features have the same impact on the computations of similarity measure we may set

$$a_i = \frac{1}{N}, i = 1,2,...,N \tag{5}$$

hence formula (2) should be rearranged into the following form

$$\Gamma_j = \frac{1}{N}\sum_{k=1}^{N} \gamma_{jk}\ . \tag{6}$$

Ranking list procedure, based on grey relational analysis consists on calculations of all rational coefficients (2) for particular circuit fault. The biggest value of grey relational degree indicates the pattern of defined state (fault or faulty free circuit).

Numerical experiments confirmed that direct use of proposed calculations scheme is very fast and effective only for single catastrophic faults of the simple analog circuits. To improve efficiency and discriminatory power of the method the special simply algorithm was invented. It is based on the auxiliary matrix $\mathbf{\Gamma}^0(\mathbf{A})$:

$$\mathbf{\Gamma}^0(\mathbf{A}) = \begin{bmatrix} \Gamma_{11}^0 & \Gamma_{12}^0 & \dots & \Gamma_{1M}^0 \\ \Gamma_{21}^0 & \Gamma_{22}^0 & \dots & \Gamma_{2M}^0 \\ \dots & \dots & \dots & \dots \\ \Gamma_{M1}^0 & \Gamma_{M2}^0 & \dots & \Gamma_{MM}^0 \end{bmatrix} \tag{7}$$

where each j-th column (j=1,2,…,M) represents the relational degree of CUT in terms of the reference set of features (testing points) for nominal values of the defined state used as testing fault

(8)
$$x_o^k = x_j^k,\ k = 1,2,...,N,$$
$$for\ \ j = 1,2,...M.$$

Note, that $\Gamma_{ii}^0 = 1\ i = 1,2,...,M$.

The matrix (7) depends on the vector of weight coefficients (3). We are interested in finding the vector **A** (3) ensuring that the distance between second highest value of each column and the highest one is large enough to preserve discriminatory power of the proposed algorithm. This is adequate to find the maximum of the function

(9) $$\overline{\Delta}(\mathbf{A}) = \min_i \Delta_i(\mathbf{A})$$

where

(10)
$$\Delta_i = abs(1 - \max_{\substack{j=1,2,...,M \\ j \neq i}} \Gamma_{ij}^0),$$
$$i = 1,2,...,M$$

Preselecting attributes

The problem of choosing the set of features proper for our faults classifier seems to be unsolved globally. There may be no substitute for trying all possible features and seeing how well the resulting algorithm works. However, there exist some data mining tools enabling us to indicate single features which are likely to have good discriminatory power (called feature selection) or linear combinations of features with the same aim (feature extraction) [6]. Forwards selection and backward elimination belong to the simplest selection strategies. The first one adds a feature at a time, at each stage choosing the addition that most increases the separation measure. The second one starts with all features and at each step drops the attribute whose presence least increases used measure. It can be also possible to find a subset which is guaranteed to be the best of assumed size without considering all the subset by the technique of branch-and-bound. Most feature selection change the set of features by adding or deleting a single feature at a time. The described beneath approach may use all features simultaneously. It enable us to estimate quality of the selected feature subsets using computer simulations performed for given circuit faults with randomly chosen values of elements parameters limited by the known tolerance. Computed data sets seem to be better if classes (data sets defining circuit states) are compact and well separated. Between-class average distance and within-class dispersion [7] have been commonly used to valuate quality of the data sets. Modified versions of the mentioned measures [8] are based on the formula

(11) $$D_f^{(i,j)} = \frac{1}{m_i m_j} \sum_{s=1}^{m_i} \sum_{t=1}^{m_j} \left\| x_f^{(i,s)} - x_f^{(j,t)} \right\|^2$$

describing average between-class distance along f coordinate (subscript f indicates the feature, superscripts i and j denote circuit fault, whereas s and t indicate number of Monte Carlo analysis). Average between-class distance has the following form

(12) $$F_{BC}(k) = \sum_{f=1}^{NF} w_f^{(k)} \left(\sum_{i=1}^{L} P(X_i) \sum_{\substack{j=1 \\ j \neq i}}^{L} P(X_j) D_f^{(i,j)} \right)$$

whereas average within-class data dispersion is given by

(13) $$F_{WC}(k) = \sum_{f=1}^{NF} w_f^{(k)} \sum_{j=1}^{L} P(X_j) D_f^{(i,j)}\ .$$

$P(X_i)$ represents known a priori class probability, $w_f^{(k)}$ is a weight coefficient having value one for the f-th combination of features, if f-th feature is present in the current feature subset (otherwise zero). This coefficient enable us to perform optimization procedure based on the following fitness function:

(14) $$F(cfs) = \frac{F_{BC}(cfs)}{F_{WC}(cfs)}$$

where *cfs* denotes combination of features chosen from all possible.

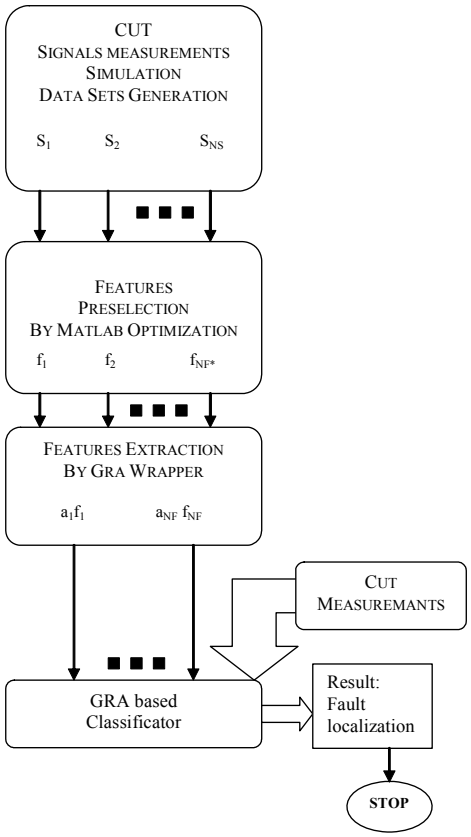

Fig.1. Schematic presentation of diagnostic algorithm using feature preselection and GRA based wrapper.

Algorithm and numerical example

Using described in the previous sections concepts we may formulate simple faults classifier (see diagram presented in Fig.1). Before test step based on modified Malina [7] concept (see equations (11)-(14)) selects features for further classification. Ranking list classifier using GRA approach, consists of two optimization stages. First, using defined earlier matrix (7) and function (9) with binary type of weight vector, we apply the Matlab GA procedure with bit string population type. As the result, the subset of features ensuring maximum value of (10) for each column is obtained separately. Next, using selected attributes we perform again GA optimization technique applying fitness function based on rational degree matrix calculated with use of the formulas (2)-(3). Using double vector population type, fitness function (9) with additional linear equality (see formula (3)) we obtain final GRA based classifier. For every CUT measurements we are using the set of nominal measurements at chosen points and weight vector (3) The highest value of calculated rational degree(2) indicates the recognized fault.

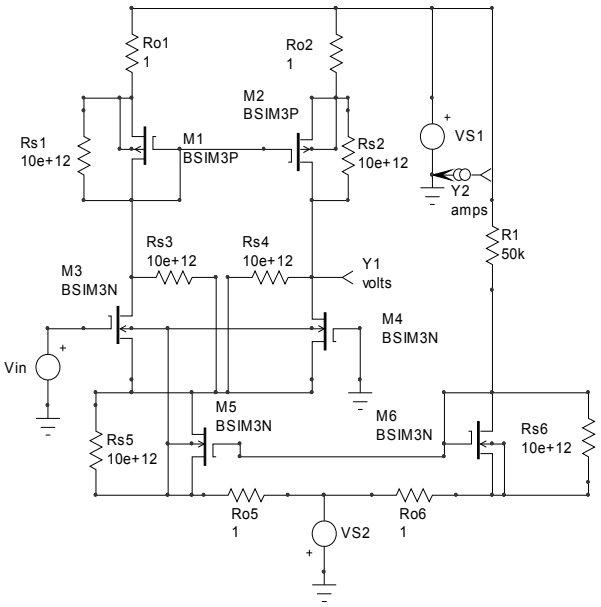

Fig.2. CMOS operational amplifier under test.

To illustrate proposed procedure let us consider an exemplary CMOS circuit presented with modelled faults in Fig.2 (Vs1=5V, Vs2=5V, BSIM3N L=3μ, W=3μ, BESIM3P L=9μ, W=3μ). Preliminary set of features (testing points) contains DC output voltage (Y1 point) and DC supply voltage current (point Y2) monitoring for different values of DC input voltage V_{in} and combinations of supply voltages (V_{s1}, V_{s2}). Additionally, transient responses due to input pulse generator signal (output voltage and supply voltage current) were analysed by use of DWT (fault pattern was calculated according to commonly use formulas [9]).

Table I. Set of measurements for test circuit of Fig.1

Circuit State	Measurements				
	Y1 for Vin=-2V [V]	Y1 for Vin=-1V [mA]	Y2 for Vin=-1 [mA]	Y1 for Vin=1 [V]]	Y1 for V_{in}=2 [V]
Nominal	-3.8078	-2.9998	-0.0004	3.2352	3.5216
R1 short	-3.8068	-2.9999	-0.0005	3.2160	3.4976
R1 open	2.8864	2.8864	-0.0000	4.9970	4.9843
M1 D-S short	4.4974	-4.2029	-0.0004	-3.5512	-3.1976
M2 D-S short	4.9998	4.9998	-0.0004	4.9999	4.9999
M3 D-S short	4.2887	4.2887	-0.0005	4.2887	4.2887
M4 D-S short	-4.2601	-3.8383	-0.0004	-2.9030	-2.6036
M5 D-S short	-4.0969	-3.3763	-0.0005	-1.1122	-0.6121
M6 D-S short	4.5950	4.5950	-0.0020	4.9466	4.9748
M1and M2 stuck-off	-5.000	-5.000	-0.0003	-5.000	-5.000

Preselection based on fitness function (14) reduced the set of attributes. Next, using GA optimization Matlab function with bit string population type we obtain the set of features listed in the Table 1. This stage ensure that all possible faults were distinguished. Finally, applying Matlab *optimtool GUI* procedure we calculate weight vector of the form

$$\mathbf{A} = \left[0.1\,0.2\,0\,0.4\,0.3\right]^T, \quad (15)$$

Efficiency of this simply multiclass ranking list algorithm was confirmed by use of test data sets generated under the assumption that tolerances of chosen parameters are as follows: $R1_{tol}$ =5%, W_{tol}=0.5%, L_{tol}=0.5%, $toxt_{tol}$ =1%.

Conclusion

To confirm efficiency of the described diagnostic procedure, many standard benchmark circuits containing bipolar and CMOS transistors were investigated. Numerical experiments performed by use of WinSpice3 integrated with Matlab simulator confirmed that, using DC analysis the proper localization of the single and multiple catastrophic faults of analog circuits is possible. Presented here very simple and fast two stage classifier using features filtering and wrapping, ensure enough effectiveness (close to 100% for tolerances not greater than listed above).

It should be mentioned that invented feature selection procedure, based on ranking list algorithm is also very good as a preprocessing stage for any, more complicated classifier, applied when higher tolerances of the parameters should be included.

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