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Optimization of the test conditions for fault detection in nonlinear analog circuits using supply current

Abstract. *In this paper, selection of the optimum test conditions for catastrophic fault diagnosis of analog circuits containing MOS transistors is presented. The method of fault detection applies power supply current waveform IDD as an indicator of a device feature. The stimulate signal parameters and values of additional components are changed in optimization process to extend variation between the test signals for considered faults. An illustrative numerical example is presented.*

Streszczenie. *W pracy przedstawiono dobór warunków testu w metodzie wykrywania i lokalizacji uszkodzeń katastroficznych w układach analogowych zawierających tranzystory MOS. W zastosowanym algorytmie detekcji uszkodzeń informacje o właściwościach układu są zakodowane w przebiegu prądu źródła, zasilającego obwód w stanie nieustalonym. Parametry sygnału pobudzającego i wartości dodatkowych elementów są modyfikowane w procesie optymalizacyjnym tak, by powiększyć różnice między sygnałami testowymi odpowiadającymi rozważanym uszkodzeniom. Działanie algorytmu zilustrowano na praktycznym przykładzie. (**Optymalizacja warunków testowych do wykrywania i lokalizacji uszkodzeń katastroficznych w nieliniowych układach analogowych**)*

Keywords: analog circuits, fault detection, discrete wavelet transform, feedforward neural network, optimization
Słowa kluczowe: układy analogowe, wykrywanie uszkodzeń, dyskretna transformacja falkowa, jednokierunkowe sieci neuronowe, optymalizacja

Introduction

Fault location and detection in electronic equipment is one of the fundamental problems in production of reliable and safe electronic multi-element systems [6], [7], [8]. For diagnosis of faults in numerical electronic devices, effective, automatic procedures have been worked out. Unfortunately, in diagnosis of analog circuits, any universal and dependable technique have not been determined yet, and therefore it is mainly based on engineers' experience [8].

The review of papers dealing with diagnosis problem [9], shows two basic types of faults: catastrophic and parametric are discussed. In case of catastrophic faults, which rely on short or open circuit, we deal with the problem of the change of circuit topology. Failures, in which there is no change of circuit topology and only values of parameters change, are called parametric faults. Both types of faults may cause improper functioning or even destruction of the system, therefore the precise fault diagnosis of the produced electrical devices is essential.

Monitoring the supply current (test IDDQ) is an effective diagnosis approach of digital CMOS. In order to overcome some limitations of this method, tracing the supply current in unsteady state, caused by a shock change of supply voltage [1], [10], was applied (test IDD).

The IDD transient response method performs a dynamic measurement of the power supply current when VDD is changed from a nominal value to a half of nominal value. Achievements, which this method brought to diagnostic investigations of digital devices, it to be used also for analog circuits testing. Yet, a great changeability of such circuits makes their diagnosis difficult and requires further studies [7].

In order to exposure changes of features of the device resulting from modification of parameters, test signals will be divided into elements by means of bank of filters formed with the use of discrete wavelet transform [2]. Having test signals divided into elements, in diagnosis process we use these which show the biggest sensitivity and also regularity over the change in value of device parameter.

Additionally, to stimulate oscillations of the supply current during the test, one should use extra components (eg. coils and capacitors), connected to external terminals [2] and one should modify shape of the excitation signal [3], [4], [5]. Due to both procedures, a test signal contains more information about the circuit.

The aim of this paper is to present that optimization of stimulate signal parameters and values of additional components significantly extends variation between the test signals measured for both damaged and undamaged devices. In this way efficiency of the procedure for fault recognitions is growing.

Selection of the test conditions

To measure of the transient supply current we need to set the tested circuit into an unsteady state. For this purpose at a zero, the V_{DD} value fell from the nominal value $5V$ to 0 during the time T like linear function, where T is in the range $[0, T_{max}]$. The voltage changes are illustrated in the Fig. 1.

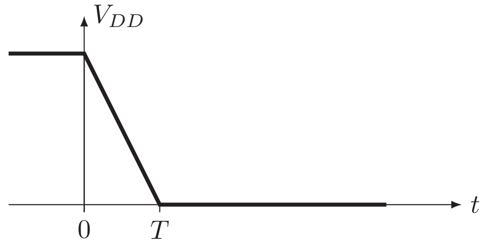

Fig. 1. V_{DD}

In order to enlarge sensitivity of the test signals for change of circuit parameters, one coil with inductance L has been mounted in series with power source. We assume that the inductance value may be in the range $[L_{min}, L_{max}]$.

Test signals preprocessing

In order to exposure changes of features of the device, resulting from modification of parameters, test signals (transient supply currents I_{DD}) are divided into elements by means of bank of filters formed with the use of discrete wavelet transformations. The wavelet with scale a and shifting b is the function given by the equation:

$$\psi_{ab}(t) = \frac{1}{\sqrt{a}}\,\psi\left(\frac{t-b}{a}\right) , \quad (1)$$

where ψ_{ab} represents the basic wavelet, ie. function determining type of the used wavelet transformation. Assuming $a = 2^m$ and $b = n2^m$, where m and n are natural numbers, determining the packet of wavelets being the basis of discrete wavelet transformation.

Each wavelet determines the pair of complementary filters, which divide the signal into two parts: the lower part of frequency band, ie. approximation and the upper part of

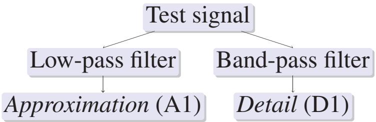

Fig. 2. The test circuit

frequency band, ie. details. The approximations are the high-scale, low-frequency components of the signal. The details are the low-scale, high-frequency components. The filtering process, at its most basic level, is shown below in the Fig. 2

The decomposition process can be iterated, so that one signal is broken down into many components. This task is performed by some filters constituting a complementary set. Such filters, and a five level division of the signal is illustrated by decomposition tree given in the Fig. 3

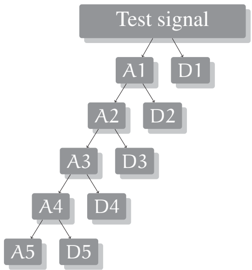

Fig. 3. The test circuit

After dividing test signals into elements, one of them is used in diagnosis process. The chosen element should show the biggest sensitivity and also regularity over the change in value of device parameter.

Neural network

It is assumed that an artificial feedforward neural network is an algorithm, and its basic component, called neuron, performs calculations given by the equation:

$$y = f\left(\sum_{i=0}^{lw} w_i x_i\right) \tag{2}$$

where numbers $x_0, x_1, \ldots, x_{lw}$ make input signal, $w_0, w_1, \ldots, w_{lw}$ are weight, modified at learning process, lw determines number of neuron inputs, $f(*)$ is a function called neuron activation function, and y is an output signal.

Neurons are arranged in layers. The first one, called *an input* layer is exceptional since it has no neurons, only input signals. The following layers, called *hidden*, contain neurons sending their own output signals to all neurons of the following layer. The last layer, called the output, produces the output signals of the whole network. An example of the construction of an artificial neural network is shown in the Fig. 4.

Input vectors of the neural network, used for learning to recognize the parametric fault, are made in the following way: At the beginning, test signals are determined for different values of the tested components. These values of parameter of the chosen component are modified to cover evenly the whole range of changes, which should be taken into account. Next, using a wavelet filter bank, the tested signals are divided into elements. The most precise element, showing regular changes together with the change of the parameter, is chosen.

Appropriately selected samples of the chosen component (approximation or detail) of power supply current waveform I_{DD} will be used as input signals of neural networks.

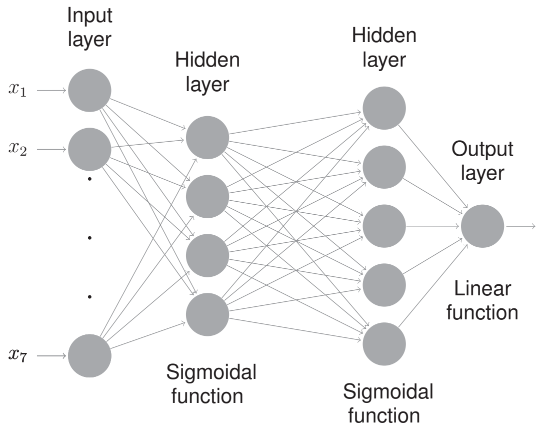

Fig. 4. Neural network

Optimization

The supply current $i_F^{(i)}$, calculated for the faulty device number i, is compared to the analogue current i_G obtained from the standard one. The measure of the difference between these quantities is calculated from the formula

$$R_i(T, L) = \sqrt{\frac{1}{N}\sum_{k=1}^{N}\left(i_F^{(i)}(T, L, t_k) - i_G(T, L, t_k)\right)^2}\ , \tag{3}$$

where N denotes a number of current samples, and t_k designates the sample number.

Time T and inductance L are elected as the set of the optimization parameters. Objective function, which will be minimized, has the form

$$Q(T, L) = \sum_{i=1}^{B} \frac{w_i}{R_i(T, L)}\ , \tag{4}$$

where w_i ($i = 1, 2, \ldots, B$) signifies weight, which is selected in a special way.

We assume that elected parameters have constraints $T \in [0, T_{max}]$ and $L \in [L_{min}, L_{max}]$.

Let by $\mathbf{x}$ denote the vector $\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} T \\ L \end{bmatrix}$.

There are inequalities arising from constraints for $\mathbf{x}$

$$\begin{aligned} -x_1 &\leq 0 \\ x_1 &\leq T_{max} \\ -x_2 &\leq -L_{min} \\ x_2 &\leq L_{max}\ . \end{aligned}$$

In the matrix notation we have

$$\begin{bmatrix} -1 & 0 \\ 1 & 0 \\ 0 & -1 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \leq \begin{bmatrix} 0 \\ T_{max} \\ -L_{min} \\ L_{max} \end{bmatrix} .$$

Let

$$\mathbf{A} = \begin{bmatrix} -1 & 0 \\ 1 & 0 \\ 0 & -1 \\ 0 & 1 \end{bmatrix} \quad \text{and} \quad \mathbf{b} = \begin{bmatrix} 0 \\ T_{max} \\ -L_{min} \\ L_{max} \end{bmatrix} .$$

Solution of the task requires finding a local minimum $\mathbf{x}$ to the function $Q(\mathbf{x})$, subject to the linear inequalities $\mathbf{Ax} \leq \mathbf{b}$.

Example

The circuit, shown in the figure 5, was chosen as an example.

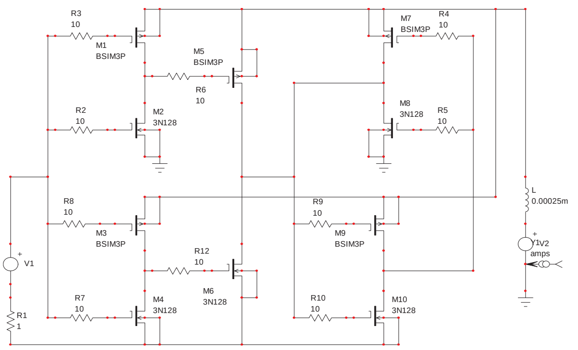

Fig. 5. The test circuit

The circuit response was calculated using ICAP4 simulator with employing Gummel-Poon transistor model. The application in learning process of test signals coming from the circuits, which parameters change within tolerance limits, enables to consider variations of elements occurring in practice.

The process of decomposition of test signals was made according to the scheme given in the Fig. 3. To calculate wavelet transformation, the wavelet db10 was used. The detail at the level 8 of power supply current waveform was used as a test signal in the presented example.

For optimized parameters, the following constraints were used: $T_{max} = 50ns$, $L_{min} = 0.1\mu H$ and $L_{max} = 0.3\mu H$.

Search for $\mathbf{x}$, that minimizes the function $Q(\mathbf{x})$, was carried out using genetic algorithm. The employed genetic procedures come from MATLAB. As a result of the calculation $T = 10.4ns$ and $L = 0.251\mu H$ was received.

The Fig. 6 shows the change of the test signal from the damaged and undamaged circuit when the V_{DD} voltage changes like step function ($T = 0$). In the damaged circuit, short circuit of transistor M6 was assumed.

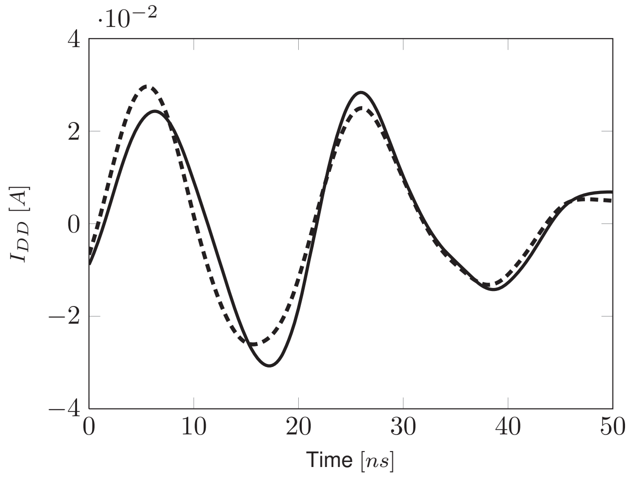

Fig. 6. The $D8$ component of the transient supply current I_{DD} in damaged (solid line) and undamaged (dashed line) circuit, whereas $T = 0$ and $L = 0.251\mu H$

Neural network learning was impossible with these test signals. Fig. 7 shows the corresponding test signals as Fig. 6 but using the optimal $T = 10.4ns$.

In this case, the neural network can correctly recognize the fault.

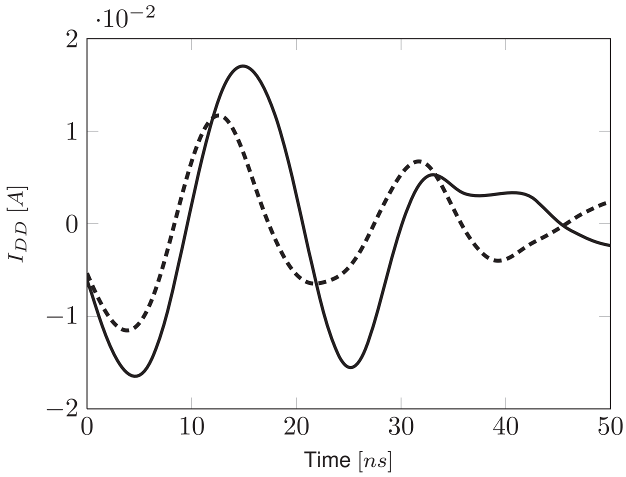

Fig. 7. The $D8$ component of the transient supply current I_{DD} in damaged (solid line) and undamaged (dashed line) circuit, whereas $T = 10.4ns$ and $L = 0.251\mu H$

Conclusions

The employment of the optimization procedure to match the test conditions (time T and inductance L) significantly extends differences between supply currents, calculated for both damaged and undamaged devices. Due to the use of the optimization procedure, number of the catastrophic faults recognized in tested devices is growing.

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