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DSP Based Hardware Implementation of Repetitive Current Controller for Interleaved Grid Connected Inverter

Abstract. *The performance of the repetitive controller (RC) for classical inverters (e.g. two-level LCL filter based inverter) can decline if the system bandwidth is not sufficient enough due to much larger LCL filter component values. The novel interleaved inverters can provide higher bandwidth than the classical inverters because of low filter values. This paper reflects upon the analysis and hardware implementation of the RC for interleaved inverter using DSP. High quality (very low THD) output current is demonstrated through simulation and experimental results.*

Streszczenie. *W artykule przedstawiono analizę i implementację na DSP sterowania powtarzalnego dla badanego falownika typu interleaved. Przedstawione wyniki badań symulacyjnych, pokazują wysoką jakość (niskie THD) prądu wyjściowego przekształtnika. (**Implementacja sterowania powtarzalnego na DSP dla przekształtnika sieciowego typu interleaved**).*

Keywords: Interleaved inverter, total harmonic distortion (THD), repetitive control (RC), digital signal processor (DSP)
Słowa kluczowe: falownik interleaved, THD, sterowanie powtarzalne, DSP.

Introduction

The power electronic inverters have been widely employed as the interface between distributed generators and the grid. There exist different types of power electronic inverters for interfacing with the grid [1]. The most common is the two-level bridge inverter. However, there is always requirement of improved efficiency and low cost. This has encouraged researchers to look into alternative topologies. Many multilevel inverters have been proposed. These inverters have the advantage of reducing the voltage step changes at the expense of increased complexity and cost of the power electronics and control components. An alternative to the multilevel inverter is to use an interleaved inverter topology (as shown in Fig. 1), which in effect comprises several low power, high frequency, multilevel bridge inverters connected in parallel. Since, there exists current ripple cancellation phenomena because of the interleaving topology, therefore only small capacitors are required that will provide high impedance to the grid and higher bandwidth for designing controller [2].

In grid connected mode of operation, it is desired to have pure sinusoidal current (clean current without harmonics) as much as possible without any distortions. Conventional classical controllers have been widely used for grid connected inverters but they were found not to provide output current as per the required standards when the grid voltage harmonic distortion is high [3]. This is due to periodic nature of the disturbances in this application. Actually classical controllers are not suitable for periodic input reference tracking. Hence, alternative controller is required. Repetitive controller (RC) is good choice due to its ability to track or reject periodic inputs. The concept of the iterative learning control (ILC) algorithm is the pioneer for the design of the repetitive feedback controller. RC utilizes the difference between the reference value and the feedback grid connected on a cycle-to-cycle basis in contrast to other controllers.

This paper makes novel contribution by analysing RC for interleaved inverters using computer simulations and hardware. Practical realisation of RC is proposed by considering different ways of implementations using DSP. The design of the RC takes into account practical constraints of the DSP hardware and system bandwidth limitations. The sampling time and computational time delay taken by the DSP for experimental implementation has been considered. Moreover, for implementation of RC and digital filters, two forms such as direct form I and direct form II will be discussed. Finally, experimental results are presented to validate the design and method. The system components are shown in Table 1. The Overall single-phase block diagram of the interleaved grid connected inverter and its controller is shown in Fig. 2.

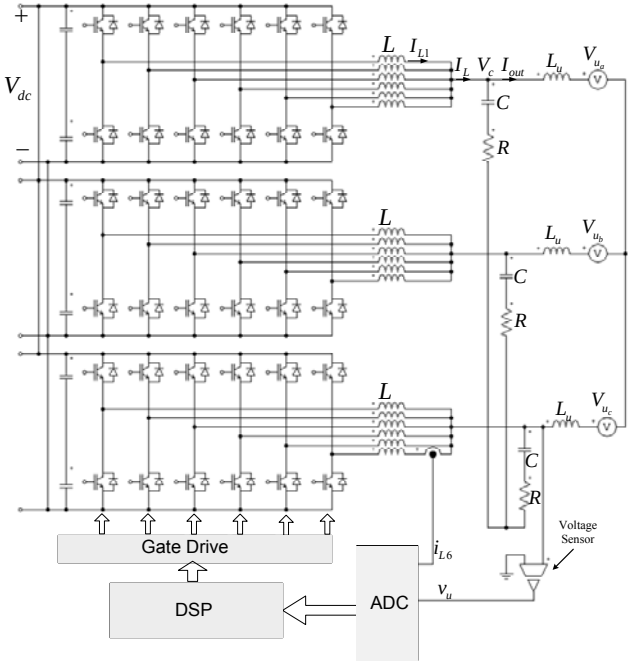

Fig. 1. Three-phase interleaved grid connected inverter-showing control of one channel of single phase

Table 1. Component values

Description	Symbol	Value
Grid phase voltage	V_u	230 V (rms)
DC link voltage	V_{dc}	700 V DC
Passive damping resistance	R	0.5 Ω
Number of channels	N_o	6
Channel inductor	L	190 µH
Grid inductance	L_u	5-50 µH
Filter capacitance	C	10.8 µF
Switching frequency	f_s	35 KHz
Grid frequency	f	50 Hz
Time delay	T_d	15µs
No. of samples per period	N	700
Maximum rated current	I_{Out}	90 A (rms)

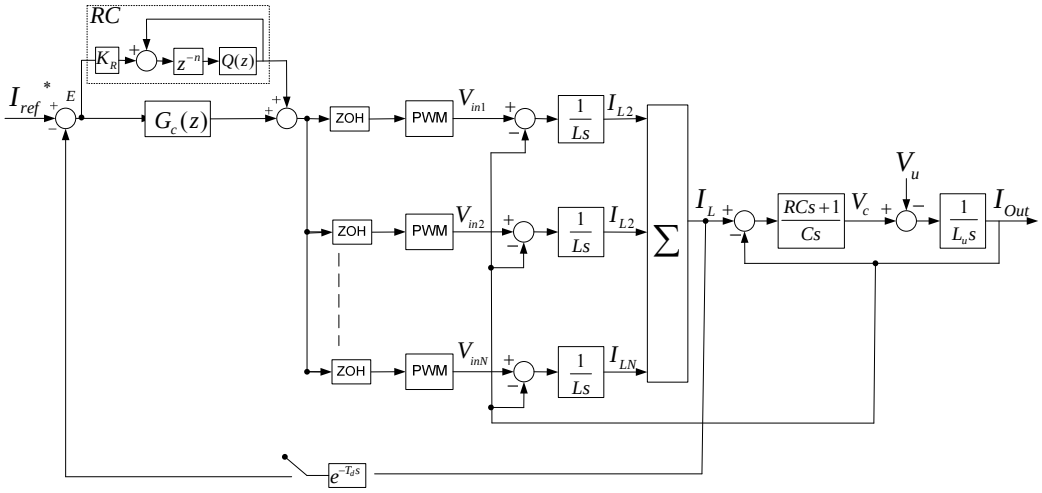

Fig. 2. Overall single-phase block diagram of the interleaved grid connected inverter and its controller

1) Proposed Control Scheme

The proposed controller incorporates a conventional feedback current controller, and a feed forward loop of the grid voltage, in addition to the repetitive feedback loop as shown in Fig. 2. For analysis purpose, if we consider inputs $I_{ref}^* = R(z)$, $V_u = D(z)$ and the output $I_{out} = Y(z)$, then the simplified diagram of system with proposed control scheme can be represented using Fig. 3. The overall transfer function of system is given by:

$$\frac{Y(z)}{R(z)} = \frac{\left(1+G_{RC}(z)\right)G_c(z)G_P(z)}{1+\left(1+G_{RC}(z)\right)G_c(z)G_P(z)} \quad (1)$$

where, $G_{RC}(z)$ is the transfer function of RC, $G_c(z)$ is the transfer function of the conventional feedback controller and $G_p(z)$ denotes the transfer function of plant i.e. interleaved inverter with respect to reference voltage. Similarly, $G_d(z)$ is the disturbance transfer function, I_{L_x} is inductor current in any channel and $V_f(z)$ is feedforwrad voltage in Fig. 3.

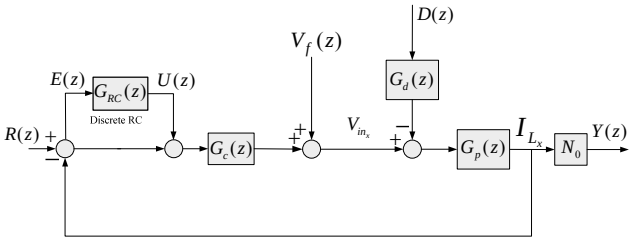

Fig. 3. The simplified general diagram of the system with proposed control scheme

The open loop transfer function of interleaved inverter (plant) with respect to reference voltage V_{in} and disturbance V_u can be following [2]:

$$G_p(s) = \frac{I_L}{V_{in}} = \frac{L_u Cs^2 + RCs + 1}{LL_u Cs^3 + Rc(L+N_o L_u)s^2 + (L+N_o L_u)s} \quad (2)$$

$$G_d(s) = \frac{I_L}{V_u} = \frac{RCs+1}{LCs^2 + RCs + 1} \quad (3)$$

It should be noted here, that the DSP computational time need to be modelled. For this purpose, the time delay T_d is modelled as $e^{-T_d s}$. That is equal to half of the sampling period i.e. $T_d = 0.5T_s$. The Zero Order Hold (ZOH) blocks represent analog to digital converetrs.In the digital domain, $G_P(z)$, can be obtained by considering zero order hold effect, and performing the Z-transform of the $G_P(s)$. Matlab can be used for this purpose.

$$G_p(z) = z\left[\frac{1-e^{-T_s s}}{s} e^{-T_d s} G_p(s)\right] \quad (4)$$

a. Conventional Tracking Controller

It is one of basic requirement that the system with conventional tracking controller should be stable enough to have add-on loop of RC in the next step. For this purpose, a simple proportional controller with phase-lag is designed and given by equation (4). The detail can be seen in [3].

$$G_c(z) = 10\frac{0.5z - 0.35}{z - 0.97} \quad (5)$$

The said controller has been tested against different values of grid impedance L_u. The system always has good positive margins as hwon in Fig.4.

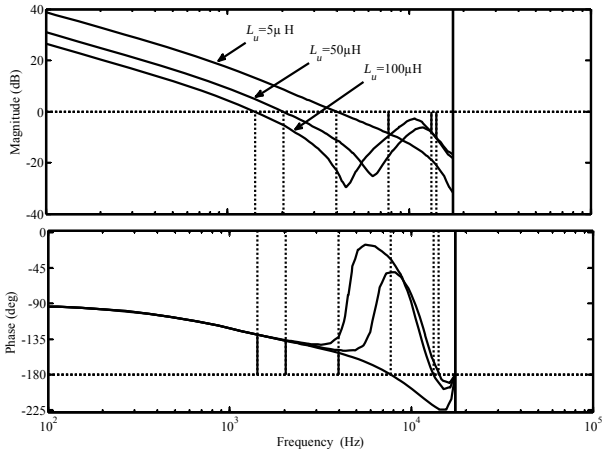

Fig. 4. Bode plot of the system with conventional tracking controller $G_c(z)$ against grid impedance variations

It is worthwhile to mention here, that this classical controller has certain limitations such as further enhancement in gain. This reuslts in low capability of rejecting higher harmonics. These limitations can be overcome by introducing RC. This is discussed in next section.

b. Repetitive Controller (RC)

The RC is applied in the discrete time domain with a sampling period T_s, the discrete periodic signal generator ($z^{-N}/1-z^{-N}$) is included in the loop. Here, *N* is the number of samples per period and is defined as the ratio of time period (T_p) to the sample period (T_s). The RC is implemented in a plug-in fashion as shown in Fig. 2 and Fig.3. The transfer function of RC is given by,

$$G_{RC}(z)=\frac{K_R Q(z) z^{-N}}{1-Q(z)z^{-N}} G_f(z) \tag{6}$$

Here $Q(z)$ is a low pass filter, $G_f(z)$ is the compensator and K_R is the gain of the RC. It is out of scope of this paper to discuss the detail of all these parametrs. This can be seen in [4].

By subsitutuing all transfer fucntion is equation (1), the overall transfer function w.r.t. reference is:

$$\frac{Y(z)}{R(z)}=\frac{\left(1-Q(z)z^{-N}+K_R Q(z)z^{-N}G_f(z)\right)G_o(z)}{1-Q(z)z^{-N}\left(1-K_R G_f(z)G_o(z)\right)} \tag{7}$$

where, $G_o(z)=\dfrac{G_c(z)G_p(z)}{1+G_c(z)G_p(z)}$

Similarly, the overall transfer function w.r.t. disturbance can be following:

$$\frac{Y(z)}{D(z)}=\frac{1-Q(z)z^{-N}}{\left(1+G_c(z)G_p(s)\right)\left(1-Q(z)z^{-N}(1-K_R G_f(z)G_o(z))\right)} \tag{8}$$

Now the overall error transfer function can be following:

$$G_E(z)=\frac{E(z)}{R(z)-D(z)}=\frac{1}{1+\left(1+G_{RC}(z)\right)G_c(z)G_P(z)} \tag{9}$$

By putting all values in above equation, we have:

$$G_E(z)=\left(\frac{1-Q(z)z^{-N}}{\left(1+G_c(z)G_p(z)\right)}\right)\left(\frac{1}{1-Q(z)z^{-N}\left(1-K_R G_f(z)G_o(z)\right)}\right) \tag{10}$$

The above equation can be used to define stability condition of RC. Clearly, closed loop system without RC should be stable and magnitude of $Q(z)\left(1-K_R G_f(z)G_o(z)\right)$ should be less than unity.

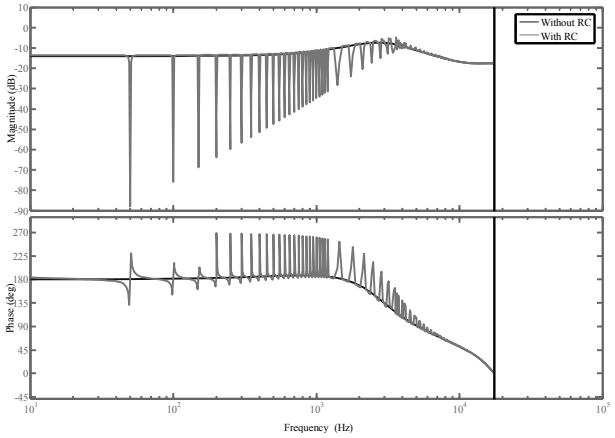

Fig. 5. Frequency response of the disturbance transfer function

To show the effectiveness of RC, the frequency repsonse of the disturbance transfer function is shown by Fig.5. It can be easily obsreved that all harmonics are suppressed by high value of gains using RC. Now implementaion of RC is discussed in next section.

2) Implementation of RC

The procedure of experimental implementation of the RC based current controller for the interleaved grid connected is explained in this section. Fig. 6. represents the block diagram of the control system for one channel of single phase. Implementation of the proposed controller is done using the Texas Instrument TMS320LF2808 digital signal processor (DSP), which is a fixed-point 32-bit digital signal processor with 16 analog-to-digital (ADC) channels that can be used for current and voltage sensing. This processor comes with code composer software that comprises a C-complier, an assembler and a debugger.

It should be noted here that the overall system has six current sensors for measuring the current in each channel in a single-phase and one voltage sensor to measure the voltage at the point of common coupling. Therefore, there are a total of seven control signals in a single-phase in addition to the twelve switching signals. This can be seen in the basic hardware configuration as shown in Fig. 6. It is one of basic requirement that the system with the conventional tracking controller should be stable enough to have add-on loop.

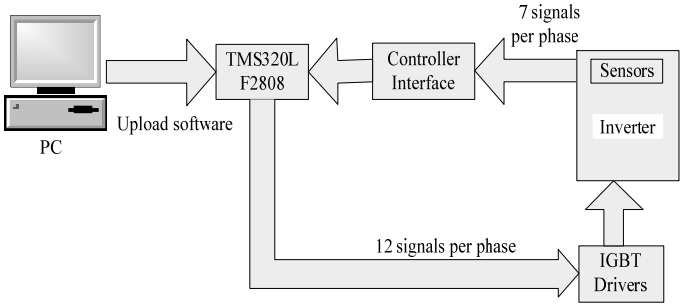

Fig. 6. Basic hardware configuration for single-phase

a. Hardware Description

The schematic diagram of the power circuit of the experimental apparatus is shown in Figure 7 and actual experimental test rig is shown in Fig. 8. The main components include isolation transformer, contractors (C1, C2 and C3), current limiting resistors, miniature circuit breaker (MCB) and a boost card with the interleaved inverter (test rig). These components are normally used for the protection of test rig. The protection devices are normally selected in such a way that the rated current of the protection devices is less than or equal to the maximum circuit current.

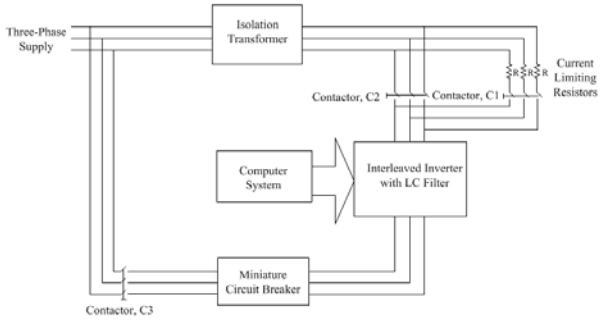

Fig. 7. Schematic diagram of the power circuit of the experimental apparatus

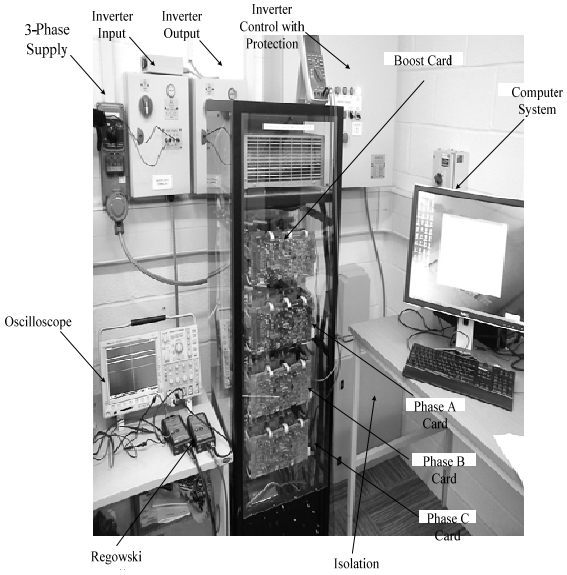

Fig. 8. Experimental test rig of the three-phase interleaved inverter

A DC supply is obtained by rectifying the grid three-phase AC supply. An isolation transformer is placed to provide galvanic isolation between the grid and the rectified DC supply. It is normally required for the balanced supply (grounding of the system) and safety reasons as well. The leakage inductances of the transformer windings can be beneficial for suppressing the PWM current ripples. However, these leakage inductances can be ignored, as they are small in nature. Instead, additional filter inductances are considered, which are sufficient for small current ripples due to the interleaved topology. The rectified DC voltage is then stepped up to the required DC link voltage of 750V using a boost circuit. The boost circuit also makes sure that this DC link voltage is in the range.

The contactors are installed for connection and isolation of the apparatus from the grid. At start-up, all the contactors should be in the open position. As the grid three-phase supply is connected by plugging the three-phase socket to the outlet, the isolating transformer is energised and the DC link capacitors are charged up through the current limiting resistors. The rectifier circuit requires slow pre-charging of the DC link capacitors. For this purpose, contactor C1 is first turned on.

The current limiting resistors are used for soft charging of the DC link capacitors. The MCB provide protection of the circuit against overloads and short circuits.

b. Development of RC Algorithm for DSP Impelmentation

The selection of suitable form in terms of the number of operations or storage elements for implementation is normally required. Additionally,numerical stability and fewer round-off errors are also desirable while implementing RC algorithm using DSP. For this purpose, initilaly a difference equation is obtained from the transfer function of the RC using Equation (6) and Fig. 9. This is normally done for every digital implementation case. For analysis, if we assume that $K_R = 1$ and $G_f(z) = 1$ in the RC transfer function, then the resultant transfer fucntion is:

$$\frac{U_{RC}(z)}{E(z)} = \frac{0.25z^{-701} + 0.5z^{-700`} + 0.25z^{-699}}{1 - 0.25z^{-701} + 0.5z^{-700`} + 0.25z^{-699}} \quad (11)$$

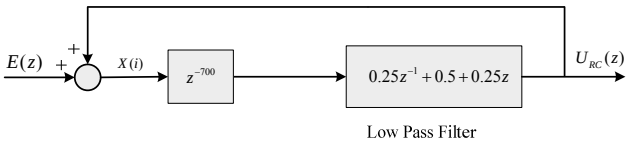

Fig. 9. Elements of the RC when $K_R = 1$ and $G_f(z) = 1$

The direct form I and direct form II are commonly used for implementation of the difference equation and filters [5]. First of all, a difference equation obtained from (11) is implmented using direct form I .The direct forrm I is a straightforward approach and the difference equation is directly evaluated. It is suitable for small filters/systems but it may not be sufficient and it may even be unrealistic for complex designs (such as in our case).The reason for non suitability is that it requires 2N delay elements for a system of order N. In other words it involves double memory. Fig. 10 shows the implementation of RC in direct form I. It can be observed that delay elements are used separately for both control signal and error coefficients.On the other hand, direct form II only needs half of memory in comparison to direct form I. The structure of direct form II is obtained by reversing the order of numenator and denominator as shown in Fig. 11.

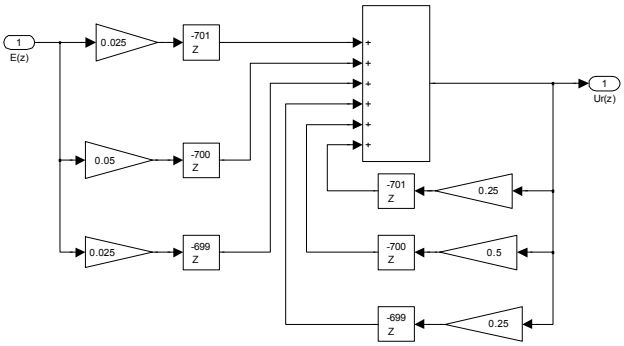

Fig. 10. Implementation of the RC in direct form I

The algorithm of RC can be developed by considering Fig. 9. Basically, an array of 700 elements needs to be assigned which represents the state variables. Instead of having separate arrays for the error and control signal, one array of state variable can be used for both error and control signal i.e. $X(i) = U_{RC}(z) + E(z)$. Following is the advantage of the direct form II scheme. The flow chart of algorithm for developing the RC is shown in Fig. 5.12.

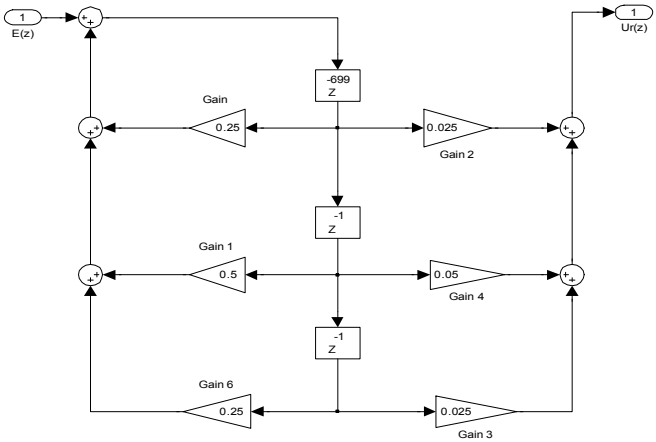

Fig. 11. Implementation of RC in direct form II

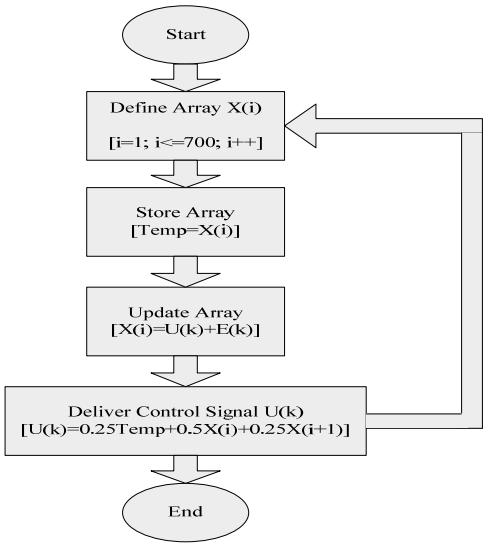

Fig. 12. Flowchart of the algorithm for implementation of the RC

Results and Conclusion

Comprehensive simulation is supported by MATLAB Simpower Systems Toolbox. The performance of the controller is tested against different grid THD levels. The measured values of the grid voltage have been used and modelled for simulation. The total grid voltage THD was 1.9%. The simulation results are shown by Fig. 13 and Fig. 14. The output current THD is 2.2% with RC and 22% without RC. Fig. 15 and Fig. 16 show the experimental results. The output current THD is 2.0% and 16% without RC. So it is clear that using RC, current THD is significantly improved. The current waveforms have been obtained using a high bandwidth Regowski coil and saved using digital oscilloscope.

We can conlude that Implementation of RC based control scheme for interleaved inverter has been evaluated using hardware. The experimental results reveal that the RC helps to lower the THD level considerably without steady state error in the output current even when the grid THD is high or under grid impedance variations. While implementing RC, two forms such as direct form I and direct form II have been considered. It is found that the direct form II involves less memory and provides faster response due to less computational burden. The detailed description of hardware set-up has been included to explain the whole process.

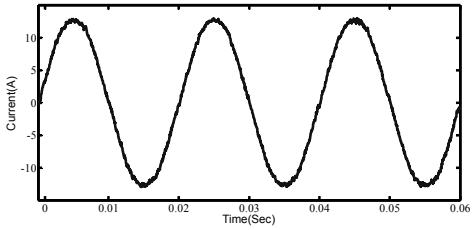

Fig. 13. Simulated output current with RC (THD=2.2%)

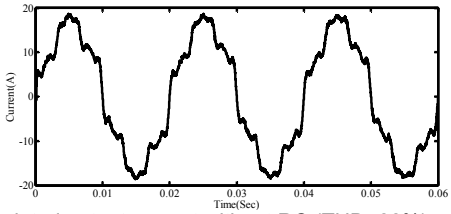

Fig. 14. Simulated output current without RC (THD=22%)

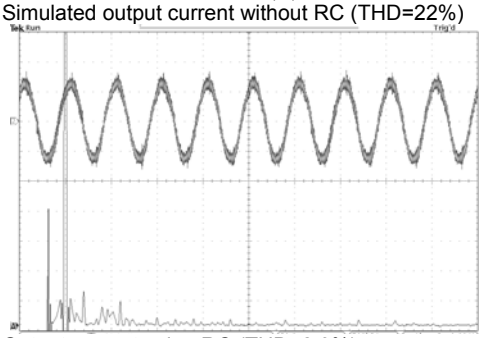

Fig. 15. Output current using RC (THD=2.0%)

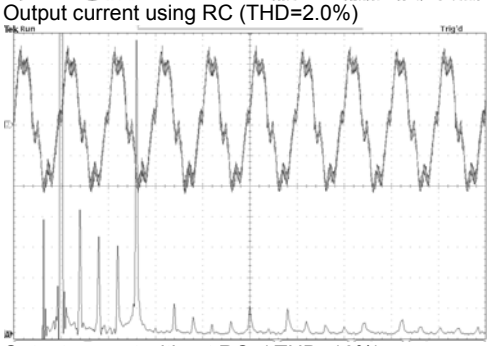

Fig. 16. Output current without RC (THD=16%)

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