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Classification and Comparison of BPFC Techniques: A Review

***Abstract**: Power factor correction (PFC) techniques play an important role in green power and energy-saving technology. Based on conventional boost PFC, many novel topologies and control strategies of bridgeless PFC(BPFC) have been proposed, and BPFC reduces the number of devices, the losses and improves the power density as well. In this paper, it discusses and investigates a variety of low conduction losses and high power factor performance of the BPFC topological structures and identifies their merits and limitations by comparing and analysing bridgeless boost PFC,bridgeless buck PFC ,bridgeless sepic PFC and Bridgeless cuk PFC. And the trends of bridgeless PFC techniques are analyzed in the meantime. For the selection, application, and the later structural optimization of Bridgeless PFC techniques which are used in the smart grid, distributed energy and green power and other equipments..*

***Streszczenie**. W artykule przedstawiono omówienie badań nad bezmostkowym korektorem współczynnika mocy, mających na celu porównanie strat przewodzenia i skuteczności działania, dla różnych topologii układu. W pracy określono zalety i ograniczenia poszczególnych architektur oraz ich ewolucję. Porównano ich zastosowanie do sieci inteligentnych, energetyki rozproszonej i odnawialnej. (**Przegląd i porównanie bezmostkowych korektorów współczynnika mocy**).*

Keywords: Bridgeless PFC; Boost; Buck; Sepic; C*uk* ;Power converter.
Słowa kluczowe: bezmostkowy PFC, podwyższający, obniżający, SEPIC, CUK, przekształtnik energoelektroniczny.

Introduction

In order to restrain harmonic pollution and improve power system quality, power factor correction device has been rapidly developed and used. Compared with passive PFC, active one can achieve a high PF and a small size [1], so PFC techniques which are mentioned at present are mostly refer to active PFC [2, 3].

Due to the existence of the input bridge in the conventional PFC, it limits to enhance the efficiency of the whole circuit [4]. In order to reduce the losses of the rectifier bridge, with continuous development of power electronics technology, based on conventional boost PFC, many novel topologies and control strategies of bridgeless PFC(BPFC) have been proposed, what make the bridgeless PFC techniques applying in all areas possible [5]. At the same time, bridgeless design ideas applied to other areas can also reduce the number of devices, the losses and it could improve the power density as well. Therefore, the studies of bridgeless become a hot spot in the research of scientific research personnel.

This paper provides a comprehensive overview of bridgeless PFC techniques. It is organized as follows. The bridgeless boost PFC techniques are reviewed in section 2. Section 3 discusses bridgeless buck PFC topologies. Section 4 shows bridgeless sepic PFC topologies, Bridgeless cuk PFC is in Section 5 and the last section looks forward to the development of the bridgeless PFC techniques.

Bridgeless boost PFC topologies

Basic bridgeless boost PFC topology

The basic topology of the bridgeless boost PFC shown in Fig.1 is proposed. It uses two controllable power switches to replace the two diodes of the lower bridge arm.

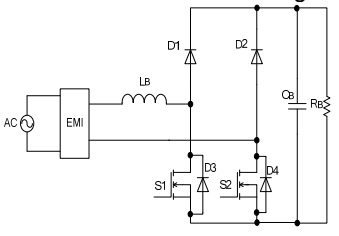


Fig.1. Basic bridgeless boost PFC topology

In the basic bridgeless boost PFC topology, switches S_1 and S_2 can be driven with the same PWM signal, which greatly simplified the control circuit. While this topology not only has the least semiconductor devices used in the whole circuit, but the line current simultaneously flows through only two semiconductors in the course of the work. So it has low loss and high efficiency. In addition, this topology solves the problem of heat management in the input rectifier diode bridge [6]. But the output ground has HF pulsating voltage source. It charges and discharges the equivalent parasitic capacitance between the output ground and the ac line ground, resulting in a significantly increased common-mode noise [7]. In the aspect of sampling the inductor current, the topology needs to build a complex detection circuit, at the same time, the body diodes of switches S_1 andS_2 are also in the HF switching state. So it should not be used in CCM [8].

Bridgeless interleaved boost (BLIL) PFC topology

The proposed novel BLIL PFC topology is shown in Fig.2. It retains the same semiconductor device count as the interleaved boost PFC topology.

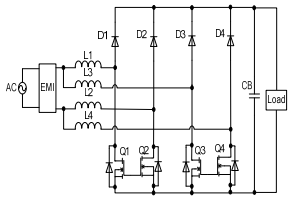
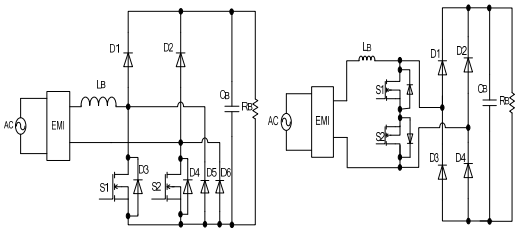


Fig.2. Proposed novel BLIL PFC topology

The topology has the advantage the interleaved boost PFC circuit, and can effectively solve the problem of heat management of the interleaved boost PFC circuit. In addition, the proposed topology achieves high efficiency at power levels above 3 kW due to the elimination of the boost diode rectifier bridge [6]. But it requires two additional MOSFETS and two fast diodes in place of four slow diodes used in the input bridge of the interleaved boost PFC. And only two inductors used in each half cycle as well. The inductor utilized rate is low, while the corresponding cost will increase.

Bridgeless PFC boost topology with bidirectional switch

The bridgeless PFC boost topology with bidirectional switch is shown in Fig.3. The modification of the basic bridgeless PFC boost rectifier is implemented by adding two diodes.



(a) Type 1 (b) Type 2

Fig.3. Bridgeless boost PFC topology with bidirectional switch

Type1 or type 2 is only two semiconductor devices on operating state, so the conduction losses are low. At the same time, diodes D_5 and D_6 or D_3 and D_4 connect the output to input voltage and the output is no longer in a floating state, what makes the common-mode interference smaller [8,9]. But its drawback is that gate voltage of the two switches is different, so it requires isolated gate-drive transformer, the design of drive circuit slightly seems complex. In the aspect of sampling the inductor current, complex detection circuit is required. Meanwhile, body diodes of the switches (S_1 and S_2) are also in HF switching state. So the topology should not be used in CCM [10].

Totem-Pole bridgeless boost PFC topology

The totem-pole bridgeless boost PFC topology shown in Fig.4 is proposed. It is the modification of the basic bridgeless boost PFC topology from Fig.1 which is obtained by exchanging the position of semiconductor device.

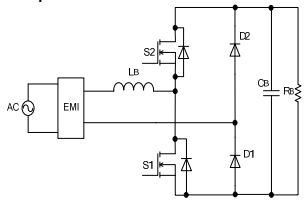


Fig.4. Totem-pole bridgeless boost PFC topology

Analyzing the circuit can be seen, in each half cycle of input voltage, there are only two semiconductor devices in working condition, so it has low conduction losses. During the working process, diodes D_1 and D_2 connect the output port to input voltage and the output is no longer in a floating state, what make the common-mode interference smaller. Meanwhile, this topology has the advantage of the simple main circuit structure and high device utilization. But body diodes of the two switches (S_1 and S_2) in the topology have the same function of the fast-recovery diodes in the conventional boost PFC. So this topology is usually used in DCM or CRM [8]. If it is working under CCM, due to the reverse recovery time of most power switches' body diode are much longer than that of fast-recovery diodes, hence the reverse recovery loss will be very serious and the efficiency is inevitably limited. In the aspect of sampling the inductor current, this topology requires a complex detection circuit. At the same time, two switches require isolated gate-drive transformer, so the design of drive circuit slightly seems complex. Although the topology has the drawback of complex drive and sampling circuit, but it had merit of low electromagnetic interference, simple main circuit structure, high device utilization and so on, so it has a good prospect in low power application [11,12].

Pseudo totem-pole bridgeless boost PFC topology

Fig.5 shows Pseudo totem-pole bridgeless boost PFC topology. It is a variation of totem-pole bridgeless boost PFC topology, which is obtained by adding two diodes.

During the working process of this topology, diodes D_3 and D_4 connect output to input voltage, which makes common-mode interference lower [7,8]. However, each inductor (L_1 and L_2) is only working at half power frequency cycle, so the inductor utilized rate is low [9]. Meanwhile, this topology would also require a complex sampling inductor current and control and drive circuit and, consequently, it is less attractive for practical implementation.

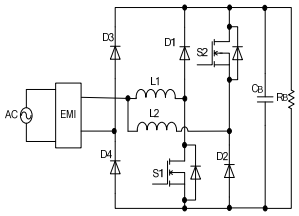


Fig.5. Pseudo totem-pole bridgeless boost PFC topology

Proposed totem-pole bridgeless boost PFC topology

The proposed totem-pole bridgeless boost PFC topology shown in Fig.6 is proposed. It employs coupled inductor to replace the separate inductors of totem-pole bridgeless boost PFC. Switches M_1 and M_2 or M_3 and M_4 operate in phase-shift mode with 180° .

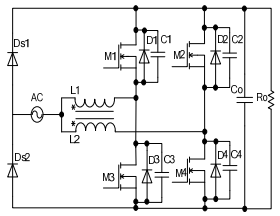


Fig.6. Proposed totem-pole bridgeless boost PFC topology

The topology inherited the advantage of totem-pole bridgeless boost PFC. It has simple circuit, low conduction losses and low CM noise interference. It can operate in any mode. The reverse recovery of the intrinsic diode is greatly reduced, and the efficiency improves greatly. At the same time, ZVS and ZCS are achieved in a considerable range. The application to bidirectional dc/dc converters and bidirectional ac/dc converters is retained [13]. But in the aspect of sampling the inductor current, proposed totem-pole topology [14,15] requires a complex detection circuit. In addition, the design and analysis of coupled inductor is complex [9]. Each switch requires an isolated gate drive. Therefore, it has a good prospect in low power application.

Bridgeless boost PFC topology with two dc/dc boost circuits

The bridgeless boost PFC topology with two dc/dc boost circuits (2nd DBPFC) is shown in Fig.7. In addition to diodes D_3 and D_4, which are slow-recovery diodes, inductors L_1 and L_2 form two dc/dc boost circuits. It is the most popular topology at present.

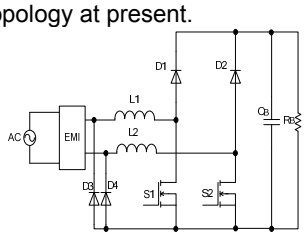


Fig.7. Bridgeless boost PFC topology with two dc/dc boost circuits

Switches S_1 and S_2 in Fig.7 can be driven with the same PWM signal, which significantly simplifies the implementation of control circuit. Meanwhile, complex sampling inductor current circuit is not required, and two inductors compared to a single inductor have better thermal performance [8-10]. However, each inductor only works at half power frequency cycle, so the inductor utilized rate is low, the cost will increase at the same time [9].

Dual coupled winding 2nd DBPFC topology

The dual coupled winding 2nd DBPFC topology shown in Fig.8 is proposed. Compared to bridgeless boost PFC topology with two dc/dc boost circuits, it employs coupled inductor to replace separate inductors and it form coupled branch by adding two diodes simultaneously.

This topology retains the merit of bridgeless boost PFC topology with two dc/dc boost circuits. By making use of the coupled inductor to transfer the current through boost diodes to the coupled branch, it achieves the natural turn-off of the boost diodes and zero-current turn-on of switches. Meanwhile, utilizing the leakage inductance of the coupled inductor reduces reverse recovery of coupled branch diodes, and therefore the switches reverse-recovery losses reduce. What can significantly improve the efficiency of the machine and solve the problem of common mode interference [16-18]. But the design and analysis of coupled inductor is complex, the cost will increase [9].

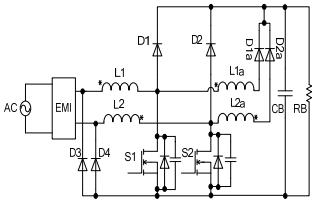


Fig.8. Dual coupled winding 2nd DBPFC topology

Bridgeless dual-boost PFC topology

Bridgeless dual-boost PFC topology is shown in Fig.9, which is the modification of the totem-pole bridgeless boost PFC topology.

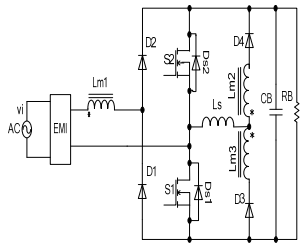


Fig.9. Proposed bridgeless dual-boost PFC topology

The topology retains the advantage of the totem-pole bridgeless boost PFC topology. A coupled inductor is utilized as a cost-effective method to reduce the diode reverse-recovery problems, and Zero-current switching (ZCS) is achieved when the body diodes are turned off. Meanwhile, the reverse-recovery currents of the auxiliary diodes are also alleviated by using a simple and efficient passive snubber circuit. In addition, to use this topology in a practical design, a control strategy by employing the linear peak current mode (LPCM) control is suggested [19]. A high power-factor can be obtained without sensing the AC input voltage. However, the design of this topology needs to consider in detail [20,21]. And the design and analysis of coupled inductor is complex, at the same time, the gate voltage of the two switches is different, so it requires isolated gate-drive transformer, the design of drive circuit slightly seems complex.

Proposed ZVS bridgeless boost PFC topology

Fig.10 shows the proposed ZVS bridgeless boost PFC topology. The circuit in the dotted box is the proposed auxiliary circuit which provides soft switching for the main switches.

This topology achieves zero voltage switching (ZVS). When the power switches are turned off, voltage across the power switch S_1 will increase slowly until all the energy stored in the capacitor C_1 transfer to load. So when the current through the power switch decays to zero, the voltage across it is much smaller V_o. That greatly reduces the loss when the switch is turned off. And using this topology, the power loss of turn-off the switches reaches near to 0, in addition, which significantly reduces the turn-off loss, thus greatly improves the efficiency [22-24]. But the drive signals of power switches require isolated drive. Meanwhile, the components of capacitances, inductors and diodes will increase, and the cost will increase.

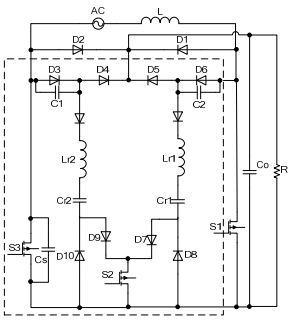


Fig.10. Proposed ZVS bridgeless boost PFC topology

Dual boost bridgeless PFC topology of capacitive coupling with CM and DM filter

The dual boost bridgeless PFC topology of capacitive coupling with CM and DM filter is shown in Fig.11. The inductors L_{cm} operates as CM filter inductor and L_{int} which integrates the CM and DM filters is used as the DM boost inductor. Capacitors C_{cm} and C_{dm} provide the loop for high-frequency interference signals.

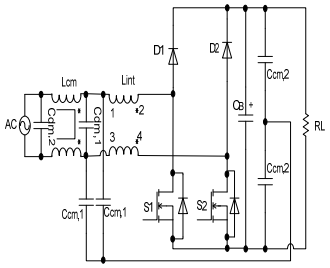


Fig.11. Dual boost bridgeless PFC topology of capacitive coupling with CM and DM filter

The topology can work in two modes CCM and DCM. Due to the large parasitic output capacitance of the parallel connected MOSFETS ZVS conditions are given during turn-off, so that the conduction losses are very small and the efficiency is improved. Meanwhile, the two input inductors can be operated as the common mode (CM) and differential mode (DM) filter, which not only reduces the volume, but achieve the purpose of reducing EMI [25]. However, the design and analysis of coupled inductor is complex [10], while the cost increases at the same time.

A single inductor three-level bridgeless boost PFC topology with nature voltage clamp

Fig.12 shows a single inductor three-level bridgeless boost PFC topology with nature voltage clamp. Only single inductor is required with nature voltage clamp in the figure. And the charging stage is presented in the low side while discharging stage in the high side, and vice verse.

Only one inductor is required in this topology, and nature voltage clamp is achieved and the voltage stresses of all semiconductor devices are reduced to half of the total output voltage. The MOSFETS and the slow diodes are both 'shared'. Extra rectifying diodes and voltage clamping diodes are not required. And low voltage stresses and low conduction losses are achieved with low common-mode

noise interference, thus effectively improve the efficiency [26]. But the complex circuit for sensing the inductor current is required. In addition, both switches require isolated gate drive, so the drive circuit is also complex.

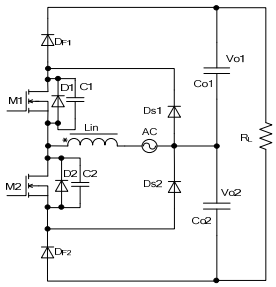


Fig.12. A single inductor three-level bridgeless boost PFC topology with nature voltage clamp

Single-Stage bridgeless three-level converter with current doubler rectifier

The single-stage bridgeless three-level converter with current doubler rectifier is shown in Fig.13. It integrates the operation of the bridgeless power factor correction (PFC) boost rectifier and the zero-voltage switching (ZVS) three-level dc-dc converter.

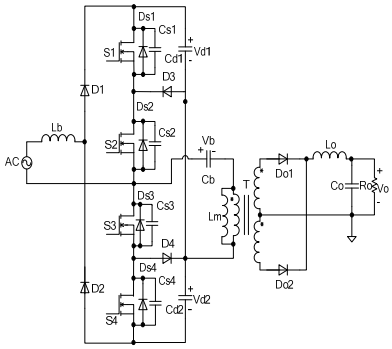


Fig.13. Single-stage bridgeless three-level converter with current doubler rectifier

The topology provides high power factor and direct power conversion from the line voltage to an isolated dc output voltage without using the full-bridge diode rectifier. By allowing the boost inductor to operate in DCM, PFC and fast output voltage regulation are performed simultaneously by the asymmetrical pulse-width modulation (APWM) control of power switches. Moreover, conduction losses are lowered by essentially eliminating the full-bridge diode rectifier, voltage stresses of the power switches are reduced by the use of three-level topology at the same time. Switching losses are also reduced by achieving zero-voltage switching (ZVS) of the power switches. The proposed topology not only reduces the number of circuit components, but also makes it possible to increase power efficiency [27].But the complex circuit for sensing the inductor current is required. In addition, both switches require isolated gate drive, so the drive circuit is also complex. Meanwhile, the design and analysis of inductors and transformer is complex. And the cost increases as well.

Bridgeless buck PFC topologies

Proposed isolated bridgeless buck PFC topology

Fig.14 shows the proposed isolated bridgeless buck PFC topology. It eliminates the bridge rectifier by employing two switches and two capacitances. And the reduction voltage is achieved by isolation transformer.

This topology can operate in DCM condition and it has the capability of high power factor correction. It is capable to perform the ac to dc conversion without the diode bridge rectifier. And this topology uses Flyback converter as it first stage dc-dc converter due to its capability to step-down the output voltage with larger ratio and capable to isolate the input and output part. And it is normally required by most application namely switch mode power supply (SMPS), LED driver and battery charger. However, the Flyback converter is not a good PFC circuit due to its input current waveform characteristics which always being turned ON and OFF simultaneously during each switching period [28]. And both switches require isolated gate drive, so the drive circuit is also complex. Meanwhile, the design and analysis of inductors and transformer is complex. And the cost increases as well.

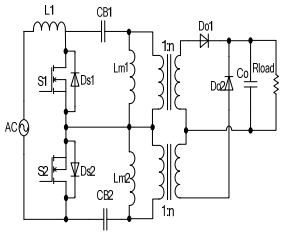


Fig.14. Proposed isolated bridgeless buck PFC topology

Bridgeless buck PFC topology with voltage doubler output

The proposed bridgeless buck PFC topology with voltage doubler output has five variable forms, as shown in Fig.15(a)~(e).

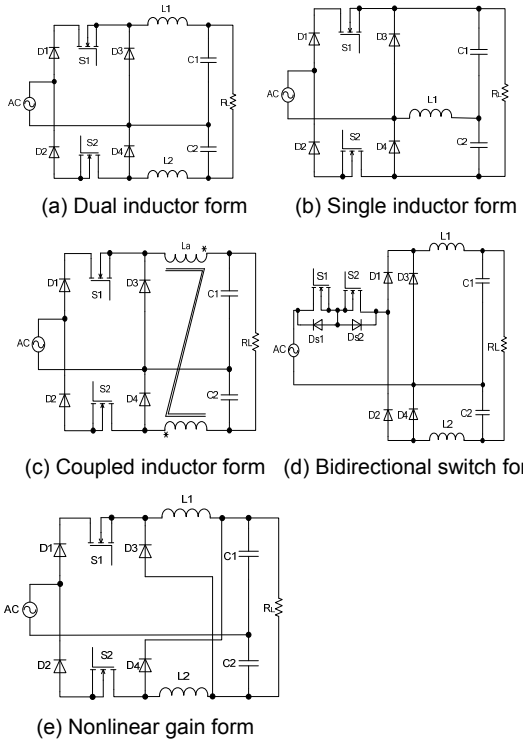


Fig.15. proposed bridgeless buck PFC topology with voltage doubler output

By eliminating input bridge diodes, this topology reduces the conduction loss through minimization of the number of simultaneously conducting semiconductor components, thus further improves the efficiency. Meanwhile, the topology doubles the output voltage, which extends useable energy after a dropout of the line voltage. And it also shows better hold-up time performance. Since the switches are located between the input and the output capacitors, switches S_1 and S_2 can actively control the input inrush current during start-up. So the proposed topology has a

good inrush current control capability. But due to the topology does not shape the line current during the time intervals when the line voltage is lower than the output voltage, so there is a strong trade-off between the THD and PF performance and output voltage selection. However, increasing the output voltage increases the THD and lowers the PF due to the increased dead angle. Switches S_1 and S_2 were operated simultaneously by the same gate signal from the PWM controller. And the gate voltage of each switch is different, so both switches require isolated gate drive, so the drive circuit is also complex [29,30].

Bridgeless sepic PFC topologies

A novel bridgeless sepic PFC topology

Fig.16 shows a novel bridgeless sepic PFC topology. It eliminates the bridge rectifier by utilizing two switches.

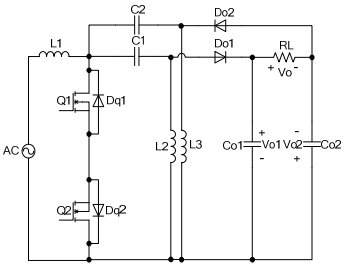


Fig.16. A novel bridgeless sepic PFC topology

In the topology, the two power switches, namely, Q_1 and Q_2, can be driven with the same PWM signal, which significantly simplifies the implementation of the control circuit. And during each switching cycle, there is either one or two semiconductors in the flowing current path. Hence, the conduction losses as well as the thermal stresses on the semiconductor devices are further reduced, and the circuit efficiency is improved compared with that of the bridgeless boost topology. Another advantage of the proposed topology is a reduction in the semiconductor voltage stress as compared with that of the conventional sepic PFC topology [31]. But it requires an additional gate drive transformer. And the number of the capacitance and inductor increase, the structure is more complex. Meanwhile, the output voltage is limited, which must be twice as large as input voltage, which destroy the advantage of the output voltage can be lower than the input voltage in the sepic PFC circuit. At the same time, the positive and negative direction of the capacitor is varied by the direction of the input voltage. So the circuit cannot use the traditional electrolytic capacitor. It increases the difficulty of capacitor selection and the cost of circuit [32].

Bridgeless sepic PFC topology with coupled inductors

The bridgeless sepic PFC topology with coupled inductors is shown in Fig.17.

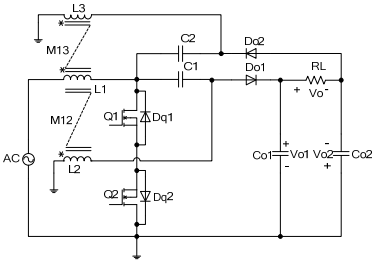


Fig.17. Bridgeless sepic PFC topology with coupled inductors

Three inductors in the figure can be magnetically coupled into a single magnetic core. In this case, a standard EI magnetic core can be used for practical implementation of the magnetic circuit. In addition, by proper coupling between the three windings, it is possible to obtain an input current having very low high-frequency content (near-zero current ripples). And the EMI noise is lowest. The topological stage for the coupled inductor circuit is similar to the topological stage for the uncoupled case and the conventional sepic PFC topology [31,32]. But the design and analysis of coupled inductor is complex.

Bridgeless sepic PFC topology

Fig.18 shows the proposed bridgeless sepic PFC topology. Two diodes of input rectifier are substituted with switches.

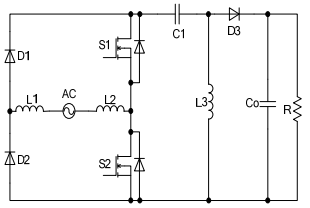


Fig.18. Bridgeless sepic PFC topology

Compared with the conventional sepic topology, one switch is added in this topology. And two switches replace the two diodes of bridge rectifier, which reduce the number of semiconductor and make ac input add to input directly without passing through the bridge rectifier. The absence of an input diode bridge and the presence of only one diode in the flowing current path during each switching cycle result in less conduction loss and improved the transmission efficiency. At the same time, two switches are driven with the same PWM signal, which significantly simplifies the implementation of the control circuit. The main switch turn on is under zero current switching condition and D_3 turn off is under zero current switching condition [33,34]. And it eliminates the current loop, while the output voltage generated by the converter can be low than the input voltage, the advantage is obvious. But it requires an additional gate drive transformer and inductor [31].

Bridgeless PFC topology based on sepic dc-dc converter

A new bridgeless PFC topology based on sepic dc-dc converter is proposed in Fig.19.

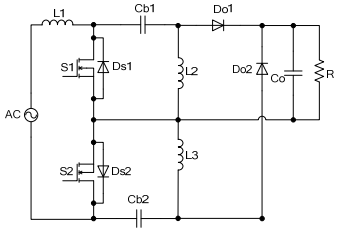


Fig.19. Bridgeless PFC topology based on sepic dc-dc converter

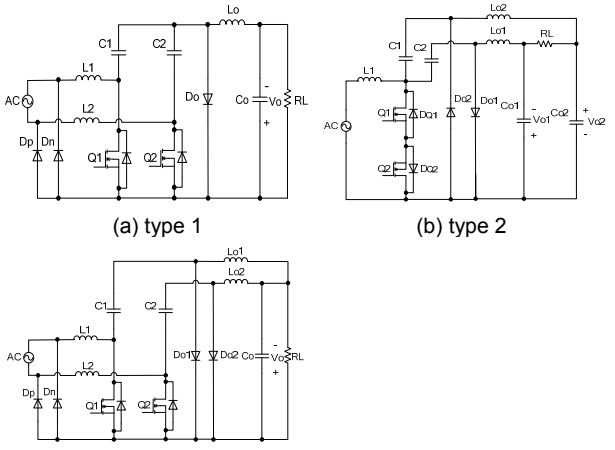
The topology has less number of components operated at each input-voltage cycle. It is capable to achieve high power factor under universal input voltage condition. And the capability to reshape the input current is inherent when the circuit is operated in DCM. Driving the MOSFETS gate terminal is simpler due to both 'source' terminals of the MOSFETS are connected to a common node and last but not least and no gate-driver circuit with isolation is required. But this topology would be only suitable to be used as a switch mode power supply application for low power equipments especially those requiring high quality input power [35].

Bridgeless cuk PFC topologies

Bridgeless cuk PFC topology

Bridgeless cuk PFC Topology has three types, as shown in Fig.20(a),(b),(c) respectively. They are formed by connecting two dc-dc cuk converters.

The absence of an input diode bridge and the presence of only two semiconductor switches in the current flowing path during each switching cycle result in reducing the switching device current stress, less conduction losses and switch losses and an improved thermal management compared to the conventional cuk PFC converter. And the proposed topologies are designed to work in discontinuous conduction mode (DCM) to achieve almost unity power factor in a simple and effective manner. DCM operation gives additional advantages of zero-current turn-on in the power switches, zero-current turn-off in the output diode, and reduces the complexity of the control circuitry. Although type 2 has a minimum number of semiconductors in the current conduction path. However, it has disadvantages of floating switch and a step-up voltage gain greater than 2. The floating switch requires a more complex driver circuitry and typically causes higher electromagnetic emissions. The gain range is limited by the blocking voltage of D_{s2}. This disadvantage can be minimized by implementing input/output galvanic isolation. However, components with higher blocking voltage capability are needed. Type 1 also has the advantage of a lower component count, but a higher current peak. Whereas, type 3 has higher component count, but lower stresses. However, the proposed topologies do not suffer from the high common-mode EMI noise emission problem and has common-mode EMI performance similar to conventional topologies. Consequently, the proposed topologies appear to be promising candidates for commercial PFC products [36-38].



(a) type 1 (b) type 2

(c) type 3

Fig.20. Proposed bridgeless cuk PFC topology

A novel bridgeless cuk PFC topology

A novel bridgeless cuk PFC topology is shown in Fig.21. It is formed by two cuk converters.

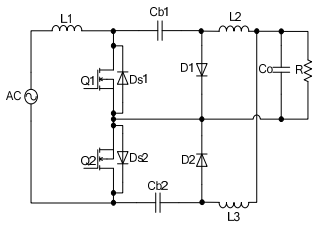


Fig.21. A novel bridgeless cuk PFC topology

The topology is formed by two cuk converters, one of the advantages inherent in each cuk converter is its high quality input and output current. And the topology is designed to work in discontinuous conduction mode (DCM). The number of components conducted, i.e. input diode, during each half-line period is less compared to the conventional cuk PFC converter and even less than the normal bridgeless cuk PFC. The fully-bridgeless cuk converter only has one input diode conducted all the time which is either D_{s1} or D_{s2}. Thus, the conduct losses reduce greatly, and the efficiency and power factor increase effectively. However, the drawback is the overall number of components used to develop this converter is more compared to the other two cuk PFC topologies mentioned earlier. It is due to two set of cuk converters exist during each half-line period [39].

The prospects of Bridgeless PFC techniques

With the emergence of new demand, the unceasing development of semiconductor technologies appearance of new topologies and control techniques, PFC techniques have broader prospects and further research focus mainly on the following aspects.

New devices

Currently, the analog integrated control chips are mainly employed in bridgeless PFC control. It progresses from the average current control in the early to new one-cycle control. In recent year, the researches of integrated control chips are focus on one-cycle and average current control, and other control algorithm is still nothingness. Meanwhile, the integrated modules of bridgeless PFC topology are nothingness at present. Consequently, more new devices about PFC are looked forward to appear.

Topological structures

In addition to the basic bridgeless PFC, some other bridgeless PFC topologies have been proposed, which are aimed at reducing EMI noise or simplifying the circuit structure. The new proposed topologies add a new member to bridgeless PFC family, and provide more structural options for engineers. At the same time, the hybrid topologies based on the existing or neoteric principles has been a hot research area, and more new topological solutions are expected to appear.

Soft-Switching topology

As a PFC structure with low conduction losses, the bridgeless PFC has less contribution to reduce the switching losses. There are two manners to reduce the switching losses by using soft-switching technology. One is active mode, the other is passive mode, no matter which way is to be chose, simple structure, low cost and high efficiency is the goal of the research. So deeply analyzing the losses sources of bridgeless PFC and using more techniques about soft-switching to suppress the harmonic is another research keystone of bridgeless PFC.

Electromagnetic interference (EMI) analysis and suppression

As the domestic and international electromagnetic compatibility standards for electric equipment are launched, reducing the EMI noise in power and various types of electronic equipment and increasing the capacity of resisting disturbance are an important part of products' research and design. As the EMI noise source and propagation path is influenced by the circuit structure, the circuit layout, switching frequency, electronic components and other element, in addition, they are bound up with the invisible magnetic, so EMI is important problem which puzzle many engineering and technical personnel. While as a circuit structure, bridgeless PFC must be passed through all kinds of tests of EMC standard to achieve market-

oriented and user-oriented. Therefore, analyzing and studying the problems of bridgeless PFC EMI are a very difficult and arduous task which is placed in the majority of the researchers.

Control strategies

In accordance with whether the input inductor current is continuous, the PFC control strategies can be divided into discontinuous current mode (DCM) and continuous current mode (CCM), and in between the critical DCM (DCM). While according to whether is directly selected the transient inductor current as the feedback value, the CCM can be divided into direct current control and indirect current control. Indirect current control technique indirectly control input inductor current by controlling the input voltage amplitude and phase of topology, which make the inductor current and voltage in phase. Control circuit is simple, but it is employed relatively less due to the sensitivity of the parameters. Direct current control sense the input current of topology as the feedback and controlled value, which have the advantages of good dynamic and steady state performance and ability to limit the input current. Currently, for direct current control, there are peak current control, hysteresis current control, average current control, predictive current control, deadbeat control, one-cycle control, state feedback control, sliding mode control, fuzzy control and so on. With the improvement of market demand, many high-speed chips with control algorithms have appeared, such as the IR1150, etc. On this basis, intelligent digital control algorithm has the advantages of simple circuit, insensitive to external interference, easy to upgrade system, strong adaptability, convenient function expansion and it can achieve more complex control algorithm, etc. So it is an important research area in bridgeless PFC. Therefore, new intelligent control methods (the new control methods based on existing control structures) and new topologies based on the special control are looked forward to appear.

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REFERENCES

[1] H.Wang, X.J. Yang,et al., "Thoretic Analysis and Experimental Study of Partial PFC Technology," The World of Inverters. Shanghai, pp.45-50, 2008.

[2] M. M. Jovanovic and Y. Jang, "State-of-the-Art, Single-Phase, Active Power-Factor-Correction Techniques for High-Power Applications-An Overview," IEEE Trans. on Ind. Electron., Vol. 52, No. 3, pp. 701-708, 2005.

[3] Y. C. Hsieh, T. C. Hsueh ,et al., "An Interleaved Boost Converter with Zero Voltage Transition," IEEE Trans. on Power Electron., Vol. 24, No. 3, pp. .973-978, 2009.

[4] Dehong Xu, Jindong Zhang, ,et al., "Evaluation of output filter capacitor current ripples in single phase PFC converters," IEEE Power Conversion Conf., PCC., Vol. 3, Osaka, Japan, pp. 1226 – 1231, 2002.

[5] Yang Xi-jun, Wang Han,et al., "Theoretic Analysis and Experimental Study of a Novel Bridgeless Partial Active PFC," IEEE Electrical Machines and Systems Conf., pp. 1179-1184, Oct. 2008.

[6] F. Musavi, W. Eberle ,et al., "A High-Performance Single-Phase Bridgeless Interleaved PFC Converter for Plug-in Hybrid Electric Vehicle Battery Chargers," IEEE Trans. on Ind. Appl., Vol. 47, No. 4, pp. 1183-1143, 2011.

[7] F. Musavi, W. Eberle ,et al., "A Phase Shifted Semi-Bridgeless Boost Power Factor Corrected Converter for Plug in Hybrid Electric Vehicle Battery Chargers," IEEE Applied Power Electron. Conf. and Exposition, APEC, pp. 821-828, 2011.

[8] L. Huber, Yungtaek Jang ,et al., "Performance Evaluation of Bridgeless PFC Boost Rectifiers," IEEE Trans. on Power Electron., Vol. 23, No. 3, pp. 1381-1390, May. 2008.

[9] Yungtaek Jang and M. M. Jovanovic, "A Bridgeless PFC Boost Rectifier With Optimized Magnetic Utilization," IEEE Trans. on Power Electron., Vol. 24, No. 1, pp. 85-93 Jan. 2009.

[10] Liu Gui-hua, Wang Wei and Xu Dian-guo, "Research On conventional PFC and bridgeless PFC in air conditioner," IEEE Power Electron. and Motion Control Conf., IPEMC , pp. 666-669, July 2009.

[11] S. S. Darly, P. V. Ranjan, ,et al., "A Novel Dual Boost Rectifier for Power Factor Improvement," International Conference on Electrical Energy Systems, pp. 121-127, 2011.

[12] B. Su, J. M. Zhang and Z.Y. Lu, "Totem-Pole Boost Bridgeless PFC Rectifier With Simple Zero-Current Detection and Full-Range ZVS Operating at the Boundary of DCM/CCM," IEEE Trans. on Power Electron., Vol. 26, No. 2, pp. 427-435, Feb. 2011.

[13] B. Su and Z. Y. Lu, "An Interleaved Totem-Pole Boost Bridgeless Rectifier With Reduced Reverse-Recovery Problems For Power Factor Correction," IEEE Trans. on Power Electron., Vol. 25, No. 6, pp. 1406-1415, Jun. 2010.

[14] H. Yao-Ching, H. Te-Chin and Y. Hau-Chen, "An interleaved boost converter with zero-voltage transition," IEEE Trans. on Power Electron., Vol. 24, No. 4, pp. 973-978, Apr. 2009.

[15] W. Wei, L. Yim-Shu, ,et al., "Interleaved boost converter with zero diode reverse-recovery loss," IEEE Trans. on Aerosp. Electron. Syst., Vol. 40, No. 4, pp. 1271-1285, Oct. 2004.

[16] Yang Fei, Ruan Xin-bo,et al.,"Design issues of interleaved critical conduction mode boost PFC converter with coupled inductor," IEEE Energy conversion Congress and Exposition, ECCE, pp. 2245-2252, Nov. 2010.

[17] W. Y. Choi, J.M. Kwon,et al. "Bridgeless Boost Rectifier With Low Conduction Losses and Reduced Diode Reverse-Recovery Problems," IEEE Trans. on Ind. Electron., Vol. 54, No. 2, pp. 769-780, Apr. 2007.

[18] Mohammad Mahdavi and Hosein Farzanehfard, "A New Zero Voltage Transition Bridgeless PFC with Reduced Conduction Losses," Journal of Power Electronics, Vol. 9, No. 5, pp.708-717, Sept. 2009.

[19] J. P. GEGNER and C. Q. LEE, "Linear peak current mode control: a simple active power factor correction control technique for continuous conduction mode," Proc. IEEE Power Electron. Spec. Conf. (PESC), pp. 196-202, 1996.

[20] W. Y. Choi, J. M. Kwon ,et al., "Bridgeless dual-boost rectifier with reduced diode reverse-recovery problems for power-factor correction," IET Power Electron., Vol. 1, No. 2, pp. 194-202, 2008.

[21] W. Y. Choi, J. M. Kwon ,et al.,"An Improved Bridgeless PFC Boost-Doubler Rectifier With High-Efficiency," IEEE Power Electron. Spec. Conf. (PESC), pp. 1309-1313, 2008.

[22] R. Haghi, M. R. Zolghadri, et al.,"Design of a Bridgeless PFC with Line-Modulated Fixed Off-Time Current Control and Zero-Voltage Switching," IEEE International conference on Power Energy, pp. 129-134, 2010.

[23] Masoud Jabbari and Hosein Farzanehfard, "A New Soft Switching Step-Down/Up Converter with Inherent PFC Performance," Journal of Power Electronics, Vol. 9, No. 6, pp. 835-844, Nov. 2009.

[24] R. Haghi, M. R. Zolghadri and R. Beiranvand, "A Novel Zero-Voltage-Transition Bridgeless PFC With Reduced Conduction Losses," IEEE Power Electron. Drive Systems and Technologies Conf., pp. 587-592, 2011.

[25] J. Biela, J. W. Kolar and G. Deboy, "Optimal Design of a Compact 99.3% Efficient Single-Phase PFC Rectifier," IEEE Applied Power Electron. Conf. and Exposition, APEC, pp. 1397-1404, 2010.

[26] B. Su, J. M. Zhang and Z. Y. Lu, "Single Inductor Three-Level Boost Bridgeless PFC Rectifier with Nature Voltage Clamp," IEEE Power Electron. Conf., pp. 2092-2097, 2010.

[27] W. Y. Choi, J. Y. Choi and J. S. Yoo, "Single-Stage Bridgeless Three-Level AC/DC Converter with Current Doubler Rectifier," IEEE International Conference on Power Electronics, ECCE Asia the Shilla Jeju, Korea, pp. 2704-2708, 2011.

[28] M. R. Sahid and A. H. M. Yatim, "An isolated bridgeless AC-DC converter with high power factor," IEEE International Conference on Power and Energy, Kuala Lumpur, Malaysia, pp. 791-796, Nov. 2010.

[29] Yungtaek Jang and Milan M. Jovanovic, “Bridgeless Buck PFC Rectifier,” Appl. Power Electron. Conf. and Exposition(APEC), pp. 23-29, 2010.
[30] Yungtaek Jang and Milan M. Jovanovic, “Bridgeless High-Power-Factor Buck Converter,” IEEE Trans. on Power Electron., Vol. 26, No. 2, pp. 602-611, Feb. 2011.
[31] R. Antonio, D. Abud,et al., “Evaluation of boost, sepic and cuk topologies as power factor correction stage in electronic ballast applications,” International Power Electron. Congress, Technical Proceeding, CIEP, pp. 51-55, Aug. 2002.
[32] Esam H. Ismail, “Bridgeless SEPIC Rectifier With Unity Power Factor and Reduced Conduction Losses,” IEEE Trans. on Ind. Electron., Vol. 56, No. 4, pp. 1147-1157, Apr. 2009.
[33] M. Mahdavi and H. Farzanehfard, “New Bridgeless PFC Converter with Reduced Components,” IEEE International Conference on Electronic Devices, Systems and Applications (ICEDSA), pp. 125-130, 2011.
[34] M. Mahdavi and H. Farzanehfard, “Bridgeless SEPIC PFC Rectifier With Reduced Components and Conduction Losses,” IEEE Trans. on Ind. Electron., Vol. 58, No. 9, pp. 4153-4160, Sep. 2011.
[35] M. R. Sahid, A. H. M. Yatim and Taufik Taufik, “A New AC-DC Converter Using Bridgeless SEPIC,” IEEE Conference on Industrial Electronics(IECON), pp. 286-290, 2010.
[36] A. A. Fardoun, E. H. Ismail, A. J. Sabzali and M. A. Al-Saffar, “A Comparison between Three Proposed Bridgeless Cuk Rectifiers and Conventional Topology for Power Factor Correction,” IEEE ICSET Kandy, Sri Lanka, , pp. 1-6, Dec. 2010.
[37] A. A. Fardoun, A. J. Sabzali, E. H. Ismail and M. A. Al-Saffar, “A New Bridgeless PFC Sepic and Cuk Rectifiers with Low Conduction and Switching Losses,” IEEE International Conference on Power Electronics and Drive Systerm, PEDS, pp. 550-556, 2009.
[38] A. J. Sabzali, E. H. Ismail,et al., “New Bridgeless DCM Sepic and Cuk PFC Rectifiers With Low Conduction and Switching Losses”, IEEE Trans. on Ind., Vol. 47, No. 2, pp. 873-881, Mar. 2011.
[39] M. R. Sahid, A. H. M. Yatim ,et al.,“A bridgeless Cuk PFC converter,” IEEE Applied Power Electronics Colloquium (IAPEC), pp. 81-85, 2011.

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