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Reconfigurable three-phase SPWM implementation on DE2 FPGA

Abstract. *The purpose of this paper is to design and implement a modified strategy in traditional three phase SPWM technique based on Cyclone II ALTERA FPGA to be used for variable voltage and frequency AC supplies with high resolution to cover a required range of v and f, with customizable SPWM characteristics such as modulation index, carrier frequency, modulating signal frequency and delay time (dead-time). The design entry is achieved using Quartus II software through schematic and VHDL description language tools. By using the Altera DE2 development and education board the proposed architecture has been implemented and tested. Behavioural simulation and experiment results are successfully achieved showing that the proposed SPWM signal generation strategy works properly and can reduce the usage of logic elements (LE).*

Streszczenie. *W artykule opisano implementację zmodyfikowanej techniki modulacji sinusoidalnej PWM dla trójfazowych zasilaczy AC o regulowanym napięciu i częstotliwości. W badaniach wykorzystano platformę DE2 z układem FPGA Cyclone II firmy Altera. Wyniki symulacyjne i eksperymentalne potwierdzają skuteczność działania i redukcję wykorzystania zasobów układu. (**Implementacja rekonfigurowalnej, trójfazowej techniki SPWM na platformie DE2 z FPGA**).*

Keywords: FPGA, SPWM, VHDL, logic elements (LEs).
Słowa kluczowe: FPGA, SPWM, VHDL, elementy logiczne (LEs).

Introduction

Field programmable Gate Array (FPGA) devices are aimed in the implementation of high performance, large size circuits, thanks to the speed advantage of direct hardware execution on the FPGA, low volume applications, particularly for applications that can exploit customized bit widths and massive instruction-level parallelism. An even more, another important issue in using FPGAs is their re-configurability and reusable hardware architectures for rapid prototyping of the digital system [1].

The Cyclone FPGA's logic array consists of LABs, with 10 Logic Elements (LEs) in each LAB. An LE is a small unit of logic providing efficient implementation of user logic functions. LABs are grouped into rows and columns across the device. Cyclone devices range from 2,910 to 20,060 LEs [2].

In many applications we need to control both the magnitude and frequency output voltage or current, for example an AC frequency converter is designed to control both the voltage and frequency fed to the motor to adjust speed of the machine, the voltage sourced inverter is another example where the input DC voltage is essentially constant in magnitude and the AC output voltage has controlled in magnitude and frequency.

The pulse width modulation strategy is proven to be the most adapted technique for the controlled inverter while it has large range of the output voltage and frequency, and low total harmonic distortion (THD)[3,4].

The PWM technique implementation has been the subject of intensive research using different digital techniques based on microprocessors, micro-controllers and Digital signal processors (DSPs). Recently some researches were conducted in generating SPWM with FPGA. As among primary physical characteristics of a digital design is the area covered by the system , subsequently, we have to design full adjustable SPWM IC by entering the reference inputs related to required modulating and carrier frequency with high resolution, further with less number of logic elements(LEs) utilization. We will concentrate in this paper on area reduction based on choosing the correct topology. Topology refers to the higher-level organization of the design and is not device specific. Circuit-level reduction as performed by the synthesis and layout tools refers to the minimization of the number of gates in a subset of the design and may be device specific [5].

The SPWM technique that was introduced in [6], use 841 of logic elements, fixed carrier frequency and 1 Hz step to adjust the modulating frequency, in the references [1, 4, 7, 8] the modulating frequency of SPWM is fixed at 50Hz and the design is limited to two levels of modulation index which are set at 0.5 and 0.75. in [8] however in our design all the characteristics of SPWM can be adjusted and reconfigures, by 0.5 Hz step for modulating signal frequency and by exactly 0,78% step for amplitude level thanks to the used 8 bit data signed format. In addition to that, both carrier frequency and dead time can be chosen from the user corresponding to power switches characteristics used in the application.

Principle of Sine SPWM

Consider the single-phase half-bridge [9] (fig.1.a) comprising two complementary switches K_1 and K'_1 supplying a voltage (Va -Vo) equals to +U/2 or –U/ 2. In PWM [9], the points of turning K_1 and K'_1 are determined by the intersections of:

- Reference wave $(Va - Vo)_w$ representing the wanted signal with a frequency f_r .
- Modulation or carrier wave M, with a frequency f_c with a triangular shape and of amplitude U/ 2 (fig.1.b)

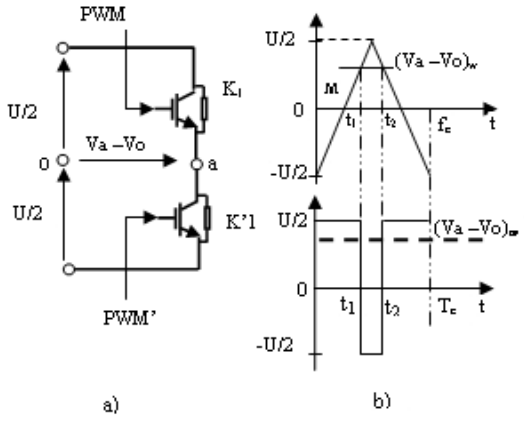

Fig.1. a) Single-phase half-bridge; (b) PWM generation

The equation of rising M Part:

$$M = -\frac{U}{2} + 2U\frac{t}{T_c} \tag{1}$$

The intersections of $(Va - Vo)_w$ with rising M at t_1, such as

$$t_1 = \left(\left(V_a - V_0\right)_w + \frac{U}{2} \right) \frac{T_c}{2U} \tag{2}$$

Determine the points at which K'$_1$ is turned on and hence the start of the periods where (Va –Vo) equals –U/2.

$$M = \frac{3U}{2} - 2U\frac{t}{T_c} \tag{3}$$

The intersections of (Va-Vo)w with falling M at t2, such a

$$t_2 = \left(\frac{3U}{2} - \left(V_a - V_0\right)_w \right) \frac{T_c}{2U} \tag{4}$$

Determine the points at which K1 is turned on and hence the start of the periods where Va –Vo equal +U/2. If f_c is much greater than f_r , voltage Va –Vo remains almost constant during a cycle T_c of carrier wave, the examination of fig. 1.b easily shows that the average value of Va –Vo, in this cycle is

$$(\mathrm{V_a} - V_0)_{av} = \frac{1}{T_c}\frac{U}{2}\left(T_c - \left(t_2 - t_1\right)\right) \tag{5}$$

Replacing t1 and t1 by their values, we get

$$(\mathrm{V_a} - V_0)_{av} = (\mathrm{V_a} - V_0)_w \tag{6}$$

So if the reference varies sinusoidally, the average value of (Va -Vo) varies in the same way. The aim is to approximate sinusoidal output voltages by sinusoidally varying their average values. The basic idea to produce SPWM switching signals consists to compare between the sine reference signal Vr and the triangular carrier signal Vc, which is clearly illustrated in Fig.2. If the reference is sinusoidal, two parameters characterize the modulation [9]:

- The modulation index or regulation factor ma; this is the ratio of the amplitude of the reference to the peak value of the carrier wave :

$$\mathrm{m_a} = \frac{V_r}{V_c} \tag{7}$$

- The frequency modulation index $\mathrm{m_f}$; this is the ratio between the carrier and reference frequencies:

$$\mathrm{m_f} = \frac{f_c}{f_r} \tag{8}$$

Since the turn-off time of power devices is usually longer

than its turn-on time, and therefore, an appropriate delay time named (dead-time) must be inserted between these two gating signals of the two complementary switches to avoid the short circuit. The length of this delay time is usually about 1.5 to 2 times the maximum turn-off time [10].

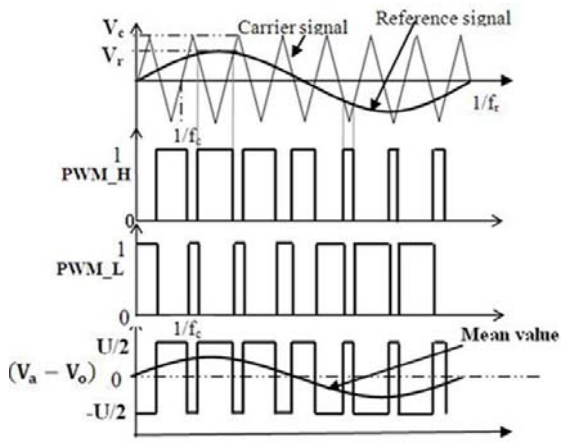

Fig.2 SPWM technique; PWM high pulse and low pulse; output voltage

Specifications

The three phase SPWM unit is designed to generate six output pulses (two signals per phase) adjusted in both index modulation, carrier modulating sine frequency with 0:5Hz step (highest possible resolution), but with a phase angle 120^o_ between pairs, and an appropriate delay time must be inserted between each two complementary pulses(PWM_H and PWM_L) to prevent short circuit problem and power converter breakdown.

The proposed SPWM architecture

The block diagram of the proposed architecture is shown in Fig. 3. The data inputs are three 8-bit data word, the first (frequency_ref) refer to the modulating wave frequency the second (Amplitude_ref) refer to the modulation index m_a, and the last corresponding to the frequency carrier, so it can be easily interfaced to a FPGA development DE2 board (IO port pins). The top module shown in fig. 3 is divided into sub-modules:

Three identical modules to generate three sine waves shifted between them with 120^0, which are used as modulating signals, each signal is generated by using an 8 bit free running counter point to the memory that contains a 256 samples of a the sine wave, that represented as 8 bit signed fractional format (-1 to + 1 of amplitude).

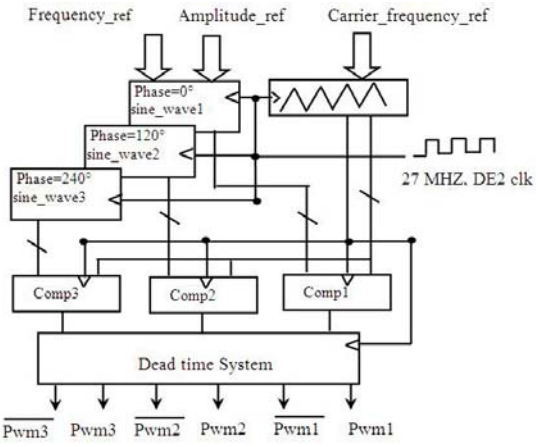

Fig.3 Block diagram of SPWM Strategy

The frequency of the generated waveform can be controlled by the clock of the pointer counter. Hence a configurable sub-module is designed to generate adequate clock frequency, in this research this sub module is configured to generate rang frequency sine wave (0.5 to 60 Hz) related to the entered Frequency_ref, since almost all the industrial motors work at 50/60 Hz as shown in figure 4.

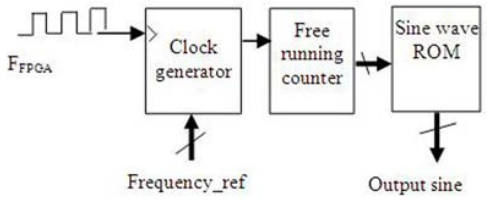

Fig.4 Generation the sine wave adjusted in frequency

The value of frequency_ref is determined by the following formula:

$$\text{Frequency}_{ref} = \frac{F_{FPGA}}{2^N.F_w} - 2 \quad (9)$$

where: Fw is desired sine wave frequency, F_{FPGA} is the FPGA board clock frequency (27 MHz in this work), N is the data width of counter (8 in our case).

Using the previous formula to calculate and store all Frequency_ref values in memory in order to generate the (1 to 60Hz) frequency rang. Another specification should be achieved is scaling the generated sine wave amplitude related to amplitude_ref (0 to 1 by requested step). To perform this operation, two fixed point arithmetic operation are used; the multiplication and the division which is carried easily by shift operation.

In this approach, each 8 bit data sine wave sample is read from the memory then it is multiplied by the entered amplitude_ref, the result is a 16 bit data signed which again shifted 7 times (division by 127), finally the result is converted into 8 bit signed data format. This approach allows us to scale the sine wave between 0 and 0:992 by 0.0078 step which represents 0.78%.

The carrier waveform is a triangle wave that was implemented in FPGA like an up-down counter, with same way described in previous paragraph we can generate the carrier waveform with desired frequency related to the carrier_ frequency_ref input.

The deadbeat time insertion was embedded after the outputs of the comparators. Every comparator output and its complement are subject to an adjustable delay when they switch from logic ’0’ to logic ’1’. The deadbeat time can be adjusted by controlling the clock which is used to trigger the dead time system. With these approaches any desired specification can be easily achieved.

Functional simulations Results

The designed SPWM top module has been developed and implemented by using the Altera DE2 development and education board, which include Cyclone II 2C35 family EP2C35F672C6 FPGA devise in a 672-pin package, and EPCS16 serial configuration device using Quartus II software provided by Altera. The figure 5 shows the top level entity of SPWM which is developed by using schematic and vhdl description language.

The entered design is synthesized into a circuit that consists of the logic elements (LEs) provided in the FPGA chip. The Fig. 6 displays the compiler flow summary section, which indicates that only 2% (607) logic element, 4% of memory bits, 13% of pins, 0% of PLLs unit are needed to implement this circuit on the selected FPGA device.

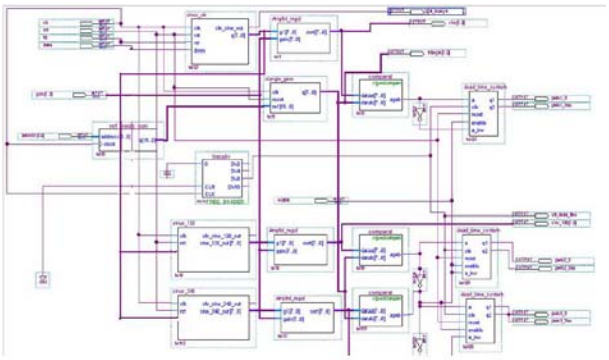

Fig.5 Top level entity of SPWM generator

Flow Status	Successful - Fri Sep 02 17:20:
Quartus II Version	7.2 Build 151 09/26/2007 SJ
Revision Name	frequencemeter
Top-level Entity Name	pwm_3_phase
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	No
Total logic elements	607 / 33,216 (2 %)
Total combinational functions	512 / 33,216 (2 %)
Dedicated logic registers	415 / 33,216 (1 %)
Total registers	415
Total pins	62 / 475 (13 %)
Total virtual pins	0
Total memory bits	17,168 / 483,840 (4 %)
Embedded Multiplier 9-bit elements	3 / 70 (4 %)
Total PLLs	0 / 4 (0 %)

Fig.6 Compiler flow summary

In order to verify the design functionality, 27 MHz is used as main clock frequency in simulation. Figures (7, 8, 9, and 10) show the functional simulation results with different entered specification. We can see that the three shifted modulating sine wave and carrier triangle wave are successfully generated. In figure 7 and figure8 the time cursors indicate 16.6127 ms (60Hz) , the zoom area of two complementary pulses shows that the dead time is properly inserted and by careful examination of the pulse widths in both figures 7 and 8 it is very clear that the pulse widths are changed by varying the modulation index from (98.4%to 62.9%). Since the carrier frequency in figure 8 is 1.35 KHz and in figure 9 is 450Hz, the number of pulses by one cycle in each figure is different.

Experimental results

The Cyclone device is configured by loading internal static random access memory (SRAM). Since SRAM is used in FPGAs, the configuration will be lost whenever power is removed, so the active serial programming is activated which means that the configuration of bit stream is downloaded into the Altera EPCS16 serial EEPROM chip. It provides non-volatile storage of the bit stream, so the information is retained even when the power supply of the DE2 board is turned off. When the board’s power is turned on, the configuration data in the EPCS16 device is automatically loaded into the Cyclone II FPGA [2, 12].

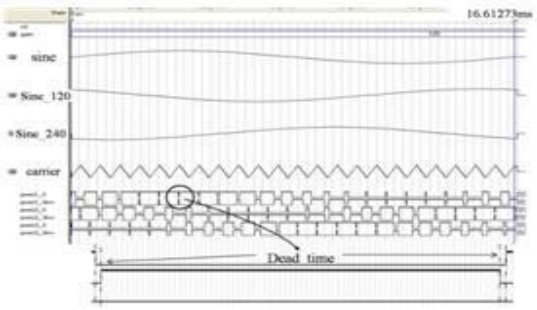

Fig.7 Functional simulation results, frequency_ref=60Hz, amplitude_ref=0.984, carrier frequency 1.35 kHz

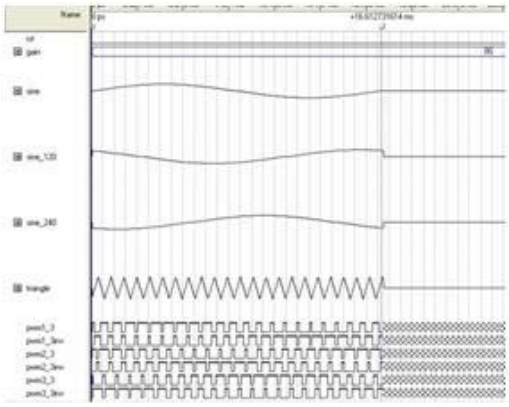

Fig.8 Functional simulation results, frequency_ref=60Hz, amplitude_ref=0.629, carrier frequency 1.35 kHz

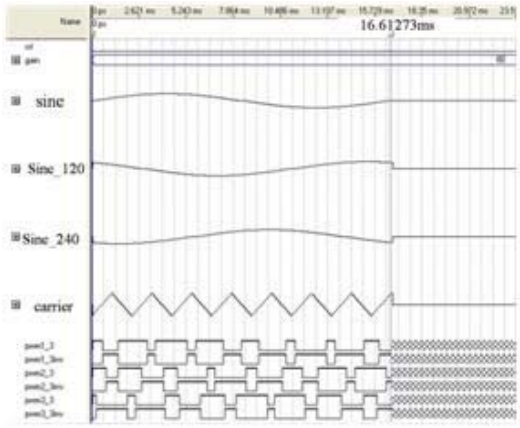

Fig.9 Functional simulation results, frequency_ref=60Hz, amplitude_ref=0.984, carrier frequency 450 Hz

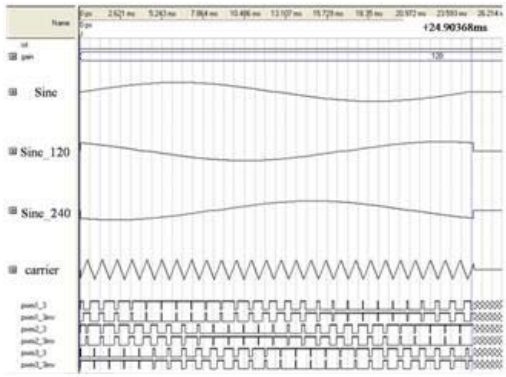

Fig.10 Functional simulation results, frequency_ref=40Hz, amplitude_ref=0.629, carrier frequency 750 Hz

Before programming the FPGA a pin assignment should be performed, so two debounced pushbuttons is used to increase and decrease the modulating wave signal frequency, four toggle switches to enter the carrier frequency, another eight switches to adjust the modulation index. The dead time is chosen by using a generic object in VHDL code, the six output pulses of SPWM are assigned to six pins of expansion headers with 3, 3 V output voltages, 27 MHz oscillator clock input is chosen as main clock for designed system. Figure 11 shows the hardware setup(PC, DE2 board and Tektronix oscilloscope) used in this experimental study to check the configurability and the real time operation of the design.

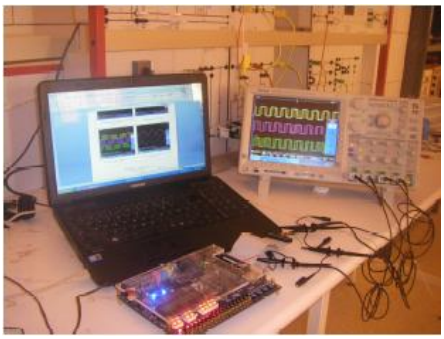

Fig.11 Hardware setup

Figures 12, 13, and 14 show the two complementary (PWM_H1, PWM_L1) SPWM pulses related to 1, 1.5 and 10Hz reference modulating frequency respectively, where the carrier frequency is set to 450Hz and the modulation index is set to 98.4%. The red square waveform, which envelope the blue PWM_H1 pulse, is generated to measure the frequency of modulating signal.

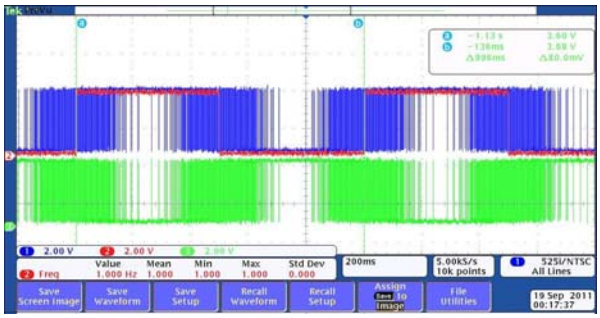

Fig.12 Generated complementary pulses with Frequency_ref=1Hz

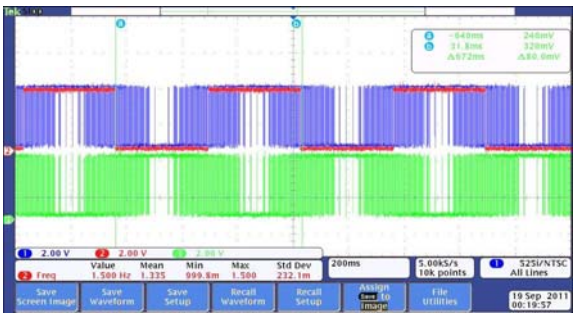

Fig.13 Generated complementary pulses with frequency_ref=1.5Hz

Fig.14 Generated two complementary pulses with frequency_ref=10.5Hz

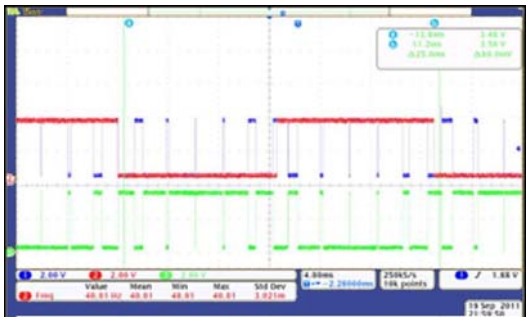

Fig.15 Generated complementary pulses with amplitude_ref=0.984

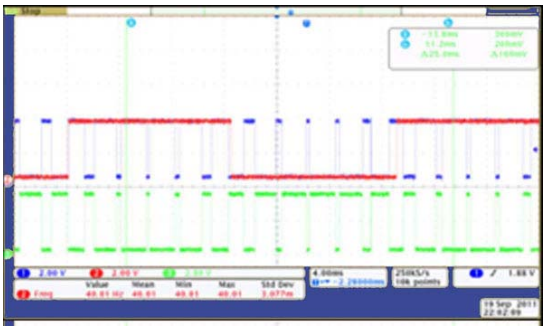

Fig.16 generated complementary pulses with amplitude_ref=0.795

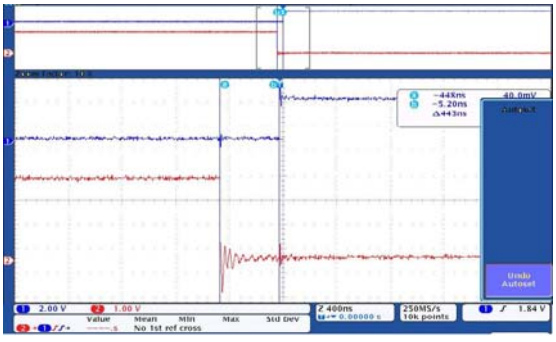

Fig.17 The dead time for turn-on and turn off

The figures 16 and 17 show the same (PWM_H1, PWM_L1) SPWM pulses but related respectively to 98.4% and 79.5% modulation index with 450 Hz carrier frequency and 40 Hz modulating frequency which explains clearly the difference in pulse width, and therefore the duty cycle is changed.

Figure 17 shows the measured delay between two complementary pulses which is 443ns. This value approximately equals the desired value specified in the design and simulation results 403ns. This little difference of 40ns which is very small is due to the signal propagation hardware delay.

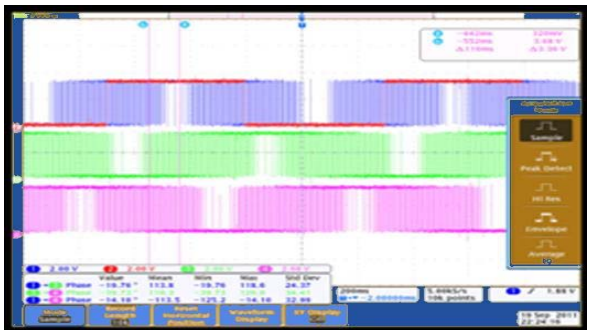

Fig.18 Generated 3 high pulses

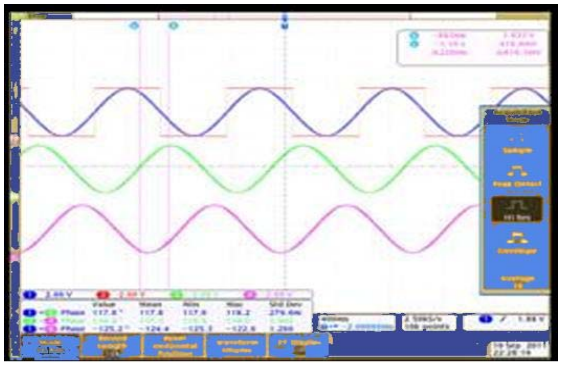

Fig.19 Three captured modulating signals using Hi Res acquisition mode.

The figure 18 shows the three SPWM high pulses PWM_H1, PWM_H2, PWM_H3. These pulses are identical with the same modulating frequency but shifted by 120^{o}.

The figure 20 is captured using Hi Res acquisition mode in Tektronix 4000 oscilloscope which can behave as a demodulator but in high carrier frequency (here it is set at 5.7kHz) with low modulating signal frequency 40Hz. It is obvious that the three reference modulating signals are extracted and a phase shift of 120° is present between each pair of signals. Hence the implemented SPWM module works properly and can be used for power 3 phase inverter control for AC machine control.

Conclusion

This paper presents the design and implementation of adjustable and configurable three-Phase SPWM with high resolution based on FPGA. A novel approach was introduce to designing such module in order to reduce the number of used logic elements (LEs) 607 in our case, 841 in [6], The constructed SPWM IC can generate a wide range of PWM output voltages and frequencies with high resolution. The aim of this hardware design is to contribute and to benefit of FPGA component in the control of electrical drives and in power electronic applications, subsequently enrich the libraries of predefined complex functions and circuits that have been tested and optimized to probable reuse and to speed up the design process employing the FPGA technology.

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