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FLL as Digital Period Synthesizer based on Binary Rate Multiplier Control

Abstract. *This article describes all digital Frequency Locked Loop (FLL) as period synthesizer, which uses Binary Rate Multiplier (BRM) in feedback for the output period control. Although BRM produces irregularities in its output, the synthesizer compensates them and generates the uniform pulse rate at the output. The functioning and realization of all parts of synthesizer are described. Particular significance was given to the description of the illustration of FLL functioning using realized model and to the application of FLL. The synthesizer for wide period range is presented.*

Streszczenie.*W artykule opisano cyfrowe FLL (ang. Frequency Locked Loop) wykorzystywane w syntezatorach okresu, wykorzystujące w sprzężeniu zwrotnym binarny mnożnik częstotliwości (ang. Binary Rate Multiplier).Syntezator kompensuje wszelkie nieprawidłowości wytwarzane przez BRM na wyjściu i generuje jednolitą częstotliwość impulsowania na wyjściu. Stworzono model opisujący funkcjonowanie FLL. Opisano realizację poszczególnych jego części . (**FLL w syntezatorze okresu cyfrowego – sterowanie z wykorzystaniem binarnego mnożnika częstotliwości***

Keywords: Frequency Locked Loop, Binary Rate Multiplier, Frequency Synthesizer,
Słowa kluczowe: FLL, BRM, syntezator częstotliwości.

Introduction

Generally, different kinds of generators, used in numerous frequency-based circuits and systems, produce the signals whose either frequencies or periods are linearly proportional to the control input. Both of them have some advantages in the corresponding applications.

Analog IC circuit Voltage Controlled Oscillator (VCO) found widely applications due to its property to generate the output frequency, which is linearly proportional to the input DC voltage. There are many applications, in both analog and digital frequency systems based on usage of VCO.

However, IC circuit BRM is all digital and it generates discrete output frequency which is also linearly proportional to the value of a digital control word. Since it is all digital, it appears, on the first sight, as more suitable circuit for frequency control applications, than VCO. However, BRM is not able to generate the uniform output pulse rate. The current output frequency of BRM changes around the average one, which is the only precise one. It is obvious that this disadvantage of BRM greatly narrows the field of its application, although BRM possesses powerful digital control ability.

In this article, the period synthesizer based on all digital Frequency Locked Loop (FLL) and BRM control is described. Although based on BRM frequency control, the FLL overcomes BRM disadvantage. The FLL generates uniform pulse rate and operates in wide frequency band.

The development of FLL as period synthesizer is based initially on ref. [1]. Closely related to this work are ref [2-6]. Ref. [7-9] are used in electronics implementation.

Organization and functioning of FLL based on BRM

The hybrid PLL, described in ref. [1], consists of Up-Down counter, D/A converter and VCO. In comparison with the hybrid PLL presented in ref. [1], the described FLL is all digital one. Precisely, D/A converter and voltage control oscillator (VCO) are changed by the programmable period generator and clock, building so the basic part of FLL described.

The organization of FLL based on BRM control, described in this work, is shown in Fig. 1. It consists of Up-Down counter, the programmable period generator, clock and BRM in the feedback.

Let us remember that BRM output frequency fopm of pulse rate Sopm, shown in Fig. 1, is linearly proportional to the decimal value Nmd of binary control word Nmb and that it can be expressed by the next equation:

$$fopm = fop * (Nmd / N\max) \tag{1}$$

where fop is the frequency of the output signal Sop and Nmax = 2^n ("n" is the number of bits of the control word Nmb). For instance, if binary control word is 8 bit, Nmax is 2^8 = 256. Providing that the current binary control word Nmb is, for instance, 01000000_2, Nmd = 64. In practice, this means that for every 256 pulses of pulse rate Sop, at the output of BRM will appear 64 pulses. It is obvious that the frequency fopm is the frequency fop multiplied by a factor of 64/256 = 1/4. That means that every fourth pulse of pulse rate Sop will appear at the output of BRM. By choosing other values for binary control word, it is possible to select any number of 256 pulses, so that ratio Nmd/Nmax may take discrete values from zero to one. Note however, that the pulse rate Sopm cannot be uniform, but at the same time, that BRM will always choose the best combination of Sop pulses. For instance, it is easy to conclude that 4-bits BRM CD 4089 will never generate the period, which is more than twice in comparison to the input period.

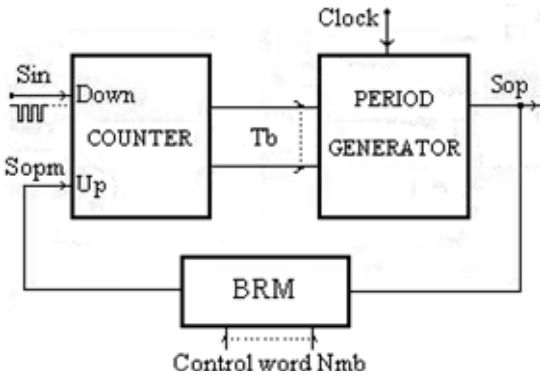

Fig. 1 Organization of FLL based on BRM

Programmable period generator produces pulse rate Sop whose period Top = 1/fop is integer of clock period tc, according to the next equation:

$$Top_{k+1} = Td_k * tc \tag{2}$$

where Td_k is the decimal value of binary content Tb_k of Up-Down counter at discrete time t_k and Top_{k+1} is the generated value of the output period at the next discrete time t_{k+1}. The

binary content Tb_k is preset to the period generator at the discrete time t_k.

Now it is possible to explain how FLL functions. Let us suppose temporarily that the ratio Nmd/Nmax is equal to one. This practically means that effect of BRM does not exist in circuit, shown in Fig. 1, and that the output pulse rate are connected directly to input Up of the Up-Down counter.

If frequency of Sin increases, the content Tb decreases and the frequency of Sop increases too, following the input frequency. If the input frequency decreases, the content Tb increases and the output frequency would also decrease and follow the input frequency. The content Tb, when FLL is in the stable state, represents actually the measured average input period and the output period at the same time. These two periods are equal, if the FLL is in the stable state.

If BRM effects are taken into account, when FLL is in the stable state, than the peiod Tin of the pulse rate Sin must be equal to the period Topm = 1/fopm. Substituting eq. (1) in Tin = 1/fopm and after that Top = 1/fop, it can be found out that:

$$Top = Tin * (Nmd / N\max) \tag{3}$$

It can be seen from eq. (3) that FLL based on BRM functions as the period synthesizer and that Top is linearly proportional to control word Nmd fed to BRM.

Realization of FLL components

The principal scheme of the programmable period generator (PPG) is shown in Fig. 2. PPG consists of Up-Down counter, RC differentiator and clock. The control word Tb defines the value of the output period of signal Sop in accordance to eq. (2). The mark Tb is taken from Fig. 1, just to demonstrate how PPG is connected to Up-Down counter, shown in Fig. 1.

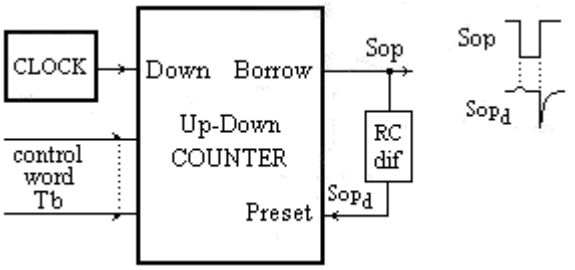

Fig. 2 The principal scheme of the programmable period generator

To describe the functioning of FLL, shown in Fig. 2, let us start from the point when the negative pulse Sop_d, acting at the input preset, enters control word Tb into PPG. This word Tb will appear at the output of Up-Down counter. Since clock pulses are fed into input Down and input Up is not used, Up-Down counter will count backwards, tending towards the content zero. Let us note that digital zero decoder is incorporated into Up-Down counter, as well as decoder of the maximum content of the Up-Down counter, but this last one is not used in this application. When the content of Up-Down counter reaches zero, the circuit generates negative pulse at the output Borrow, which is shown in Fig. 2. This pulse is actually one of the pulses of the output pulse rate Sop.

Every pulse of pulse rate Sop is differentiated on the rear edge, as it is shown in Fig. 2. Every differentiated pulse Sop_d starts entering the new control word Tb into Up-Down counter. This process repeats continuously. The result of this process is the generation of output pulse rate Sop, exactly in accordance to eq. (2).

Eight-bit PPG, shown in Fig. 2, consists of two 4-bits binary up-down counters CD 40193. If necessary, PPG might be extended to any number of counters CD 40193, forming so the corresponding capacity.

Eight bits up-down counter, shown in Fig. 1 also consists of two 4-bits binary up-down counters CD 40193. Note that according to the characteristics of CD 40193, the input pulses fed to Up and Down are not allowed to be simultaneous. The practical solution for this problem is described in ref. [4].

Eight bits BRM, shown in Fig. 1, consists of two 4-bits BRM CD 4089, cascaded in „Add" mode (see Data Sheet for CD 4089).

Illustration of FLL functioning

For better understanding how FLL, shown in Fig. 1, operates, let us suppose that the transfer function of BRM is equal to one (Ncw = Nmax) and that FLL is in the stable state. Two illustrations of Sin and Sop are shown in Fig. 3 and Fig. 4. It is supposed that some irregularities occur in pulse rate Sin. One pulse was lost in Fig. 3 and two additional pulses appeared in Fig. 4. The last edges of pulses Sop represent the discrete times t_1, t_2, t_3, ...t_k,.., whenstart generations of new pulse periods. Due to properties of FLL, the lost pulse of pulse rate Sin, shown in Fig. 3 will be recovered in pulse rate Sop. If we analyze what would happen when occurs the case like in Fig. 3, it might be concluded that the loss of pulse will increase the period Top_3 for one clock period tc, because the expected pulse was not fed to input Down and the content Tb increases for one. Providing that two pulses are lost in Sin, Top_3 will increase for two tc. In similar way, the black undesirable pulses in pulse rate Sin, shown in Fig. 4, will not appear in pulse rate Sop. But these two pulses, being fed to input Down, will decrease Top_3 for time value of two tc. Note that the changes of the period Top_3, in Fig. 3 and Fig. 4, may be in practice as negligible as we need. It is only necessary to choose the corresponding value of the clock period tc in order to adopt ratio between the output period Top and tc to the appropriate application.

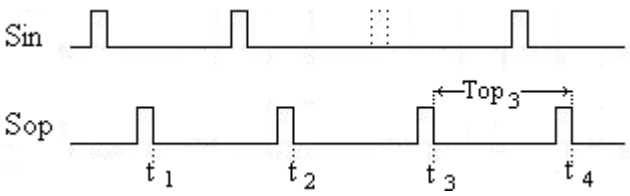

Fig. 3 The lost pulse is recovered; Top_3 is increased for tc

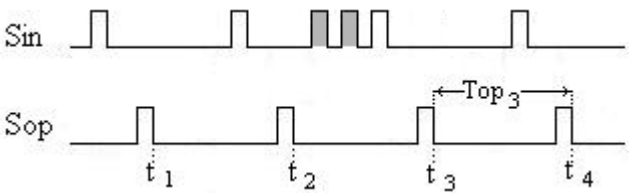

Fig. 4 Black pulses are eliminated; Top_3 is decreased for two tc

Another property of FLL is powerful ability to average period of non-uniform pulse rate. To illustrate operation of described digital FLL in the stable state, two oscilloscope pictures are shown in Figs. 5 and 6. The ratio between the average output period and clock period tc is purposely chosen to be small in Fig. 5 (only four), so that every step in real time operation may be followed, taking in account the effects of input pulses to the output period. The greatest output period in Fig. 5 consists of five clock periods.

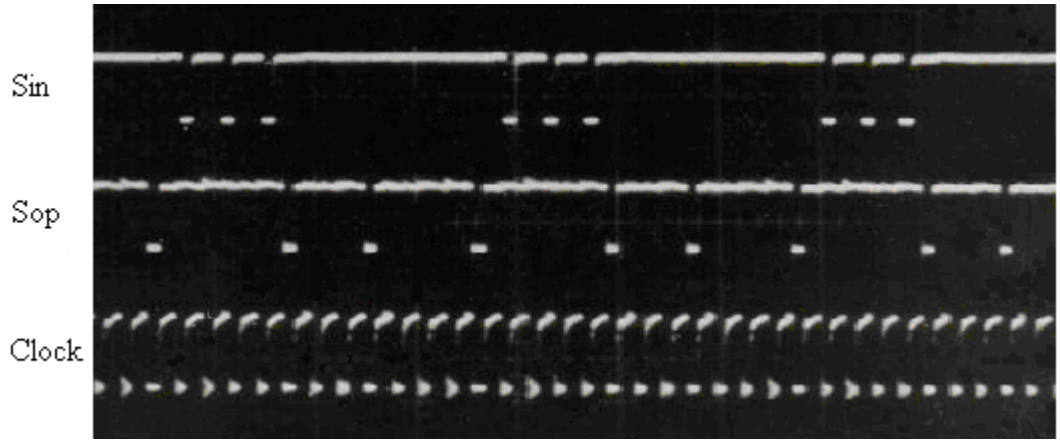

Fig. 5 Timing diagram of the FLL signals; the functioning of FLL may be followed in real time for every pulse

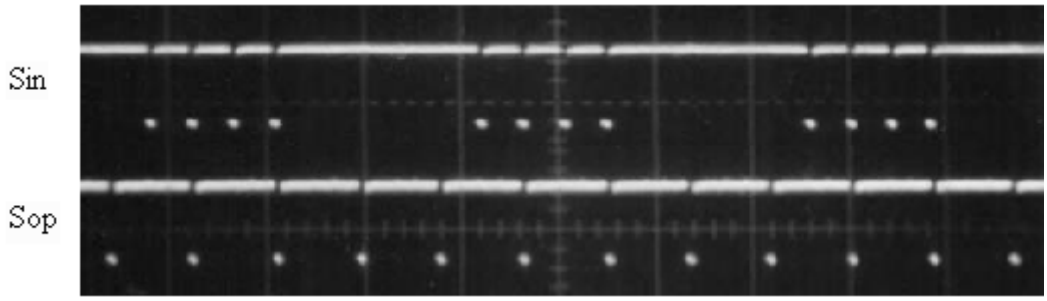

Fig. 6 The greater Top/tc produces the better averaging; Sin possesses high period irregularities

During the greatest output period, there come three pulses of Sin to Down and one pulse of Sop to Up. The result is that the next output period consists of three clock periods. At the end of this output period, one pulse of Sop comes to Up. The result is that the next output period consists of four periods. At last, new pulse of Sop comes to Up and makes the output period with five clock periods. The cycle is completed and from this point, it starts from the beginning. Note that the input frequency irregularities, shown in Fig. 5, are considerably greater than it is the case in the most real applications. In spite of that, the variation of the output period is only +/- one clock period tc, with regard to the average output period, which, in this case, is four clock period tc. Providing that, for the given input signal, the clock frequency is one thousand times greater than the average output frequency, the irregularities of the output periods should be only +/- one thousandth part of the average output period. This illustrates how powerful averaging capability possesses described FLL. In practice, the ratio Top/tc may be greater than one thousand, if necessary. The greater ratio of Top/tc produces the better resolution in generation of the output period.

The ratio between the clock frequency and the output frequency of Sop is increased only to about 15, in Fig. 6, but the averaging of the output period is better, no matter that the input period irregularities are very high.

The period irregularities of Sin in Figs 5 and 6 are considerably higher than the irregularities of BRM output pulse rate. Due to that fact, BRM appears as very suitable and powerful digital control circuit. If it is used in combination with the FLL described, the main BRM disadvantage, i.e. the period irregularities at its output, is overcome.

It was supposed that period irregularities belong to the input pulse rate Sin in Figs. 5 and 6. As to the manner of functioning of FLL, it is completely the same if the irregularities belong to Sin or Sop. The irregularities may appear in both Sin and Sop simultaneously and FLL would still work in the same way, successfully. This fact opens possibility to consider some other types of organization of FLL for different applications, with one, two or more BRM's, which are positioned in different places in FLL. All what is important is that their effects of irregularities to the FLL output are compensated. They will be always compensated if the pulse rates with irregularities are fed to one of inputs Up or Down of Up-Down counter.

Organization of the period synthesizer for wide band

Organization of the period synthesizer for wide band is shown in Fig. 7. In addition to the synthesizer shown in Fig. 1, this one has programmable counter with binary control word Ncb. Let us mark the decimal value of Ncb by Ncd and the period of output pulse rate Sco by Tco. Since the counter is frequency divider by Ncd, It follows that Tco = Tin * Ncd. Changing now Tco instead of Tin in eq. (3), it follows:

$$Top = Tin * Ncd * (Nmd / N\max) \tag{4}$$

Eq. (4) is valid only if FLL is in the stable state. It shows that the output period Top is linearly proportional to both control inputs Ncd and Nmd. Since Ncd takes integers 0, 1, 2, 3,… and Nmd takes values from zero to one, for any integer Ncd, due to Nmd, Top will be scaled from zero to one. Using additional programmable counter, the synthesizer is allowed to operate in wider range. Note that if Ncd increases for one, the period range would increase for Tin.

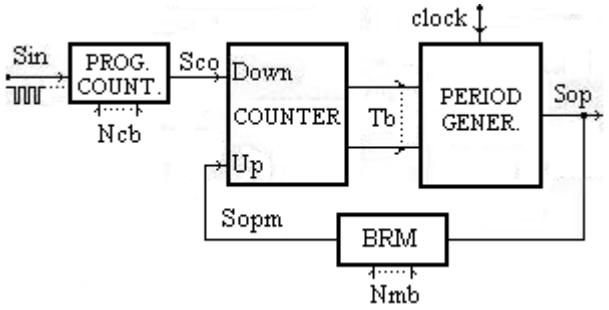

Fig. 7 Organization of the period synthesizer for wide range

Application of the synthesizer

FLL described, is suitable for wide range of applications in the field of telecommunication, measurements and control. Let us enumerate the main of them like the period and frequency synthesizers, the frequency multipliers and dividers, the different measurements, the recovery of lost pulses in pulse rate, the applications in noisy environments, the applications of period or frequency averaging, the applications with frequency subtraction and/or addition, control applications and the others. Due to property to eliminate irregularities of BRM output, the field of application of FLL together with BRM is increased. FLL with BRM in the feedback opens possibility for solving new kind of tasks in simple way and with high quality.

Number of bits of Up-Down counter and the period generator, i.e. FLL capacity, depends on the ratio between the maximum used period Top and tc. Clock period tc is determined so that the minimum used period Top is generated with satisfactory resolution. The higher capacity enables better averaging regulation. However, the greater capacity decreases the speed and increases the transient time of FLL, necessary to come to the stable state. At the same time, the greater capacity, the better filter performance of FLL. It is obvious that, depending on the given task, one should carefully choose the construction parameters of FLL, making all the time trade off in order to adopt FLL to the specific application.

The number of bits of BRM control word depends on how many discrete periods it is necessary to generate to cover the required frequency band.

The number of bits and the programmable counter in the period synthesizer, shown in Fig. 7, depends on kind of application, i.e. on the required frequency band.

Besides the two models off FLL as the period synthesizer, shown in Figs. 1 and 7, there are some other combinations of similar models, which one could easily make. They might be made by combining the positions of BRM and the programmable binary counter in the basic FLL circuit. They may be positioned together or separately in the feedback, or in front of Up-Down counter. BRM will always make scaling of the output frequency or period, multiplying by factor between zero and one. The programmable binary counter will make the wider range. For any of these combinations it is necessary to analyze the characteristics of the output pulse rate. Some of them will enable linear change of frequency and the others will enable linear change of periods at the output of the synthesizer.

All digital FLL, described in this work, is more applicable in measurement and control than hybrid PLL described in ref. [1]. Since it is all digital, FLL is more stable and more precise in work. Note that the precision of FLL is defined primarily by clock frequency, which might be controlled by quartz, if it is necessary.

Instead of generation of pulse rate, the content in the period generator may be continuously decoded before FLL reaches the stable state. According to the digital states of the content, different signal may be generated to control a number of processes, which will on the other side effect to the frequencies of the FLL input signals. In such feedback control applications, all parts of the complex system are incorporated into the FLL and represent the parts of an extended FLL, like in ref. [4].

Conclusion

The description and illustrations of the realized circuits have demonstrated ability to construct simple all digital FLL as the period synthesizer with powerful performances, suitable for a wide range of applications.

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