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Electromagnetic disturbances elimination methods in microprocessor systems

Abstract. *The paper deals with noise suppression methods in microprocessor systems. Two methods are presented: hardware (LC decoupling) and software (microcontroller digital clock sources management). Advantages and disadvantages of each method are presented. The tests are conducted on a real, battery operated mobile device with an AVR microcontroller onboard. Efficient noise suppression for proposed methods is proven.*

Streszczenie. *Artykuł dotyczy metod tłumienia szumów w systemach mikroprocesorowych. Przedstawione zostały dwie metody: sprzętowa (odsprzęganie za pomocą elementów LC) oraz programowa (zarządzanie pracą wewnętrznych źródeł sygnałów zegarowych). Zostaną przedstawione zarówno zalety jak i wady poszczególnych rozwiązań. Przeprowadzone badania zostały oparte na rzeczywistym, zasilanym bateryjnie urządzeniu wyposażonym w mikrokontroler z rodziny AVR. Wykazano skuteczną ochronę przeciwzakłóceniową proponowanych metod.* (***Metody eliminacji zakłóceń elektromagnetycznych w systemach mikroprocesorowych***).

Keywords: digital noise, ripple, noise suppression, decoupling, internal ADC, microcontroller.
Słowa kluczowe: szum cyfrowy, tętnienia, tłumienie szumu, odprzęganie, wewnętrzny przetwornik A/C, mikrokontroler.

Introduction

Electromagnetic disturbances are also very common in digital systems. However these systems are more resistant than the analog circuits, their malfunction may cause more serious side effects like system hang up or improper control of an industrial process. Mentioned digital systems (especially microprocessor systems) are also very significant source of any kind of electromagnetic disturbances due to their principles of operation - beginning from square wave clock sources, ending with long, multi-ended tracks on PCB boards. These tracks can be treated as the antennas emitting the whole spectrum of electromagnetic waves towards the other circuits on a board. Most of the modern microcontrollers are equipped with many peripherals like timers/counters, serial bus controllers and AD converters. These last are especially susceptible to disturbances of digital origin. Due to the fact that the microcontrollers are mixed-signal circuits significant couplings occur between the digital and analog parts. Some of the ways of suppressing such couplings will be presented in the following paper.

Hardware noise suppression methods

The most intuitive method of suppressing the noise in analog circuits is decoupling them from the digital parts and switching power supplies. Due to the fact that the modern power supplies are mostly switching power converters there exists a significant high-frequency ripple within the supply [3]. Most of the built-in A/D converters are based on successive approximation registers, so they are not resistant to such disturbances [2]. Even the dual-slope converters are not resistant to noise coming from high-speed digital devices [2]. That is why one should assure the least digital noise level as possible.

Decoupling the ADC converters supply from digital clocks and switching power supplies ripples can be made in various ways. The most common are: LC filtering, signal and power ground separation (including galvanic isolation) and shielding. Not all of these methods have to be used in parallel. It commonly happens that we are not able to assure them due to the project design conditions.

Especially the galvanic isolation between CPU and the analog circuits can present some problems due to the independent power supplies and optical coupling. More simpler way can be proposed. We should assume having several independent supply grounds e.g. power, digital and analog. Schematics design and the PCB layout should be done as if all of the grounds are separate. They are joined only in one point at the decoupling capacitor pin in the main power supply. Additionally there should be poured a ground polygon on the PCB board corresponding to appropriate circuit.

The passive LC/RC filters should be also applied into the supply of analog circuits. Some of the manufacturers advice using local independent filters for each IC. The LC or RC structure choice depends mainly on the disrupting signal frequency response and the analog circuit power consumption. The schematics of circuit including a LC decoupling and digital-to-analog grounds separation is presented in figure 1.

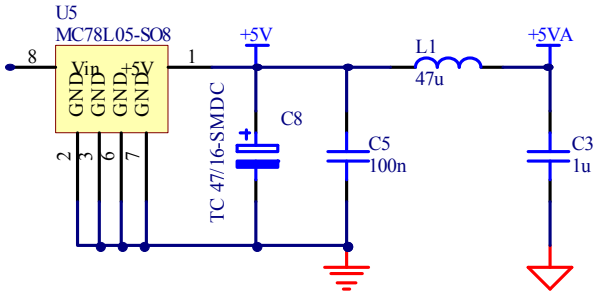

Figure. 1. Analog power supply LC filtering with ground separation schematics.

The PCB design should also be done properly. The L and C elements should be placed as near as possible to the decoupled IC. A decoupling of the ATMega128's [4] analog power supply is presented in figure 2.

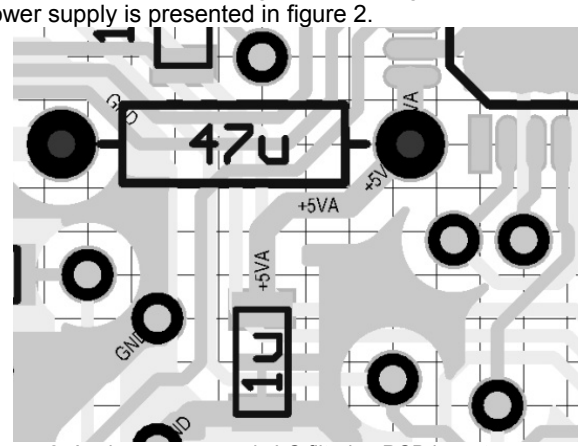

Figure. 2. Analog power supply LC filtering PCB layout.

Presented above methods will be tested along with the described below software algorithms.

Software noise suppression methods

The paper deals with noise suppression methods in microprocessor systems. These system are very specific and require some sophisticated hardware-software mechanisms. One will present these mechanisms, which are implemented in almost every AVR [4] microcontroller.

As it was mentioned above modern microcontrollers consist of the CPU core and some additional internal peripherals like A/D converters. It is obvious that they are made within one structure, so the coupling between the analog and digital parts occur. The Atmel company provides their microcontrollers with a special mechanism that allows to disable most of the digital clocks during the A/D conversion [4]. Due to the fact, that the A/D converters can also be interrupt driven [4], the whole algorithm turns to be not so complicated. One should provide few steps and make some configuration before executing the "start conversion" command.

Let's assume that one requires analog input signal sampling with the frequency equal to $f_d = 1/T_d$. The CPU hardware initialization algorithm is as follows:

- turn on and configure the AD converter (write appropriate values to ADCSRA register),
- configure appropriate timer/counter to execute the interrupt every T_d and unmask the corresponding interrupt,
- inside the timer interrupt routine: set CPU sleep mode to "ADC Noise Reduction", mask all other interrupts and enter the sleep mode (the ADC will start a conversion once the CPU has been halted),
- inside the ADC interrupt routine: reenable all other interrupts, restore the default sleep mode, write the conversion result.

So described method disables the CPU from functioning during the AD converter operation. This causes the apparent CPU load come into existence. The additional utilization can be described by the following equation:

$$L_{ADC\ NR} = \frac{N_{ADC}}{N_T} \tag{1}$$

where: N_{ADC} – number of clock cycles required to perform the AD conversion, N_T – number of clock cycles between the conversions (timer overflow or compare).

Let's assume that the CPU is clocked with the maximum speed of 16MHz. The maximum ADC conversion time (equal to the CPU idle time) for the ATMega128 does not exceed 260 µs [4]. The apparent CPU load (1) can be represented in figure 3.

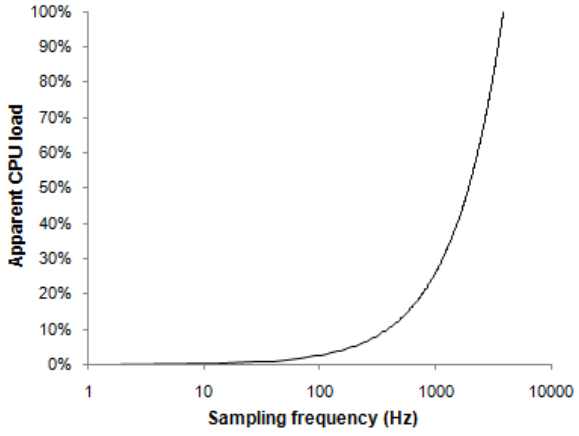

Figure. 3. Apparent CPU load vs. sampling frequency.

Basing on the equation (1) and the CPU datasheet [4] the maximum sampling frequency allowed using the ADC Noise Reduction Mode is only 3846 Hz, which is the ¼ of maximum AD converter speed. Moreover the effective sampling frequency, when the CPU load lowers to 10% is only 385 Hz.

Application of the noise suppression methods

The tests of presented above algorithms and methods were conducted on a mobile, battery operated CPU system based on the ATMega128 microcontroller. The PCB board was designed according to figure 2. The measured quantity was the battery voltage, which was needed for battery condition approximation and -dV sensing during its charging process. Due to the sensitivity of the -dV method any additional noise coming from the running CPU could cause improper end-time detection and shorten a battery life [1]. During the tests the device was supplied from external power supply and no charging occurred. The determinant of noise suppression accuracy is assumed to be the coefficient of variation, equal to the standard deviation divided by the mean value. The sampling frequency in this case was 1 Hz, 30 following samples were taken into account during the calculation.

Table 1. Test results of noise suppression methods.

Test conditions	Coefficient of variation
No LC network, no ADC noise reduction	1.27%
LC network, no ADC noise reduction	0.96%
LC network, ADC noise reduction enabled	0.42%

The analysis of the data presented in Table 1 shows that using the LC network and turning on the ADC Noise Reduction Mode significantly decreases the noise level. Best results are obtained during the combination of these two methods.

Conclusions

Conducted research shows that the problem of internal noise disturbances within the measurement systems is very significant. During the system design procedure one should be aware of any couplings between the analog, digital and supply (especially switching) circuits and apply as many decoupling methods, adapted to the particular solution, as possible. Also the emission of any disturbances should be decreased by disabling any possible digital clock sources as well as avoiding the switching power supplies to operate during the data acquisition. However, some disadvantages of presented methods must be pointed. The LC network and especially the galvanic isolation causes more complicated and expensive circuits. Turning off the digital clocks including the CPU core significantly reduces the CPU performance and causes the maximum ADC throughput decrease.

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