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A Multi-Level Inverter for Ultra High Speed PM Motor Control Application

Abstract. *The general concepts of multi-level technology involve utilizing a higher number of semiconductor devices to achieve higher power conversion, eliminate harmonics and reduce the switching loss. This paper is concerned with applying multi-level techniques to a PM motor to achieve ultra high speed features with better quality waveforms and less dv/dt for an aerospace application. A three-level diode clamped inverter is used to control a low inductance, ultra high speed PM motor with an integrated designed load compressor. Results from a 15kW experimental prototype are presented to validate the reliability of the inverter, the stability of the DC-link voltage balance and the practicality of vector control in this application.*

Streszczenie. *W artykule opisano zastosowanie wielopoziomowego przekształtnika do sterowania silnikiem z magnesami trwałymi. Osiągnięto bardzo dobra jakość kształtu sygnału napięciowego I małe dV/dt. Dzięki temu uzyskano ultra duża szybkość do zastosowań lotniczych.* (***Wielopoziomowy przekształtnik w zastosowaniu do sterowania silnikami PM o dużych prędkościach obrotowych)***

Keywords: neutral point clamped inverter (NPC), space vector modulation (SVM), ultra high speed PM motor and vector control
Słowa kluczowe: silnik z magnesami trwałymi, przekształtnik wielopoziomowy.

Introduction

In recent decades, the multi-level topology gains an increasing attention due to its inherent advantages in high voltage power conversion, reducing the dv/dt stresses on semiconductor devices, producing better quality waveforms with less harmonics and reducing the electromagnetic compatibility (EMC) concerns [1]-[6] .

There are three basic types of multi-level topologies (diode clamped, capacitor clamped and cascaded H-bridge). The cascaded multi-level converter was introduced by Baker and Bannister in 1975 [7]. The capacitor clamped multi-level converter was introduced by Foch in 1992 [8] and the diode clamped multi-level converter was first proposed by Nabae in 1981 [9].

The aim of this paper is to present a comparative study of the DC-AC inverter topologies for an experimental ultra high speed, low inductance and low resistance motor used in an aerospace compressor application. Since the low inductance and low resistance of the target ultra high speed PM motor results in sensitivity to change in terminal voltage and the ultra high speed results a high output frequency (66845rpm for PM motor and 1.114kHz for the inverter output frequency), it is interesting to look at the potential of utilizing multi-level topology to improve the waveform quality and reduce the switching frequency and switching loss of each semiconductor devices.

The diode clamped multi-level inverter (Fig 1) has been adopted due to the appropriateness in this application [10]-[12]. Details of the space vector modulation and vector control algorithm are given in this paper. The practical multi-level inverter rig and the experimental results using a 15kW, one pole pairs, ultra high speed (up to 66845rpm), low inductance PM motor are presented to validate the method (this project is funded by the European Frame Project, FP6 MOET, hence the motor parameters cannot be provided for security reasons).

Space Vector Modulation

Compared to traditional two-level inverter, a three-level diode clamped inverter (Fig 1) consists of two additional clamping diodes at each inverter leg, the DC-link and all switching legs are connected to a common neutral point. Hence the load terminals are able to be connected to either the positive input, negative input or neutral point and the diode clamp topology is also known as the neutral point clamped (NPC) topology [1] [2].

Fig 1 shows a three-level NPC which has two capacitors that divide the DC supply into two equal voltages with proper control strategy [13]-[15]. The voltages across the two capacitors are E and –E respectively. It can be concluded that an N-level NPC can produce N-level phase voltage levels, 2N-1 line to line voltage levels and has N-1 capacitors to support the DC link. The switching frequency and dv/dt of each semiconductor devices is obviously reduced than traditional two-level inverter, which significantly reduce the switching loss and is suitable for ultra high machine control application.

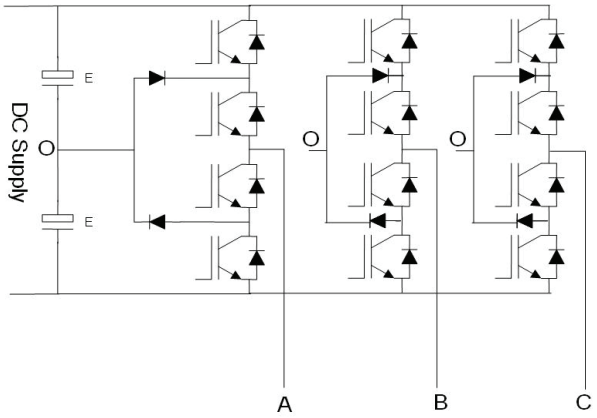

Fig.1. Diode Clamped Three-Level Inverter (NPC)

To generate the desired output voltage waveform, two modulation schemes are considered, carrier based PWM and space vector modulation (SVM) [1] [2]. Carrier based PWM is widely used in a variety of industrial applications [16]-[20]. Furthermore, carrier based PWM also provides natural balancing of the DC-link capacitor voltages. The SVM directly uses the vector defined in the vector space in modulation and it performs the balanced capacitor voltages with extra control strategy [14]. SVM inherently advantages in switching state and sequence control. Hence it is suitable for the DSP implementation [21]. Considering all advantages mentioned above, the SVM is used in this project [22].

Referring to Fig 1, the output voltage space vectors for a typical three phase, three-level NPC can be defined as:

$$V_o(t) = \frac{2}{3}\left[V_{AO}(t) + V_{BO}(t)e^{j2\pi/3} + V_{CO}(t)e^{j4\pi/3}\right]$$

(1) $$= \frac{2}{3}E\left[S_A e^{j0} + S_B e^{j2\pi/3} + S_C e^{j4\pi/3}\right] \quad)$$

$$= \mathrm{Re}[V_o(t)] + j \cdot \mathrm{Im}[V_o(t)]$$

(2) $$\mathrm{Re}[V_o(t)] = \frac{2}{3}E\left[S_A - \frac{1}{2}S_B - \frac{1}{2}S_C\right]$$

(3) $$\mathrm{Im}[V_o(t)] = \frac{1}{\sqrt{3}}E[S_B - S_C]$$

Table I Three-level NPC modulation states

Space Vector	Switching State		Vector Classification	Vector Magnitude
V0	PPP OOO NNN		Zero vector	0
	P type	N type		
V1	POO	ONN	Small Vector	$\frac{1}{3}V_{dc}$
V2	PPO	OON		
V3	OPO	NON		
V4	OPP	NOO		
V5	OOP	NNO		
V6	POP	ONO		
V7	PON		Medium Vector	$\frac{1}{\sqrt{3}}V_{dc}$
V8	OPN			
V9	NPO			
V10	NOP			
V11	ONP			
V12	PNO			
V13	PNN		Large Vector	$\frac{2}{3}V_{dc}$
V14	PPN			
V15	NPN			
V16	NPP			
V17	NNP			
V18	PNP			

P (N) type states means positive (negative) DC-link voltages are used in modulation.

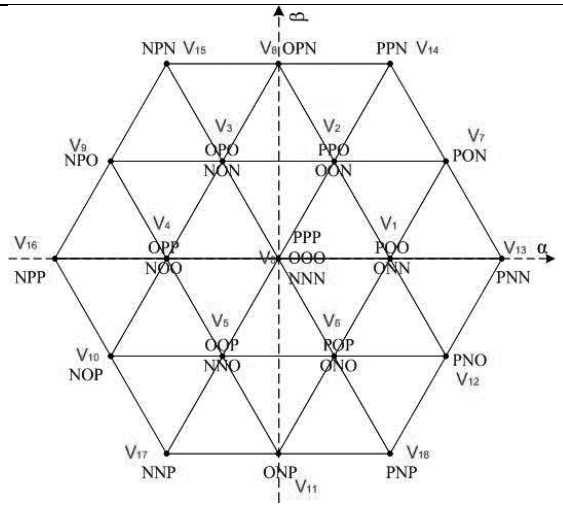

Fig. 2. Output voltage vector in SVM

Obviously, all twenty-seven possible voltage states can be formed, as listed in Table I. The corresponding voltage vectors are plotted in Fig 2. In Fig 2, the switching states plotted at the inner hexagon have redundant switching states, which can be named as either P type or N type [5]. These redundancies are important for the DC-link capacitors balancing.

To facilitate the duty cycle calculations [1] [2] [23], the vector space shown in Fig 2 is divided into six equal sectors and four triangles in each 60o sector (Fig 3). In every triangle, the target voltage vector is synthesized by the three adjacent fixed states. To achieve the minimal number of switching events between adjacent states and to minimize the impact on the neutral point voltage deviation, a seven-segment switching sequence can be adopted for the SVM. For the target vector position shown in Fig 4, the seven-segment switching sequence is shown in Table II.

In a three-level NPC, only the commutations between P and O states or N and O state are legal. Commutations between P state and N state are not allowed because they result in all four switches (per output leg) changing state, resulting in non-equal dynamic voltages and high switching loss. To investigate the commutation process, the output leg is assumed to commutate from P state to O state and the load current is assumed to be constant during commutation.

TABLE II seven-segment switching sequence

Sequence	State
1st	ONN
2nd	PNN
3rd	PON
4th	POO
5th	PON
6th	PNN
7th	ONN

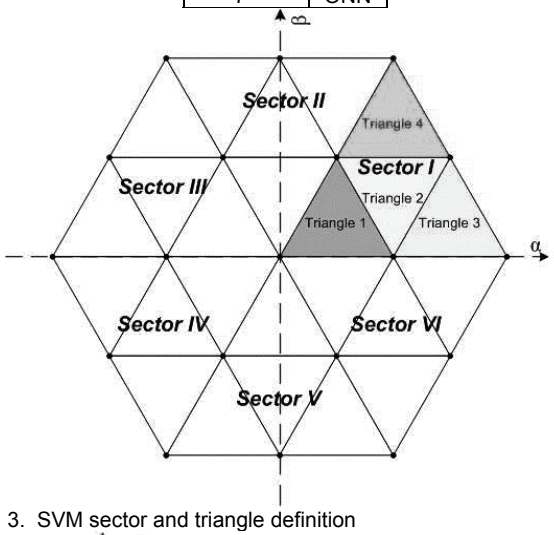

Fig. 3. SVM sector and triangle definition

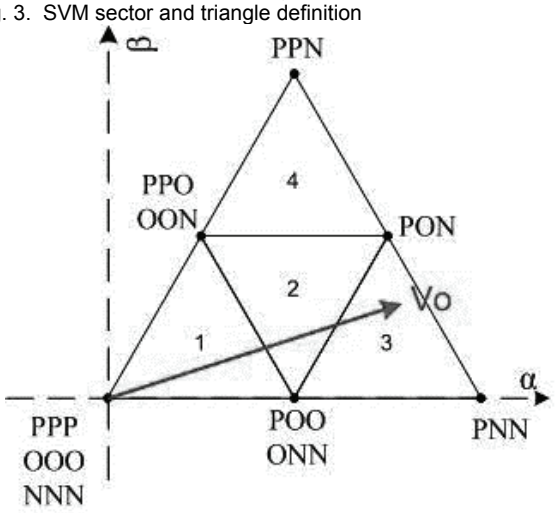

Fig. 4. Seven-segment switching sequence

The target output voltage vector is synthesized using the nearest three states in each modulation triangle as shown in Fig 4. The related duty cycles can then be determined by decomposing both target output vector and the fixed states into the real and imaginary axies. Making an assumption that the three nearest fixed states and their relative duty cycles are V1, V2, V3 and t1, t2, t3 respectively, the duty cycles can be calculated by following equations:

(4) $$V_o = V_o\_re + j\omega V_o\_im$$

(5) $$\begin{cases} V_o\_re = V_1\_re \cdot t_1 + V_2\_re \cdot t_2 + V_3\_re \cdot t_3 \\ V_o\_im = V_1\_im \cdot t_1 + V_2\_im \cdot t_2 + V_3\_im \cdot t_3 \\ t_1 + t_2 + t_3 = 1 \end{cases}$$

In above equations, the subscripts _re and _im represent the components along the real (α) and imaginary (β) axies as shown in Fig 4.

The voltages across two DC-link capacitors can be controlled by adjusting the period distribution between P type and N type states shown in Fig 4 (in the inner hexagon) in each modulation cycle. In the seven-segment switching sequence, there is always a small vector in every modulation cycle. Hence the capacitor voltages can be controlled in any sector [1] [2] [5].

Vector control for ultra high speed PM motor

In this paper, vector control has been adopted to achieve ultra high speed (up to 7000rad/s, which is 66845rpm) control of the low resistance and low inductance PM motor [24] [25]. The basic vector control algorithm can be expressed as follows:

(6) $$\left.\begin{array}{l} Gc = (kp \cdot s + ki)/s \\ Gs = kt/(Js + B) \\ 1 + Gc \cdot Gs = 0 \end{array}\right\} \Rightarrow speed\ \ loop$$

(7) $$\left.\begin{array}{l} Gc = (kp \cdot s + ki)/s \\ Gs = 1/(Ls + R) \\ 1 + Gc \cdot Gs = 0 \end{array}\right\} \Rightarrow current\ \ loop$$

In equations (6) and (7), J, B, kt, L and R are the rotor inertia, friction, torque constant, equivalent inductance and resistance respectively. Therefore the PI controller parameters (kp & ki) can be calculated using (6) and (7) for a damping factor ξ=0.707 and proper selected bandwidth ωn for both speed loop and current loops. In this work, MATLAB simulation has been utilized to validate the PI controller design. The MATLAB simulation scheme is plotted as shown in Fig 5 and the simulation results are shown in Fig 6.

In this application, following situations must be taken into consideration:

- the ultra high speed motor is integral designed with the load compressor and the load compressor cannot be regarded as a constant torque source but it follows a fan curve. Hence the PM motor outputs maximum torque at maximum speed.
- the speed loop response cannot be designed very fast due to the ultra high speed motor cannot allows an high acceleration mechanically.
- the motor need to be controlled with almost zero speed overshoot as required;
- due to the low inductance and low resistance design, the R, S parameters are not accurate and immeasurable with the lab condition;
- due to the low inductance and low resistance design and high frequency application, the equivalent reactance of the transmission path (such as power cables) significant affect the motor control performance;
- due to the motor works at ultra high speed, the motor internal temperature can reach up to 150oC within 2 minutes, hence results the motor parameters varying at a wide range according to the speed;
- cogging effect significantly affect the motor dynamic performance when speed less than 2000rad/s (19098rpm).

With all above consideration:

- the speed loop is designed with a slow dynamic response (bandwidth ≈ 0.01Hz) which only allows the motor accelerate slowly;
- due to the speed changing in every DSP interrupt routine increase rapidly, an speed compensation is utilized in practical application to ensure the speed information follows the actual motor speed;
- the minimum operating speed is 2000rad/s to avoid significant cogging effect;
- the current loop (bandwidth ≈ 600 Hz) need to be designed much faster than the speed loop for a good dynamic performance;
- due to the high output frequency, the transmission path reactance cannot be neglect. The output voltage compensation in DSP is utilized in practical application to minimum the voltage drop on the transmission path (7% voltage drop per meter is measured at the transmission cable in practical rig).

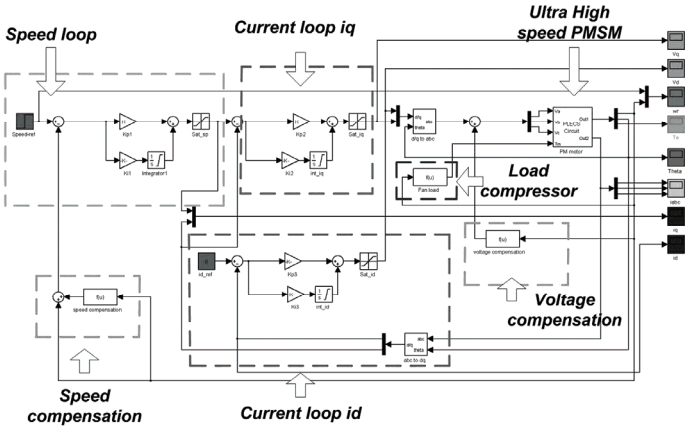

Fig. 5. MATLAB simulation scheme

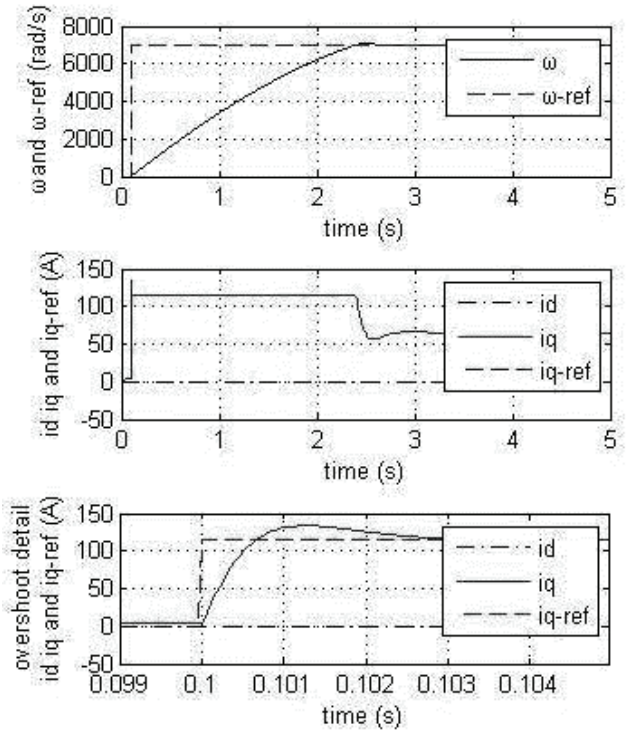

Fig. 6. Vector control simulation result

From Fig 6, it is clear that a 7000rad/s step change was given as the reference speed at 0.1s. The speed loop limits the overshoot in motor speed to almost zero and only allows a gradually acceleration as required by the application. Furthermore, the current loop fully follows the reference current with an acceptable overshoot (id and iq are limited under 130A by the controller in MATLAB simulation).

Experimental results

The schematic of the experimental system is shown in Fig 7. Since the resistance and inductance of the ultra high speed PM motor are small, low ESL & ESR DC-link capacitors are utilized to reduce the inverter reactance. Copper power planes and copper bus bars are also used to reduce the connection reactance between devices. The skin effect of the transmission path is taken into consideration in practical application.

The control system includes gate drivers, DSP & FPGA, interface card, resolver to digital (R/D) converter, voltage transducers, current transducers and isolated 28V~5V & 28V~±15V power supplies for aerospace application (Fig 8).

Furthermore, the ancillary components (Fig 9) consist of the heatsink blower, dust protector, water coolant system and bleed air coolant.

- The two blowers are used to cool the heatsink;
- The mechanical switch is connected to the main DC input;
- Two 10cm diameter windows (on the side of the cabinet) with dust protectors allow air flow to assist heat removal which also protecting the whole system from dust;
- The water coolant system allows the target motor and compressor temperatures to be controlled during operation;
- The bleed air coolant is necessary in motor spinning and the air pressure need to be controlled at two bars.

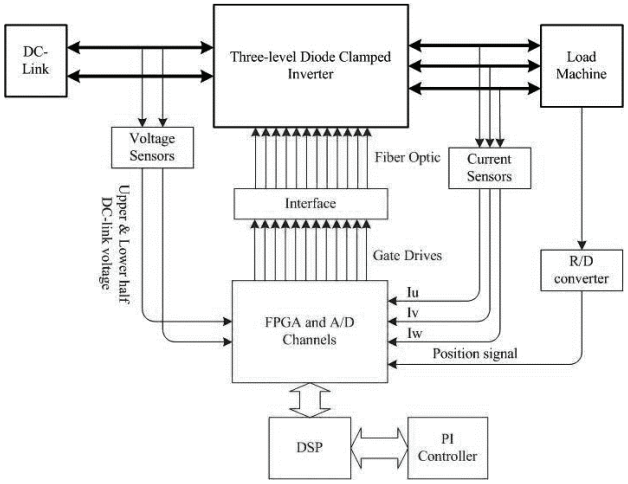

Fig. 7. Experimental system schematics

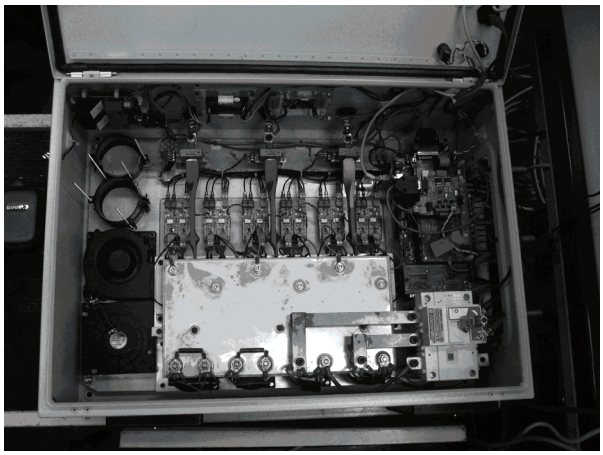

Fig. 8. Inverter rig

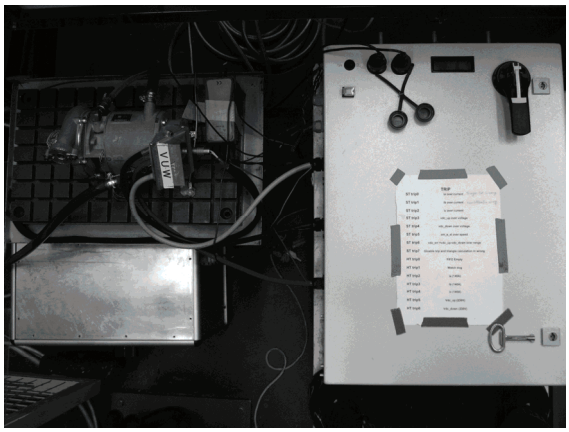

Fig. 9. Inverter rig and ancillary components

The experimental results are shown for two operating conditions to demonstrate the reliability of the inverter rig and the validity of the PI control design. The following experimental results include both inverter variables (DC-link voltages, output line to line voltage Vab and motor phase current ia) and control parameters (ω, ω_ref, id, iq, iq_ref, vd_ref and vq_ref). Waveforms are plotted in two groups according to the speed information (4000rad/s and 7000rad/s) from Fig 10 to 13 (control parameters are negative due to the motor spinning at the opposite direction as defined in modulation).

- 4000rad/s (38200rpm) is a nominal spinning speed in this application. The inverter modulation index is 36% when speed reaches 4000rad/s. From the following waveforms, it is obvious that:
  - the PM motor is controlled at 4000rad/s with load compressor as required
  - the inverter line to line output voltage consists of three voltage levels due to the modulation index is only 36%
  - the load current is sinusoidal shaped
  - id is controlled to zero to as required by the PM motor
  - iq is controlled centre with its reference value. The ultra high speed PM motor output constant torque to the load compressor at 4000rad/s as required
  - both top and bottom DC link capacitor voltages are balanced DC values (Fig 11)
- 7000rad/s (66845rpm) reaches the maximum speed of application. The inverter modulation index is 62% at 7000rad/s. From the following waveforms, it is obvious that:
  - the PM motor can be controlled at the maximum speed 7000rad/s with load compressor
  - the inverter line to line output voltage consists of five voltage levels. Better waveform quality is obtained with the stair case output voltage
  - the load current is sinusoidal shaped but higher amplitude than 4000rad/s
  - id is controlled to zero as required by the PM motor
  - iq is controlled centre with its reference value. The ultra high speed PM motor output constant torque to the load compressor at 7000rad/s and the maximum torque is obtained at this speed due to the fan curve features of the torque
  - both top and bottom DC link capacitor voltages are balanced DC values but a voltage drop can be seen from Fig 13 due to the current results voltage drop in the supply

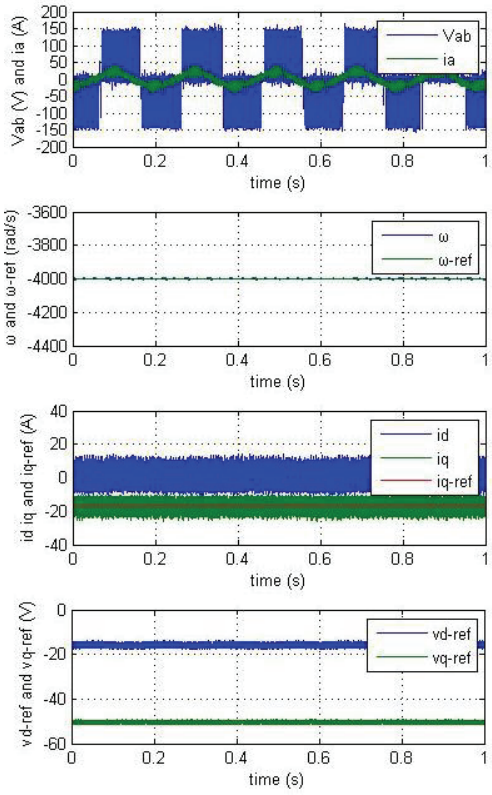

Fig 10 Experimental results at 4000rad/s

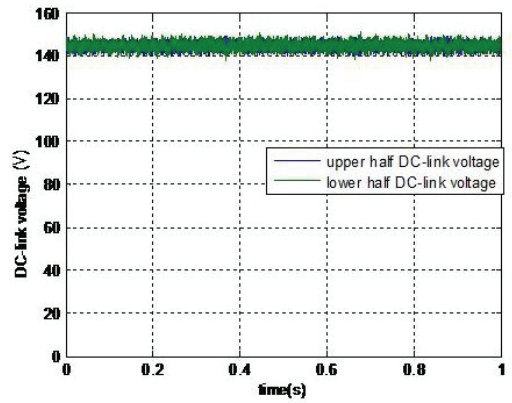

Fig 11 DC-link voltages at 4000rad/s

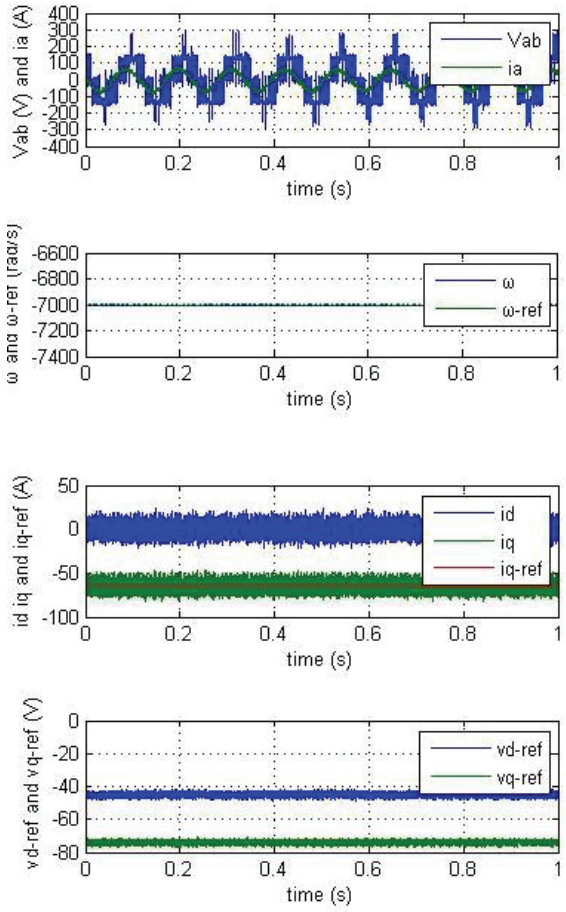

Fig 12 Experimental results at 7000rad/s

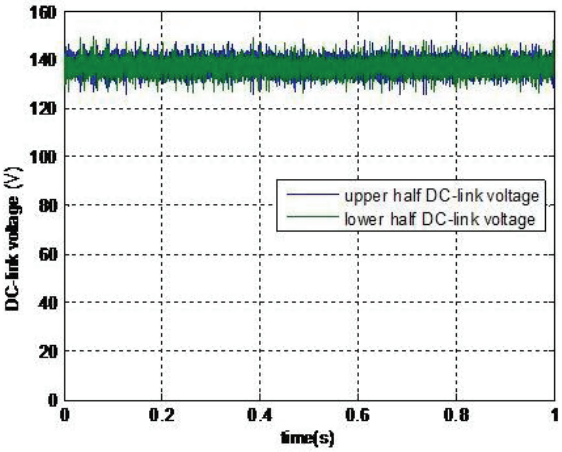

Fig 13 DC-link voltages at 7000rad/s

Conclusion

In this paper, the SVM of a three-level diode clamped inverter and the vector control of a ultra high speed PM machine vector control are introduced. The extremely low resistance and inductance of the motor lead to sensitivity with terminal voltage change. Hence the hardware design plays an important role in the practical inverter rig. As shown in section IV, the experimental results have demonstrated that the motor can be controlled

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