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The Design of the Signal Generator Circuit for Single-Phase Industrial Frequency Power Based on XC2C64A

Abstract. *The paper mainly introduces the new signal generator circuit of industrial frequency power based on XC2C64A, which focus all digital circuit in a CPLD chip, making simple structure and convenient debugging. And the general diagram, design idea, the benchmark waveform signal oscillating circuit, frequency synthesis circuit, phase synthesis circuit and D/A transformation circuit are given in the paper. The phase and frequency of the circuits are simulated.*

Streszczenie. *Zaprezentowano nową koncepcję genertatora sygnałów o częstotliwości przemysłowej wykorzystujący syntezę częstotliwości i fazy oraz przetwornik cyfrowo-analogowy. Układ bazuje na obwodzie XC2C64A (**Projekt generatora sygnałowego napięcia jednofazowego o częstotliwości przemysłowej**)*

Keywords: XC2C64A; frequency synthesis; phase synthesis; signal generator
Słowa kluczowe: synteza częstotliwości, generator sygnałowy.

Introduction

Power testing power is an important part of watt-hour meter verification device, according to requirements of electric verification regulation, power supply output in the sine wave frequency 45 ~ 65Hz continuous adjustable, phase need 0.0°-360.0°continuous adjustable [1]. The traditional signal generator is composed by using many general IC count circuit composition of counting circuit, frequency dividing circuit, phase lock loop circuit [2-3], frequency synthesis circuit, phase synthesis circuit, data output circuit and D/A transformation circuit [4]. This signal circuit is complex, board area is big, debugging complexly. XC2C64A-CPLD is applied to the signal generator circuit of industrial frequency power, making counting circuit, frequency dividing circuit, phase lock loop circuit, frequency synthesis circuit, phase synthesis circuit, data output circuit and D/A transformation circuit to focus on a chip solved some shortcomings of traditional circuit. It is brought great convenience for the production and debugging of industrial frequency power.

The overall structure of the signal generator circuitand its working principle

XC2C64A is one CPLD from CoolRunner-IIseries.It is inherited the advantages of XC9500,having high speed,easy use and super lower power consumption from XPLA3 series[5].Its delay time from pin to pin is only 3.5ns and Static current is less than 100uA. It has 64 macrocells,33 I/O ports and an additional I/O group to support voltage conversion and the connection with other device.Adopting the special RealDigital technology from Xilinx Company, which realizes low power consumption and high performance,allows it to be applied especially in the low power consumption device widely. The overall structure of the signal generator circuit made of CPLD is shown as figure 1.

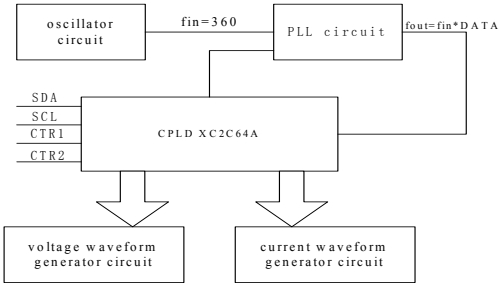

Fig.1.The overall structure of the signal generator circuit

XC2C64A has serial shift registers and two 12 bits pre-set counters inside which can be used to count to 3600.Then the singlechip will sends the needed frequency and phase data into CPLD,and the CPLD will ensures whether is it frequency or phase data,by judging these two control signals of CTR1 and CTR2.

One counter as a frequency divider of phase-locked loop circuit,will make the 360HZ double,and use the signal of frequency doubling as the address of needing voltage wave,which can drive the outer wave generator circuit,to generate the sine wave signal.The other counter as the wave address of current signalwill drive current wave generator circuit[6] to generate current signal.

The frequency and phasedata of the two sine wave signal will be sent into CPLD by serial mode.When CTR1 is enabled,the data is for frequency signal, its valuewhose is between 450 from 650, it show the frequency value is 45.0HZ to 65.0HZ.When CTR2 is enabled,the data is for phase signal,whose value is between 3000-0 and 0-600,show the phase value is between -60.0°- 0°and 0°-60.0°.The current counter's output address data is added the input data from singlechip to form the address of the outer wave generator.

The principle of the voltage and current wave signals generator circuit are as follows:The sine wave data which is placed in the EPROM,will be sent to D/A converter,and then to form the needing voltage and current wave signals.

The data which is written into EPROM are total 3600.It means that a sine wave of whole cycle is divided into 3600,and D-value of two adjacent data is 0.1°.The calculating formula is as follows:

(1) $$D = 7FH + 80H\sin\phi_i$$

where: ϕ_i =0.1,0.2,0.3…359.

The sine wave data are generated through Microsoft Visual C++ program,and then is written into EPROM by programming unit.One important point is the minimum value of this formula is 0,not negative.

The designof hardware circuit

a) The Design of Oscillator Circuit

The oscillator circuit is composed of 92.16KHZ crystal and CD4046.The schematic diagram is shown as figure 2.

The IC CD4046 is composed of an oscillator and 14 bits binary system serial counter.The oscillator can be RC or crystal circuit.Considering the precision of the Oscillator,the paper uses a 92.16KHZ crystal. The output frequency from Q_8 port shown in the figure 2 is:

(2) $$f_{out} = 92.16K \div 2^8 = 360\text{Hz}$$

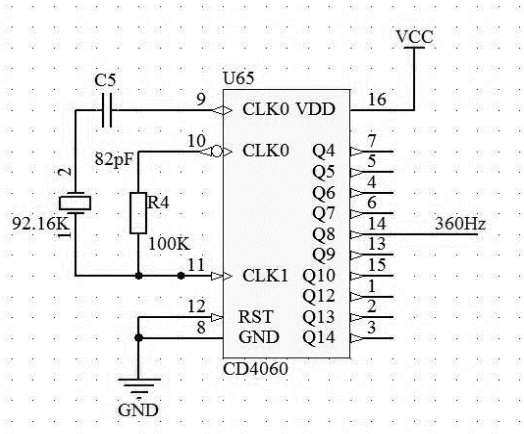

Fig.2. Oscillator circuit diagram

b) The Design of the Frequency Synthesise Circuit

The 360Hz frequency signal which is generated by oscillator circuit[7],through the phase-locked loop circuit composed of XC2C64A and CD4046,can generate new frequency signal for setting. The schematic diagram is shown as figure 3.

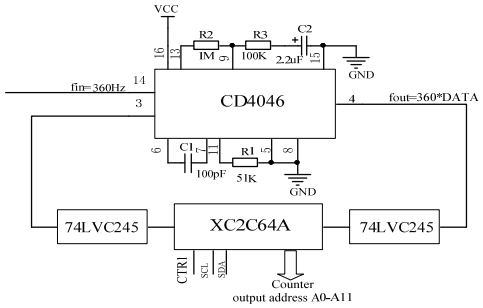

Fig.3 Frequency synthesizer circuit

The XC2C64A has a pre-set frequency divider.When the singlechip sends data into CLPD,the counter which is constituted by CPLDbegins to plus one continuously until its value reaches the pre-set data.At this time,the CPLD will send pulse signal which will be sent into the comparing input port of the phase-locked loop. Then the loop's output frequency is:

(3) $$f_{out} = 360 \times X$$

The XC2C64A counts continuously by the frequencyof f_{out} ,and sends the counter's state to its outer pinsas the output address data of EPROM.Thedatathrough the conversion of D/Agenerates the output sine wave signal.

The frequency of output sine wave signal is:

(4) $$f_{\sin} = \frac{360 \times X}{3600},$$

If X=501

Then: $f_{\sin} = \frac{360 \times 501}{3600} = 50.1Hz$

Obviously,the frequency resolution of this system is 0.1Hz.

c) theDesign of Phase Synthesise Circuit

The output signals of industrial frequency power have both voltage and current signals[8].If the voltage signal is sited to 0,by changing the phase of currentsignal and voltagesignal,the ahead or lag current signal will be got.The phase generator circuitfor the core to XC2C64Ais shown as figure 4.

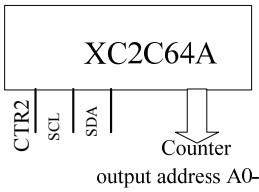

Fig.4 PhaseSynthesis circuit

After that the singlechip sendsthe phase data into XC2C64A, XC2C64A will see the data as offset address to plus it with the value from the voltage signal counter,to get the initial value of the current signal counter in the end.Because of the EPROM has 3600 data whose D-value of two adjacent data is 0.1°,each data correspond to an output data of EPROM.Therefore, the phase of voltage and current wave is:

(5) $$\Phi = \frac{X}{3600} \times 360,$$

If the input data is 301,the phase of voltage and current wave will be:

$$\Phi = \frac{X}{3600} \times 360 = 30.1^0$$

Obviously, its phase resolution is 0.1°.

d) The Design of Output Wave Circuit and D/A Circuit

The industrial frequency power has voltage and current data separately stored in two parallel EPROM working with 3.3V.The output data of those two counters in the XC2C64A is the output address data of those two EPROM.Then the data from EPROM will be sent to the same D/A circuit to be converted[9].The circuit is shown as figure 5.

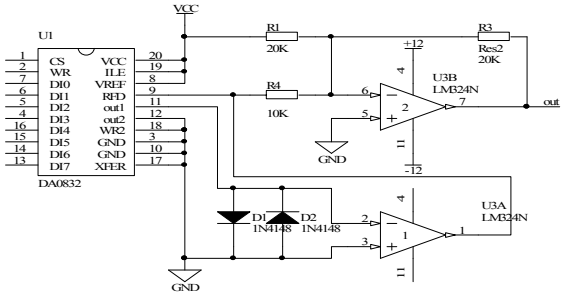

Fig.5 D / A converter circuit

The data which is converted is the output data from EPROM.TheD/A converter use DAC0832 in the straight connection mode.The amplifier uses LM324.Then theoutput voltage of the ambipolar amplifier is:

(6) $$V_O = (D - 128) \times \frac{V_{REF}}{2^8}$$

There into :D represents the output data from EPROM, whose value ranges from 0 to 255. V_{REF} represents the referenced voltage. The output signal of this circuit is ambipolar sine wave which is symmetrical compared with X axis.

The simulation result of VHDL language program

a) The Simulation of Frequency Synthesis Circuit

The data which is sent into XC2C64Ais450. It means that synthetic frequency is 45.0 Hz;the simulation diagram is shown as in figure 6. Figure 6 is a simulation diagram which is amplified, f_{in} is 360Hz whichisgenerated by oscillating circuit, f_{out} is the 360*450 frequency which is produced by phase lock loop. ADDR is the output address dataof XC2C64A, the output data controlsthe EPROM circulation to output 3600 sine dates, and realizesthe signal to produce.

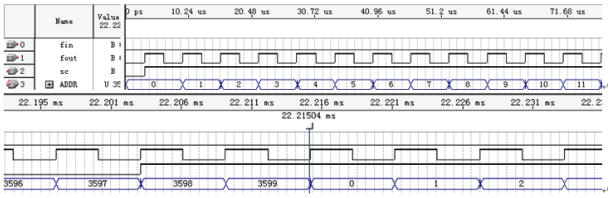

Fig.6 The simulation diagram of frequency synthesis

b) The Simulation of Phase Synthesis Circuit

Voltage phase is sited to 0, the phase data is sent input XC2C64A.The offset addressof current counter happens to migrate for voltage address,makes current and voltage to produce phase difference, the simulation results is shown as figure 7.

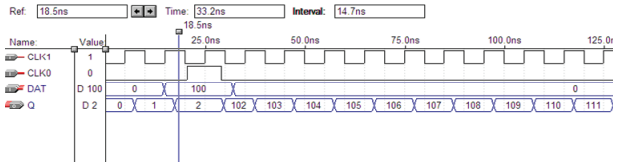

Fig.7 The simulation of phase synthesis

Figure 7, CLK1 is the output frequency by the PLL circuit, CLK0 is the benchmark frequency from the oscillation circuit,and DATis the phase information which is transmitted fromthe singlechip into XC2C64A, Q is the output data address by current data memory. As shown in figure 7, when the data is changed, the current data address happens to migrate, realizesto change of the phase offset.

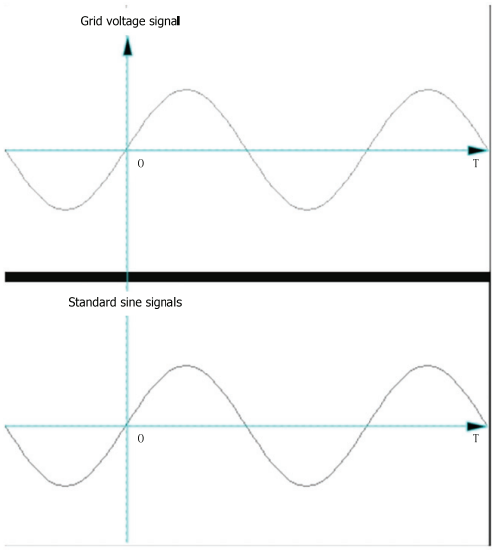

Fig.8 The simulation of signal waveform

The analysis of signal error

a) The Analysis of Wave Precision

Through reading the data in the sine wave table which is stored in the EPROM and then converted by D/A,the step-like analog sine wave signal is gained.Obviously,the data in the sine wave table affects the shape of step-like sine wave directly.According to the ideal sampling rule, the interval in the adjacent X（n）data is constant.Because the sampling number is limited,all sampling points aren't form a smooth sine wave,and the gap is called ΔR.

For a sine formula like $y = \sin x$, its slope is:

$$y' = \cos x$$

$$\text{Then, } y'' = -\sin x$$

Apparently, when the value of X is 0,the biggest slope value is gained.It means that the sine wave has the roughest signal wave and biggest error at this point.The absolute error is: $\sin 0.1 - \sin 0.0$

The relative error is[10]:

$$R = \frac{\sin 0.1 - \sin 0.0}{2} \times 100\% = 0.087\%$$

Obviously,low distortion rate of the sine wave like this is gained can by filter circuit.

b) *The Simulation Output Waveform*

The waveform got asshown figure 8 throughsimulatingthis system in MATLAB.

As shown figure 8, the signal waveform of this system is good, and is a high quality sine signal.

Conclusion

Comparing with analog power supply, the electronic power supply holds a leading position, because of continuously adjustable output,higher stable power supply and lower distortion rate. The phase synthesis circuit of traditional electronic power supply is composed of universal IC,as a result,has the following feature: complex circuit structure,high cost,high fault rate,big volume and great power consumption.However, by applying CPLD,the oscillator circuit has the character of CPLD,the cost and the labor intensitylargely decreased.

Acknowledgment

During the process of studying this system,great support was gained from students such as Liwen Yin,Shuai Wang,ZongmaChen and Yuwei Xu. R.B.G. thanks.

REFERENCES

[1] G.C. Hu, H.H. Xiao, "Design of the Signal Generator Circuit of Industrial frequency power sources," Electronic Technology, July. 2007, pp. 4–5. (in chinese)

[2] Q.Ma, Y.X.DAI, L.Q.Yi, "Software PLL of grid-connected PV power generation system based on DSP," Electric Power Automation Equipment, vol. 30, Feb.2010, pp. 99–102.(in chinese)

[3] X.J. Zheng, D.L.Chen, "Reference sinusoid circuit of grid-connected photovoltaic system based on software phase lock technique," Electric Power Automation Equipment, vol. 29, Jun. 2009, pp. 102–105. (in chinese)

[4] L.X. Jia, Y.Wang, "electronic systems design and practice," Tsinghua university press, beijing ,Feb. 2008. (in chinese)

[5] Y.H. Yu, Y.S.Dai, P.Wang, Y.ZYou, "Design of Wireless Well Logging Winch Signal Detecting Circuit Based on XC2C64," Electronic Engineering & Product World, vol. 16, Apr.2009, pp. 30–32. (in chinese)

[6] Bojoi, R.I. Griva, G. Bostan, V. Guerriero, M. Farina, F. Profumo, F.Current control strategy for power conditioners using sinusoidal signal integrators in synchronous reference frame. IEEE,Nov. 2005

[7] Lu, A.K, Roberts, G.W.An analog multi-tone signal generator for built-in-self-test applications. IEEE.2002

[8] X.G.Chen,Q.Fu,L.H.Zhou.Photovoltaic Grid-connected Inverter Control based on the technique of DSP phase-locked.Journal of the Graduates Sun YAT-SEN University(Natural Sciences.Medicine). 2007-03

[9] H.W.Ting, B.D.Liu, S.J.Chang. An on-chip concurrent high frequency analog and digital sinusoidal signal generator . IEEE.2004

[10] Y.X.Chen, "Distortion Control in the Sin Wave Form Based on Microprocessor," Instrumentation Technology, Mar. 2004, pp. 45–46. (in chinese)

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